★ 100% EAS Guaranteed
★ Green Device Available
★ Super Low Gate Charge
★ Excellent CdV/dt effect decline
★ Advanced high cell density Trench technology

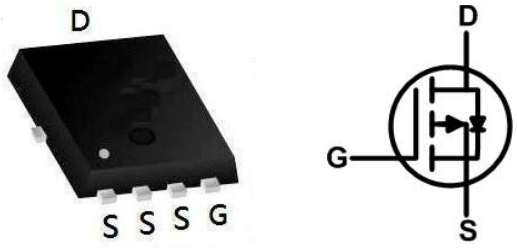
Product Summary

BVDSS	RDSON	ID
-30V	6mΩ	-65A

Description

The ZX 70P03N is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.
The ZX 70P03N meet the RoHS and Gree Product requirement 100% EAS guaranteed with full function reliability approved.

PDFN3*3 Pin Configuration



Package Marking and Ordering Information

Product	Package	Marking	Packing	Min Unit Quantity
ZX 70P03N	PDFN3*3	*	5000PCS/Reel	5000PCS

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current@-10V[1]	T_C=25℃	I_D	-65	A
	T_C=75℃		-35	
Pulsed Drain Current[2]		I_{DM}	-175	A
Single Pulse Avalanche Energy[3]		EAS	31	mJ
Avalanche Current		I_{AS}	-70	A
Total Power Dissipation[4]	T_C=25℃	P_D	31.2	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to+150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient[1]	$R_{\theta JA}$	61	°C/W
Thermal Resistance from Junction-to-Case[1]	$R_{\theta JC}$	4	°C/W

Electrical Characteristics T_c = 25°C, unless otherwise noted

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30	-	-	V
Gate-body Leakage current		I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T_J=25℃	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V	-	-	-1	μA
	T_J=55℃			-	-	-5	
Gate-Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.0	-1.6	-2.5	V
Drain-Source On-Resistance[2]		$R_{DS(on)}$	V_{GS} = -10V, I_D = -12A	-	6	8	mΩ
			V_{GS} = -4.5V, I_D = -8A	-	9.5	14.5	
Forward Transconductance		g_{fs}	V_{DS} = -5V, I_D = -20A	-	28	-	S
Dynamic Characteristics							
Input Capacitance		C_{iss}	V_{DS} = -15V, V_{GS} =0V, f =1MHz	-	4320	-	pF
Output Capacitance		C_{oss}		-	529	-	
Reverse Transfer Capacitance		C_{rss}		-	487	-	
Switching Characteristics							
Gate Resistance		R_g	V_{DS} = 0V, V_{GS}= 0V, f=1.0MHz	-	4.0	-	Ω
Total Gate Charge		Q_g	V_{GS} = -10V, V_{DS} = -15V, I_D= -15A	-	45	-	nC
Gate-Source Charge		Q_{gs}		-	8.5	-	
Gate-Drain Charge		Q_{gd}		-	12.8	-	
Turn-On Delay Time		$t_{d(on)}$	V_{GS} = -10V, V_{DD} = -15V, R_G = 2.5Ω, I_D= -15A	-	18.9	-	nS
Rise Time		t_r		-	15.7	-	
Turn-Off Delay Time		$t_{d(off)}$		-	64.8	-	
Fall Time		t_f		-	36.5	-	
Drain-Source Body Diode Characteristics							
Diode Forward Voltage[2]		V_{SD}	I_S = -1A, V_{GS} = 0V	-	-	-1	V
Continuous Source Current[1,5]		I_S	V_G=V_D=0V , Force Current	-	-	-65	A

Note :

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
3. The EAS data shows Max. rating . The test condition is V_{DD}= -25V, V_{GS}= -10V, L= 0.1mH, I_{AS}= -25A
4. The power dissipation is limited by 150℃ junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

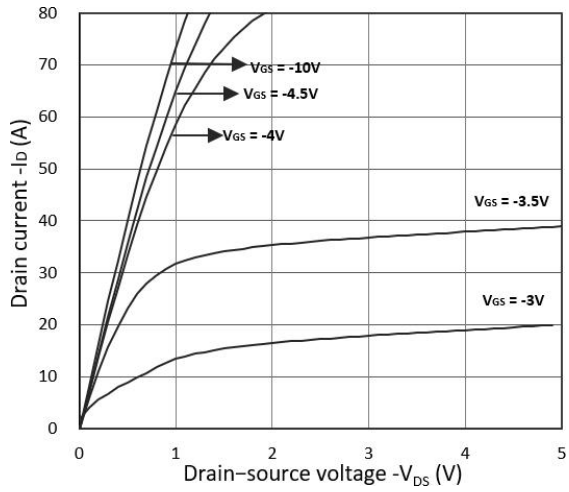


Figure 1. Output Characteristics

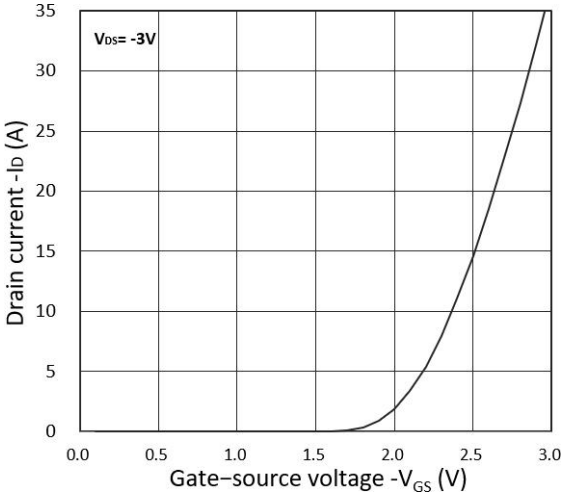


Figure 2. Transfer Characteristics

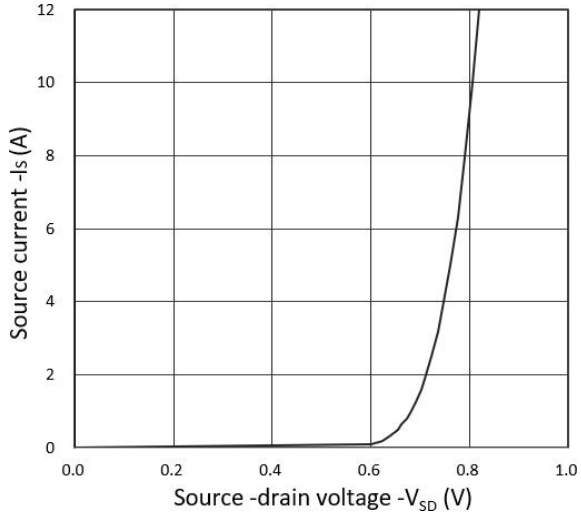


Figure 3. Forward Characteristics of Reverse

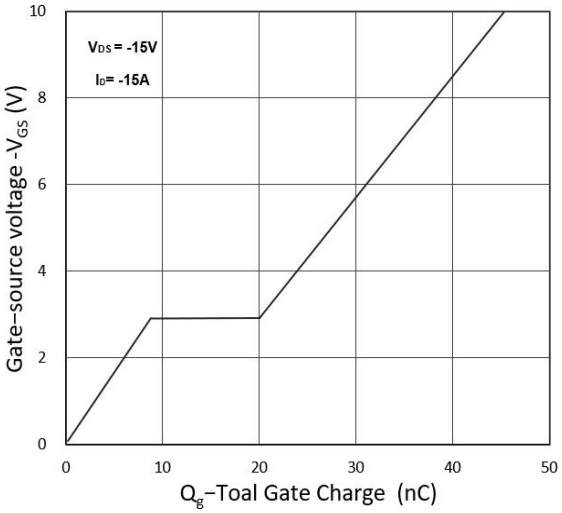


Figure 4. Gate Charge Characteristics

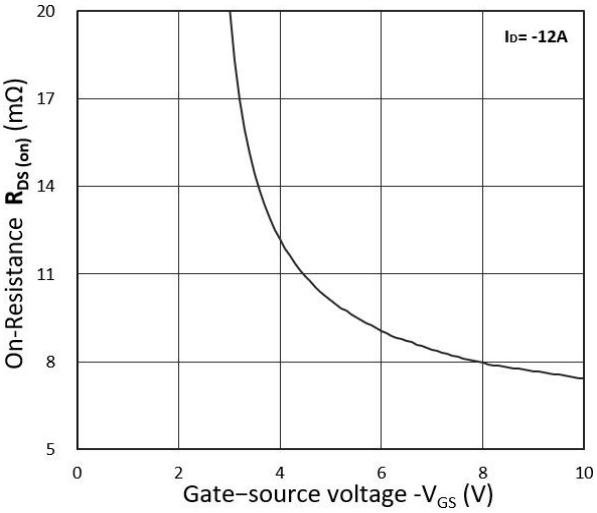


Figure 5. $R_{DS(on)}$ vs. V_{GS}

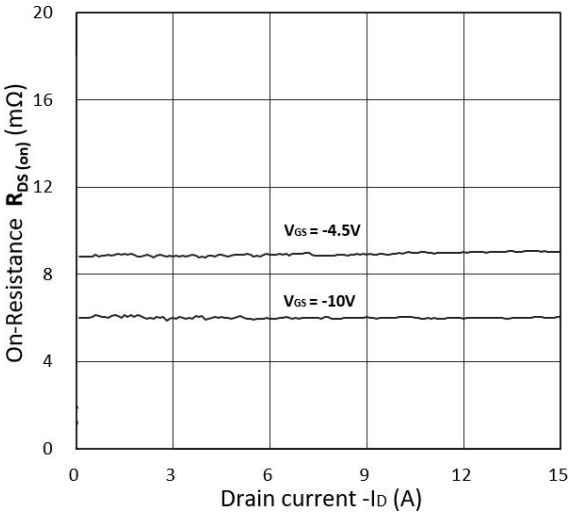


Figure 6. $R_{DS(on)}$ vs. I_D

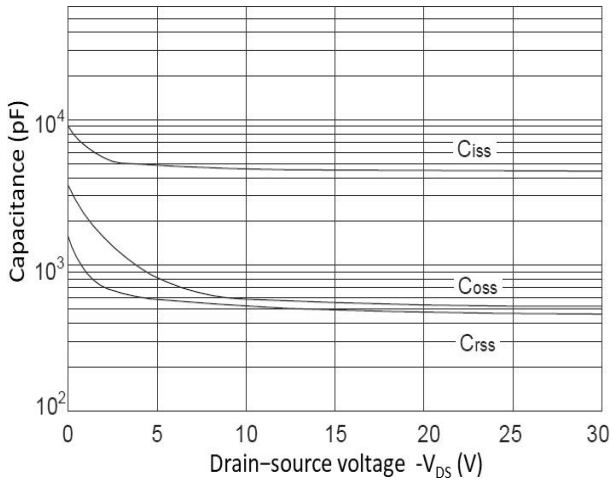


Figure 7. Capacitance Characteristics

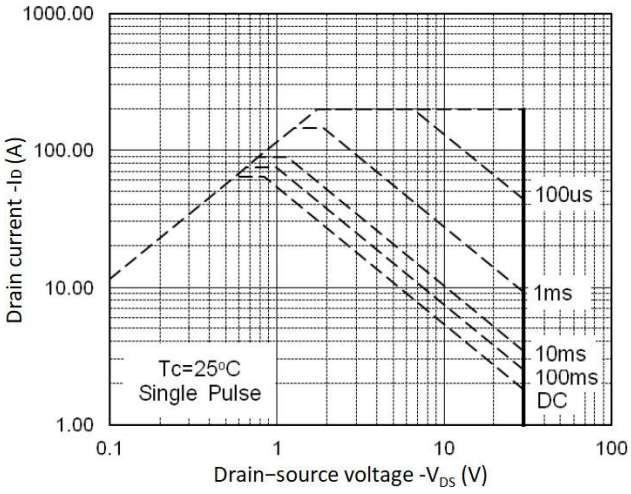


Figure 8. Safe Operating Area

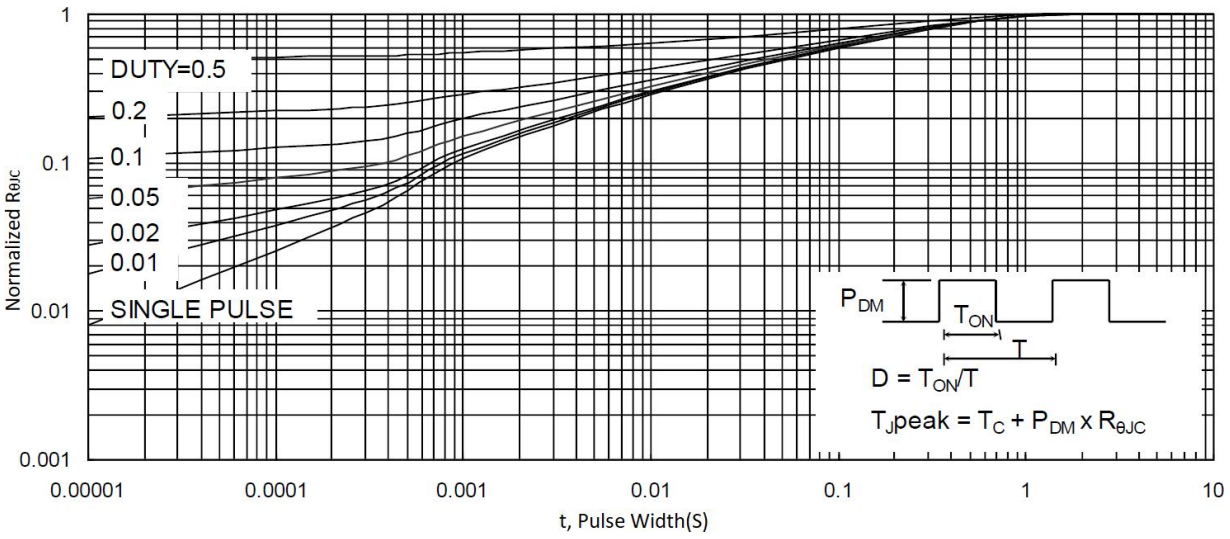


Figure 9. Normalized Maximum Transient Thermal Impedance

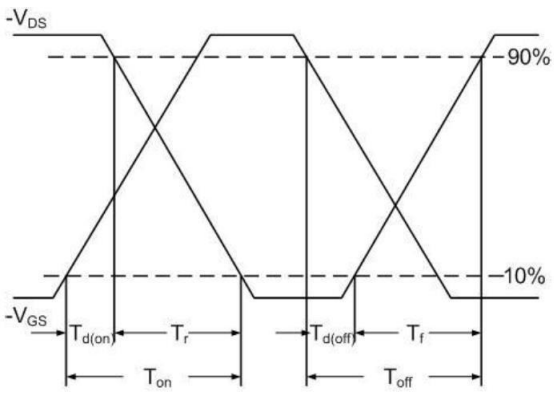


Figure 10. Switching Time Waveform

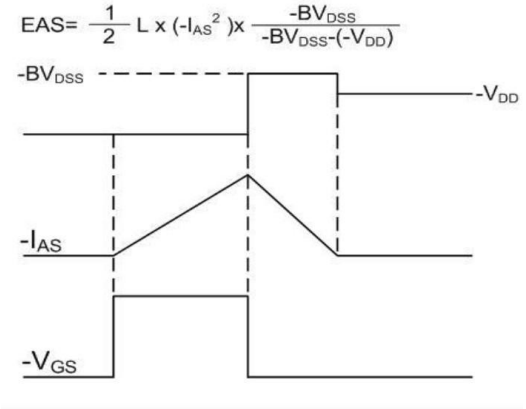
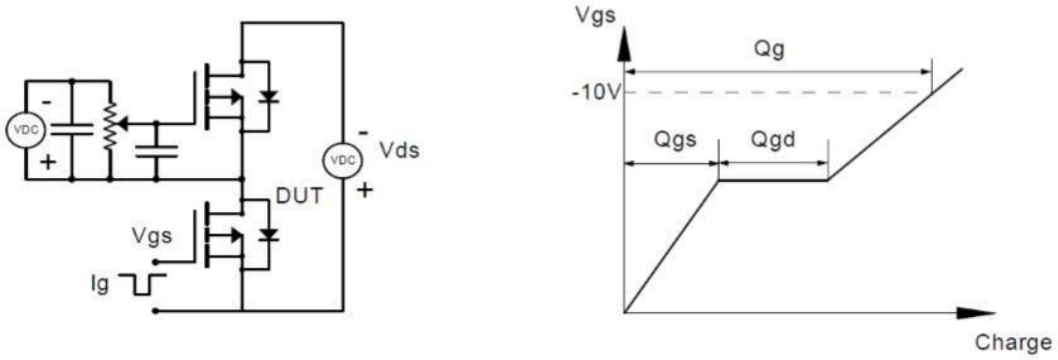


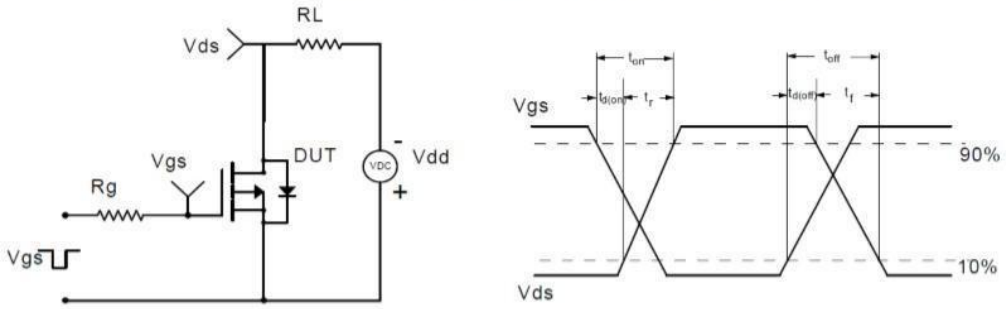
Figure 11. Unclamped Inductive Switching Waveform

Test Circuit

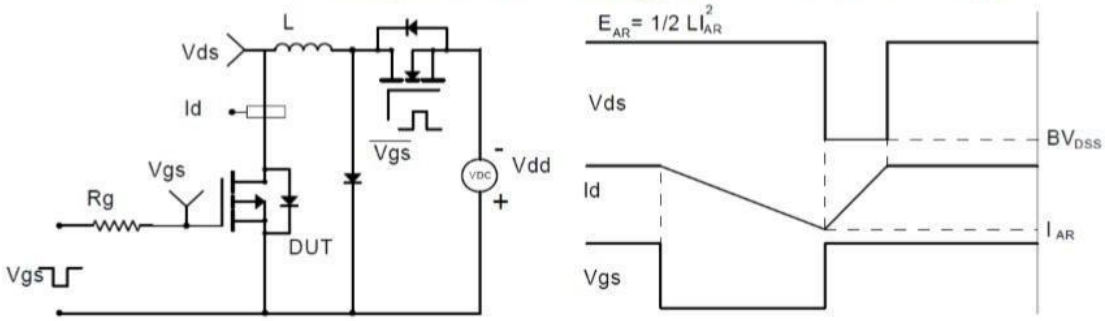
Gate Charge Test Circuit & Waveform



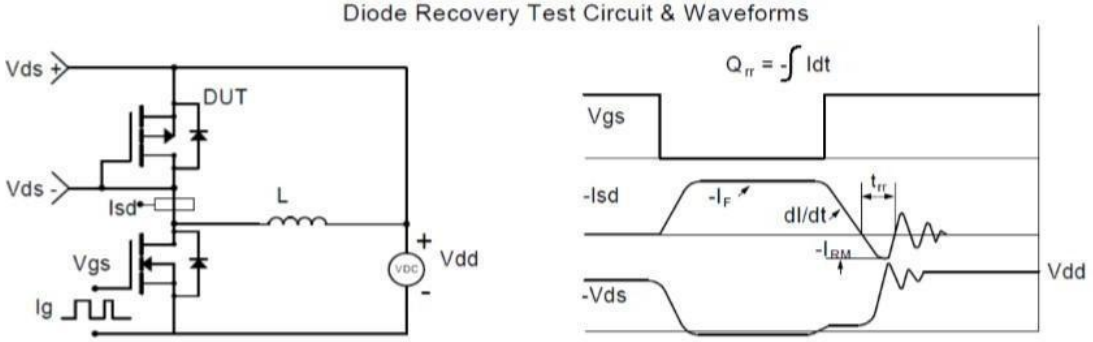
Resistive Switching Test Circuit & Waveforms



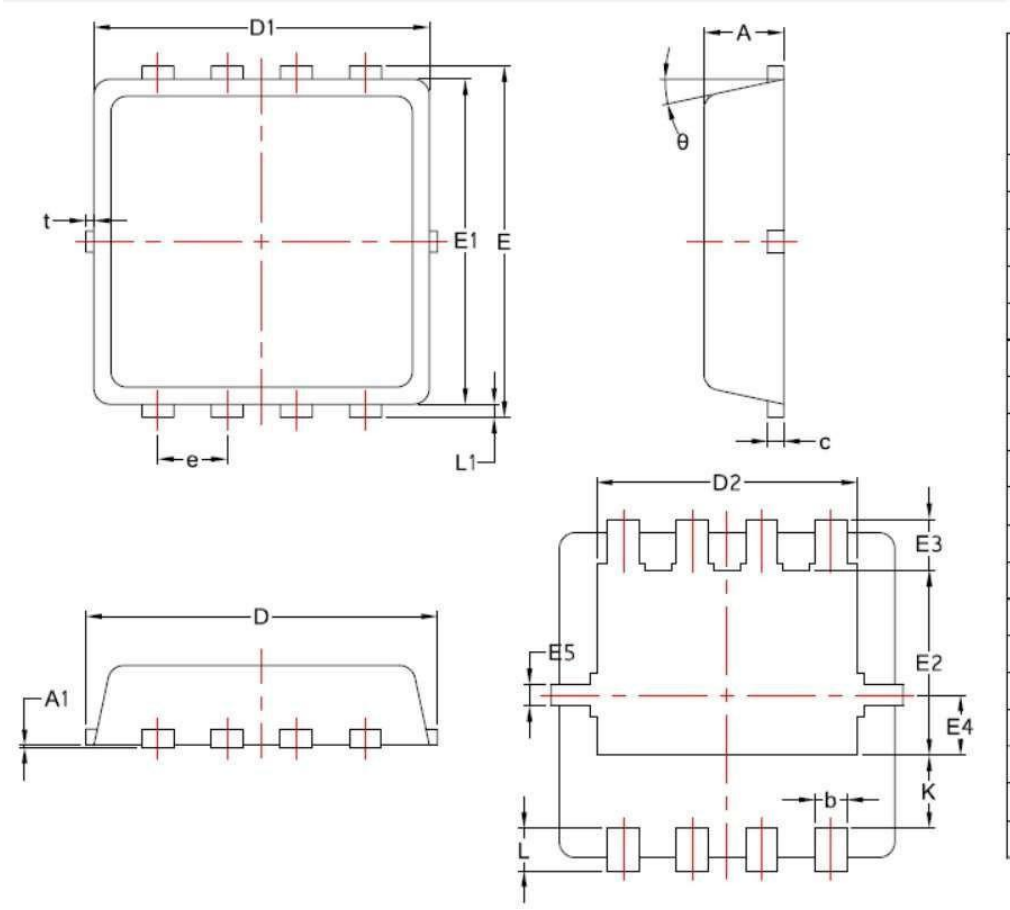
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Mechanical Data-DFN3*3-8L-Single



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
θ	10°	12°	14°