- ★ Super Low Gate Charge
- ★ Green Device Available
- ★ Excellent Cdv/dt effect decline
- ★ Advanced high cell density Trench technology

Product Summary

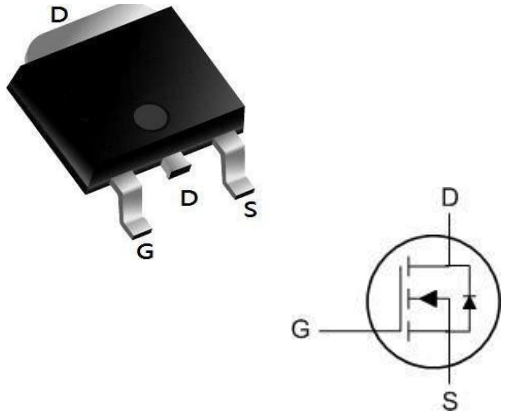
BVDSS	RDSON	ID
100V	20 mΩ	40A

Description

The ZX40N10 is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The ZX40N10 meet the RoHS and Green Productrequirement, 100% EAS guaranteed with full function reliability approved.

TO252 Pin Configuration



Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		100	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current note5	T_C = 25℃	40	A
I_D	Continuous Drain Current note5	T_C = 100℃	16	A
I_{DM}	Pulsed Drain Current note3		100	A
P_D	Power Dissipation note2	T_C = 25℃	27	W
I_{AS}	Avalanche Current note3,6		8	A
E_{AS}	Single Pulse Avalanche Energy note3,6		16	mJ
$R_{\theta JC}$	Thermal Resistance, Junction to Case		4.65	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient note1,4		62	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	100	-	-	V
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 80V, V_{GS} = 0V	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.8	2.6	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10V, I_D = 15A	-	20	23	mΩ
		V_{GS} = 4.5V, I_D = 10A	-	-	33	mΩ
g_{fs}	Forward Threshold Voltage	V_{DS}= 10V, I_D= 20A	-	22	-	S
R_g	Gate Resistance	V_{DS} = V_{GS}=0V, f = 1.0MHz	-	1.62	-	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1.0MHz	-	822	-	pF
C_{oss}	Output Capacitance		-	310	-	pF
C_{rss}	Reverse Transfer Capacitance		-	23.5	-	pF
Switching Characteristics						
Q_g	Total Gate Charge	V_{DS}= 50V, I_D = 20A, V_{GS} = 10V	-	22.7	-	nC
Q_{gs}	Gate-Source Charge		-	6.2	-	
Q_{gd}	Gate-Drain(“Miller”) Charge		-	5.3	-	
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 50V, I_D = 20A, R_G = 3Ω, V_{GS}=10V	-	15	-	ns
t_r	Turn-On Rise Time		-	3.2	-	
$t_{d(off)}$	Turn-Off Delay Time		-	30	-	
t_f	Turn-Off Fall Time		-	7.6	-	
Diode Characteristics						
I_S	Continuous Source Current		-	-	40	A
V_{SD}	Diode Forward Voltage	I_S=20A . V_{GS} = 0V	-	0.88	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD}=20A, dI_{SD}/dt=100A/μs	-	45	-	ns
Q_{rr}	Reverse Recovery Charge		-	59	-	nC

Notes:

1. The value of $R_{\theta JC}$ is measured in a still air environment with TA =25°C and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

2. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

3. Single pulse width limited by junction temperature $T_{J(MAX)}$=150°C.

4. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

5. The maximum current rating is package limited.

6. The EAS data shows Max. rating. The test condition is V_{DS}=50V,V_{GS}=10V,L=0.5mH

Typical Performance Characteristics

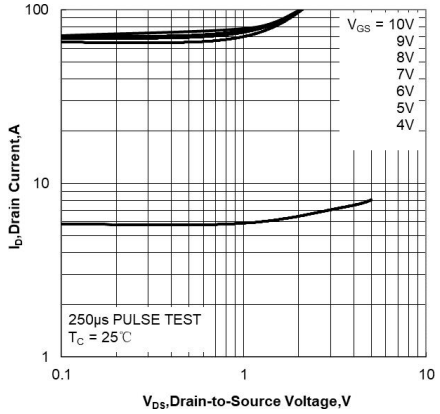


Figure 1. Output Characteristics

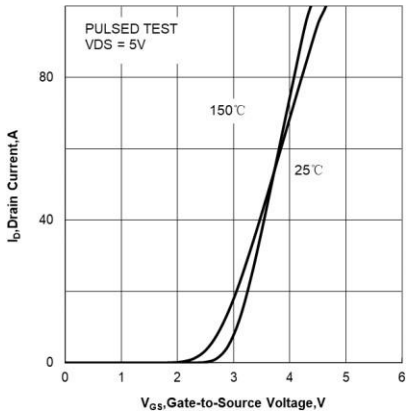


Figure 2. Transfer Characteristics

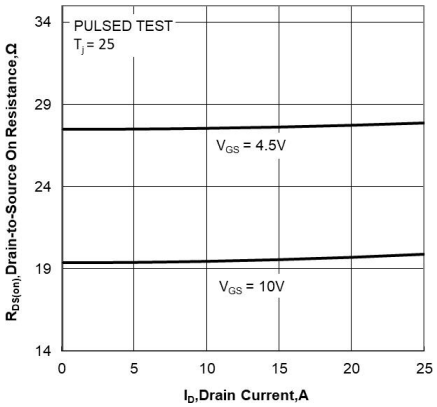


Figure 3. Drain-to-Source On Resistance vs Drain Current

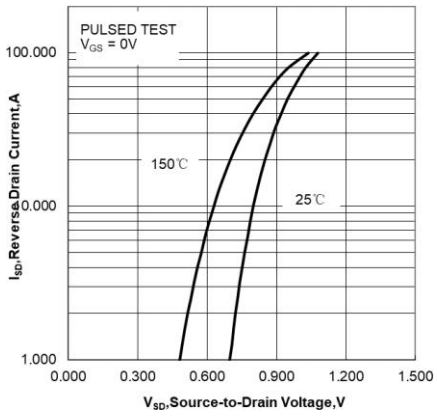


Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

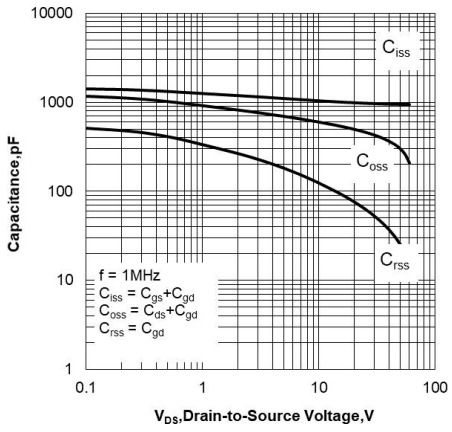


Figure 5. Capacitance Characteristics

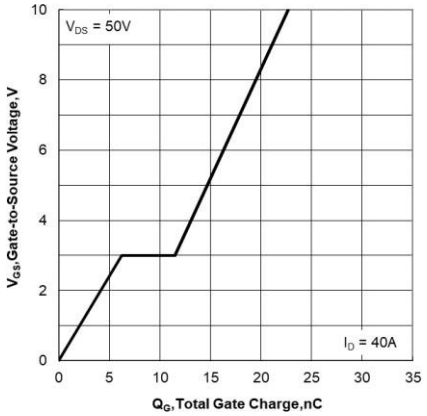


Figure 6. Gate Charge Characteristics

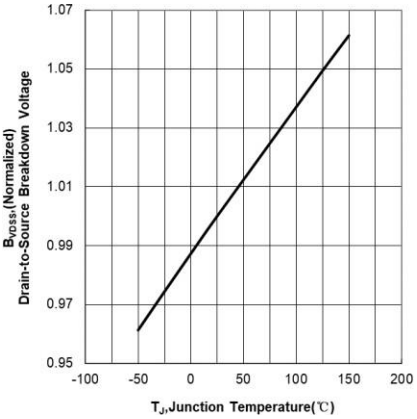


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

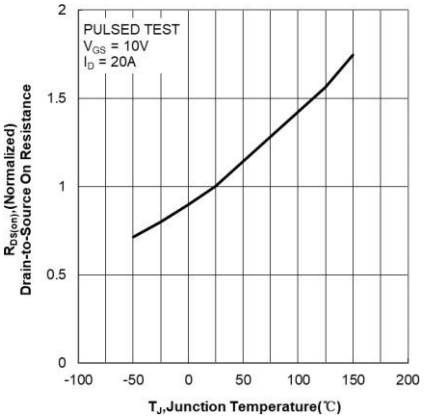


Figure 8. Normalized On Resistance vs Junction Temperature

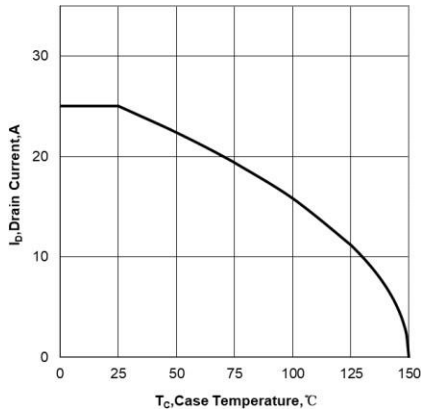


Figure 9. Maximum Continuous Drain Current vs Case Temperature

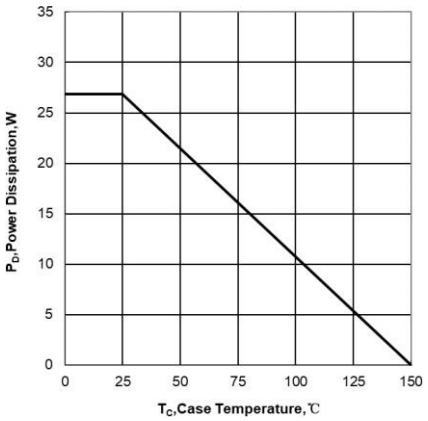


Figure 10. Maximum Power Dissipation vs Case Temperature

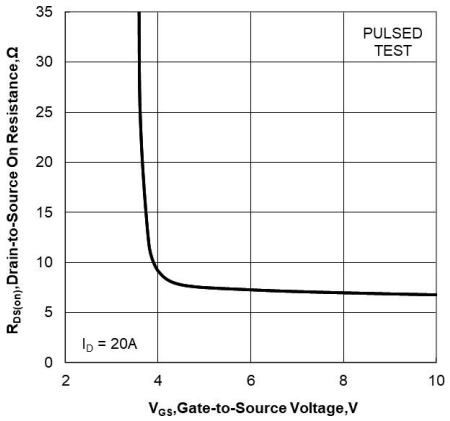


Figure11. Drain-to-Source On Resistance vs Gate

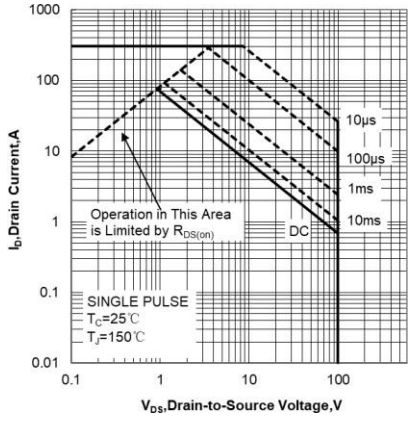


Figure 12. Maximum Safe Operating Area

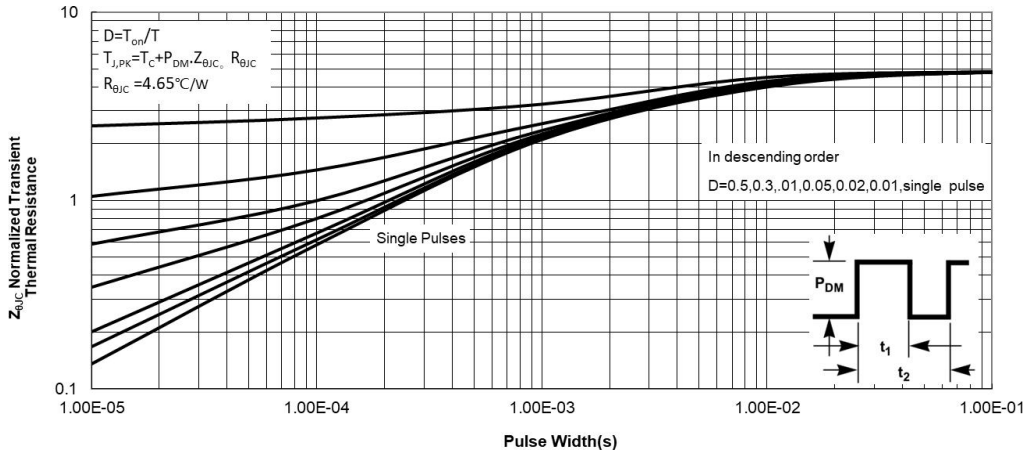
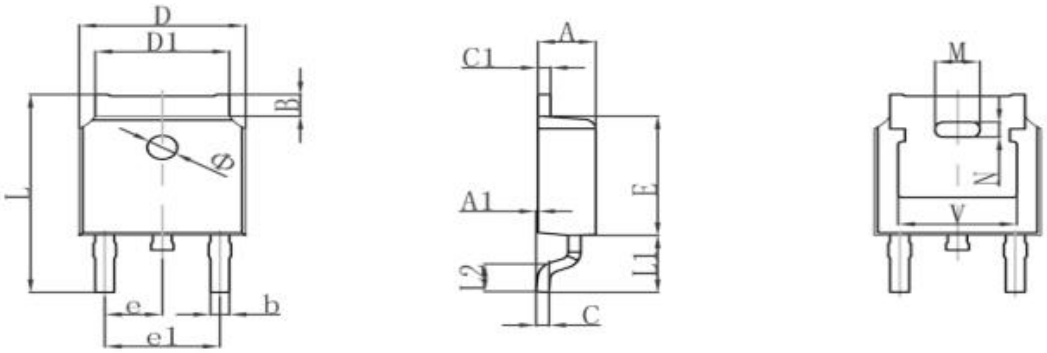


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

TO-252 Package outline



Symbol	DimensionsIn Millimeters		DimensionsIn Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.380	0.087	0.094
A1	0.000	0.100	0.000	0.004
B	0.800	1.400	0.031	0.055
b	0.710	0.810	0.028	0.032
c	0.460	0.560	0.018	0.022
c1	0.460	0.560	0.018	0.022
D	6.500	6.700	0.256	0.264
D1	5.130	5.460	0.202	0.215
E	6.000	6.200	0.236	0.244
e	2.286TYP		0.090TYP	
e1	4.327	4.727	0.170	0.186
M	1.778REF		0.070REF	
N	0.762REF		0.018REF	
L	9.800	10.400	0.386	0.409
L1	2.9REF		0.114REF	
L2	1.400	1.700	0.055	0.067
V	4.830REF		0.190REF	
Φ	1.100	1.300	0.043	0.051