General Description

The ZX 250N55K uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a wide variety of applications.

Features

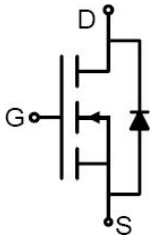
- Low Gate Charge
- 100% UIS Tested, 100% DVDS Tested
- High Power and current handing capability
- Lead free product is acquired

Application

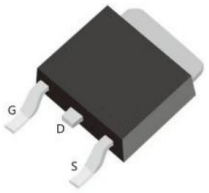
- PWM Applications
- Load Switch
- Power Management

Key Performance Parametes

Parameter	Value	Unit
V_{DS}	250	V
$R_{DS(ON)_TYP}$	550	mΩ
I_D	8	A
Q_G	29	nC



Schematic Diagram



TO-252 top view

RoHS

Package Marking and Ordering Information

Device/Ordering Code	Marking	Package	Packing	Reel Size	Tape width	Quantity
ZX 250N55K	*	TO-252	Tape	\	\	2500 Pcs

Table 1. Absolute Maximum Ratings (T_C=25℃ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage (V_{GS}=0V)	250	V
V_{GS}	Gate-Source Voltage (V_{DS}=0V)	±20	V
I_D	Drain Current-Continuous(T_C=25℃)	8	A
	Drain Current-Continuous(T_C=100℃)	5	A
$I_{DM\ (pluse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	32	A
P_D	Maximum Power Dissipation(T_C=25℃)	60	W
	Maximum Power Dissipation(T_C=100℃)	23.8	W
E_{AS}	Avalanche energy (Note 2)	10	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	℃

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		2.1	°C/W

Table 3. Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	250			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=200V, V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V, V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=4A		8		S
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=4A		550	675	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=25V,V_{GS}=0V, f=1.0MHz		842		pF
C_{oss}	Output Capacitance			18		pF
C_{rss}	Reverse Transfer Capacitance			8.7		pF
Rg	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1.0MHz		0.6		Ω
Switching Parameters						
$t_{d(on)}$	Turn-on Delay Time	V_{GS}=10V, V_{DS}=100V, R_L=25Ω, R_{GEN}=5Ω		13		nS
t_r	Turn-on Rise Time			10		nS
$t_{d(off)}$	Turn-Off Delay Time			40		nS
t_f	Turn-Off Fall Time			9		nS
Q_g	Total Gate Charge	V_{GS}=10V, V_{DS}=100V, I_D=4A		29		nC
Q_{gs}	Gate-Source Charge			4.6		nC
Q_{gd}	Gate-Drain Charge			9.8		nC
Source-Drain Diode Characteristics						
I_{SD}	Source-Drain Current (Body Diode)				9	A
V_{SD}	Forward on Voltage (Note 2)	V_{GS}=0V, I_S=4A			1.2	V
t_{rr}	Reverse Recovery Time	I_F=4A, dI/dt=100A/μs		80		ns
Q_{rr}	Reverse Recovery Charge	I_F=4A, dI/dt=100A/μs		282		nC

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature.
Notes 2.E_{AS} condition: T_J=25℃,V_{DD}=60V,V_G=10V, Rg=25Ω, L=0.5mH.
Notes 3.Repetitive Rating: Pulse width limited by maximum junction temperature.

Characteristics Curve:

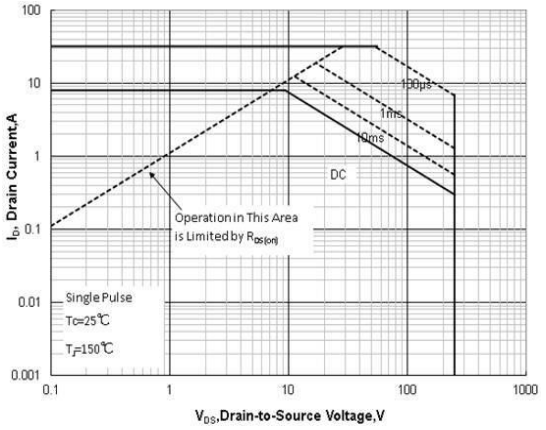


Figure 1 Maximum Forward Bias Safe Operating Area

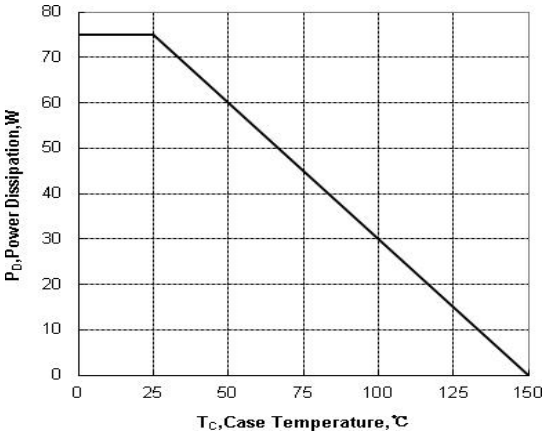


Figure 2 Maximum Power dissipation vs Case Temperature

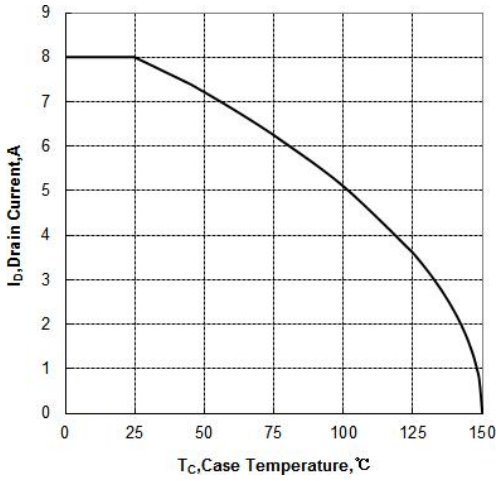


Figure 3 Maximum Continuous Drain Current vs Case Temperature

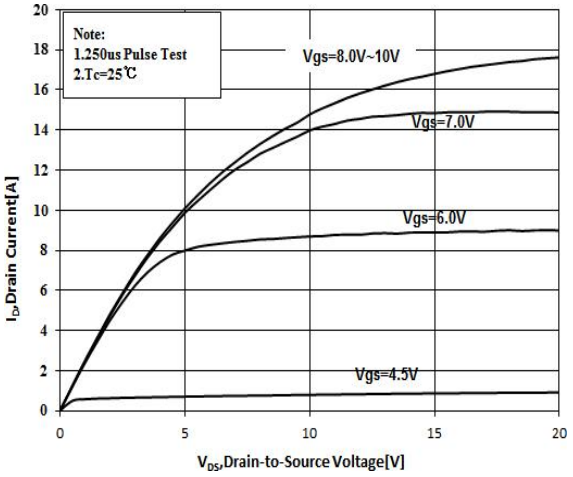


Figure 4 Typical Output Characteristics

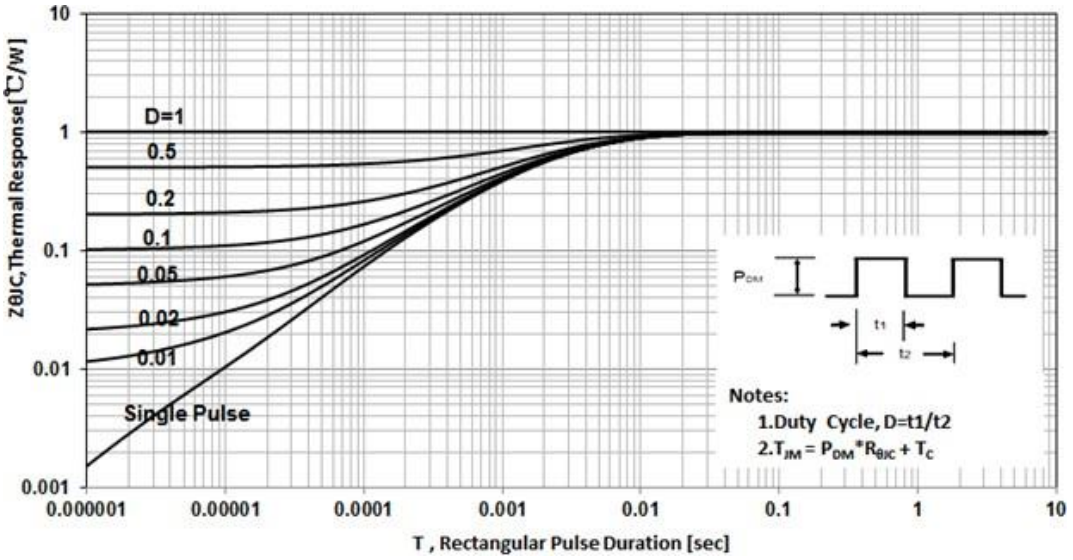


Figure 5 Maximum Effective Thermal Impedance , Junction to Case

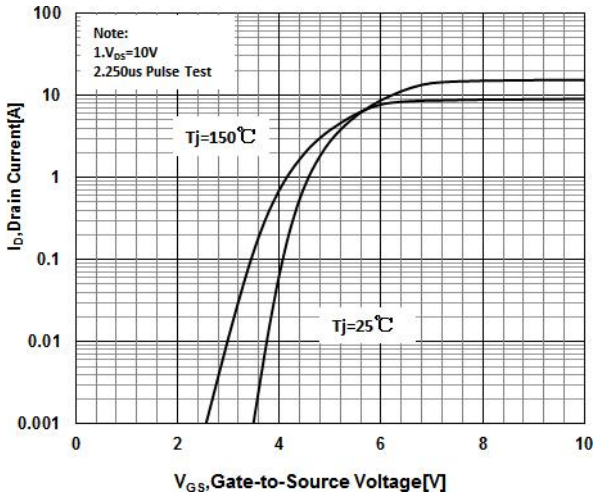


Figure 6 Typical Transfer Characteristics

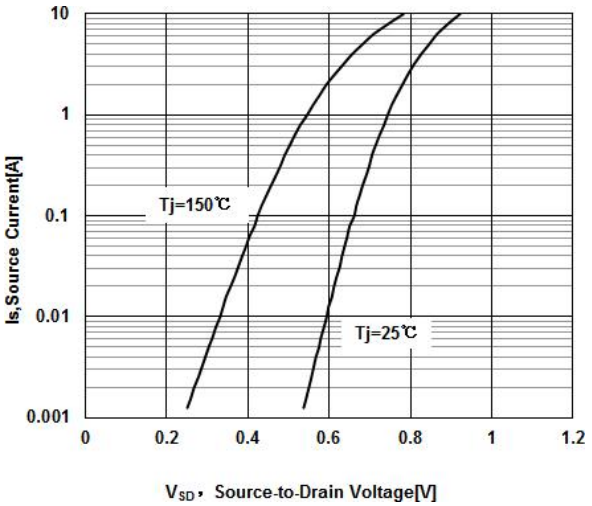


Figure 7 Typical Body Diode Transfer Characteristics

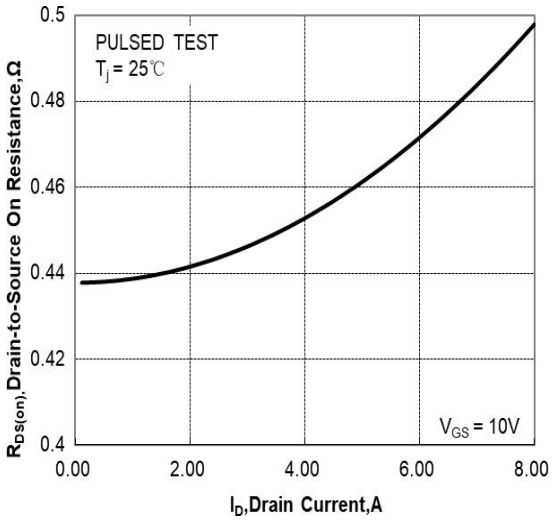


Figure 8 Typical Drain to Source ON Resistance vs Drain Current

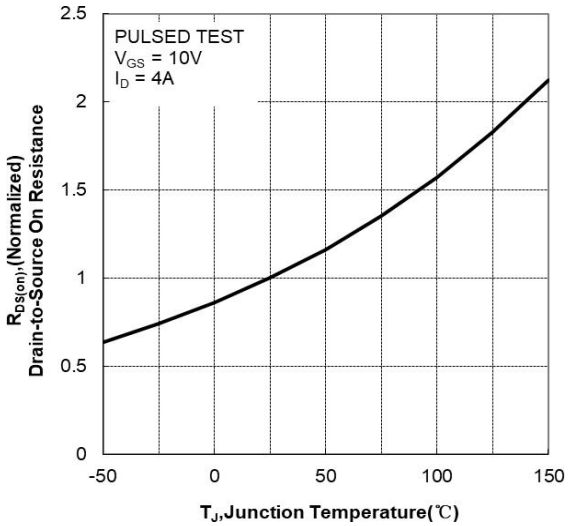


Figure 9 Typical Drian to Source on Resistance vs Junction Temperature

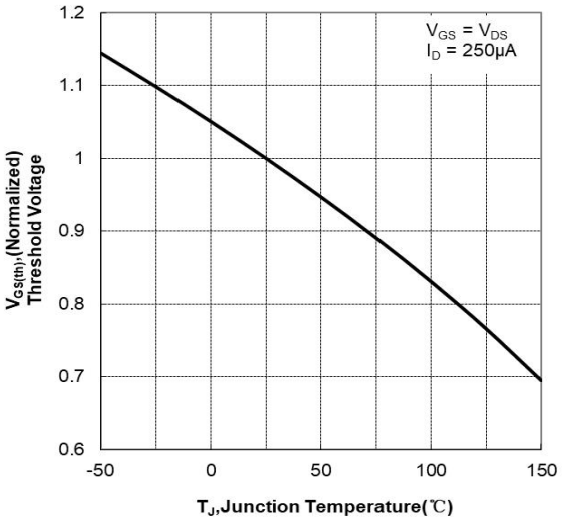


Figure 10 Typical Theshold Voltage vs Junction Temperature

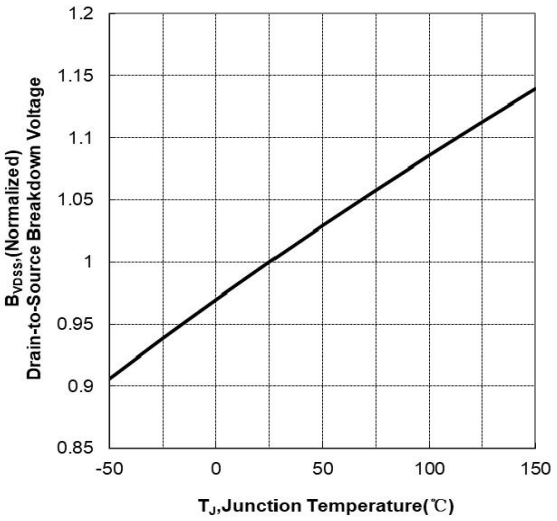


Figure 11 Typical Breakdown Voltage vs Junction Temperature

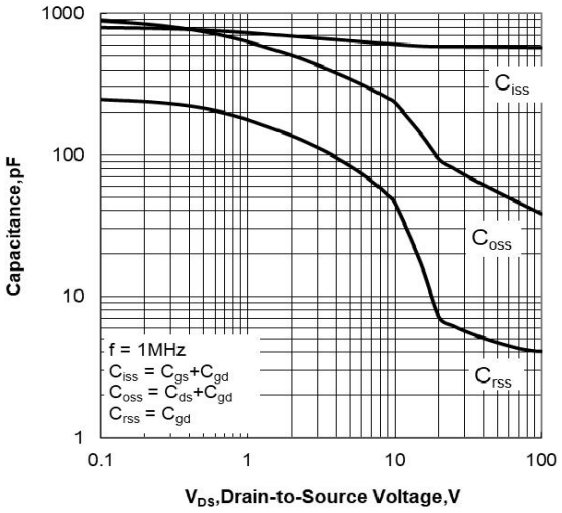


Figure 12 Typical Capacitance vs Drain to Source Voltage

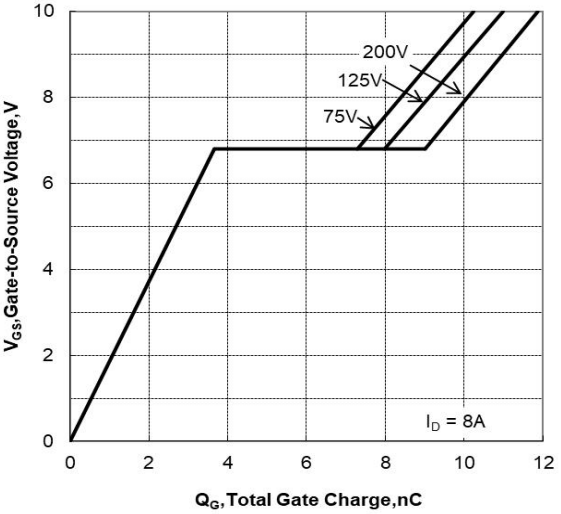


Figure 13 Typical Gate Charge vs Gate to Source Voltage

Test Circuit and Waveform

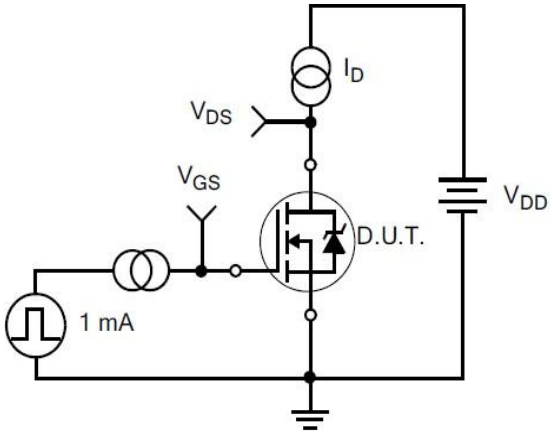


Figure 14. Gate Charge Test Circuit

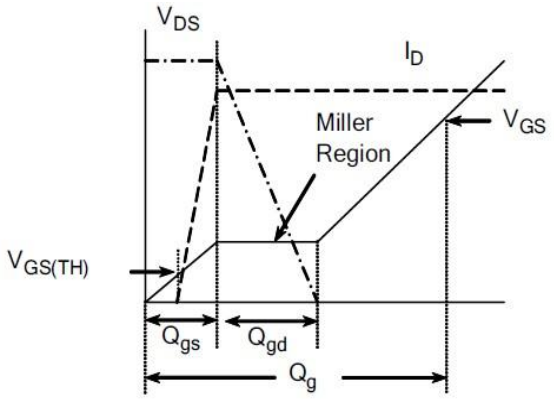


Figure 15. Gate Charge Waveforms

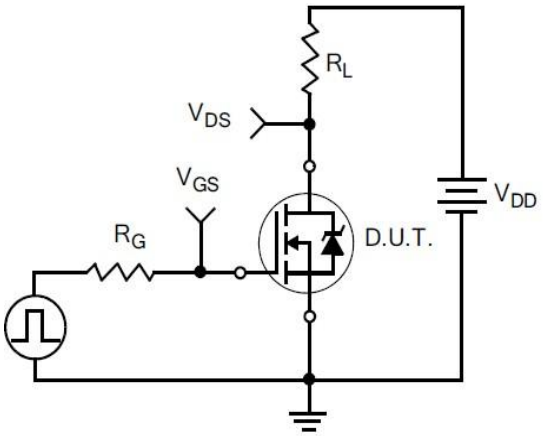


Figure 16. Resistive Switching Test Circuit

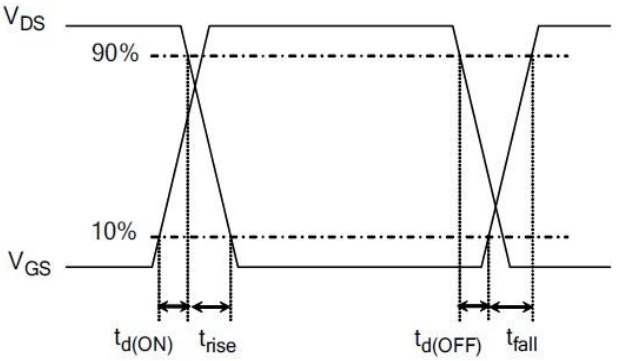


Figure 17. Resistive Switching Waveforms

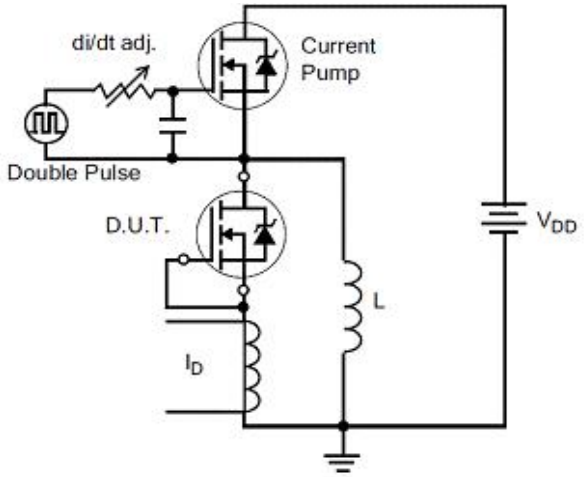


Figure 18. Diode Reverse Recovery Test Circuit

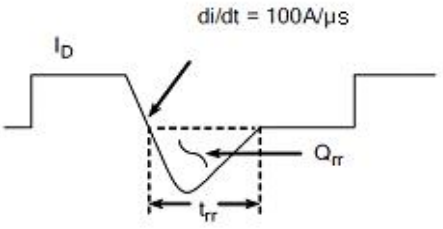


Figure 19. Diode Reverse Recovery Waveform

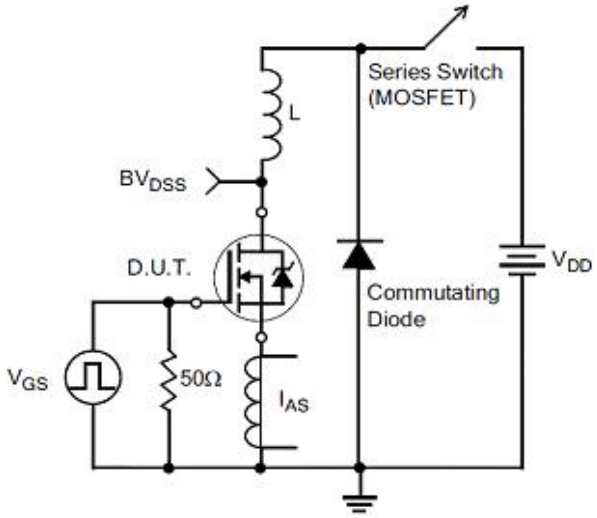


Figure20.Unclamped Inductive Switching Test Circuit

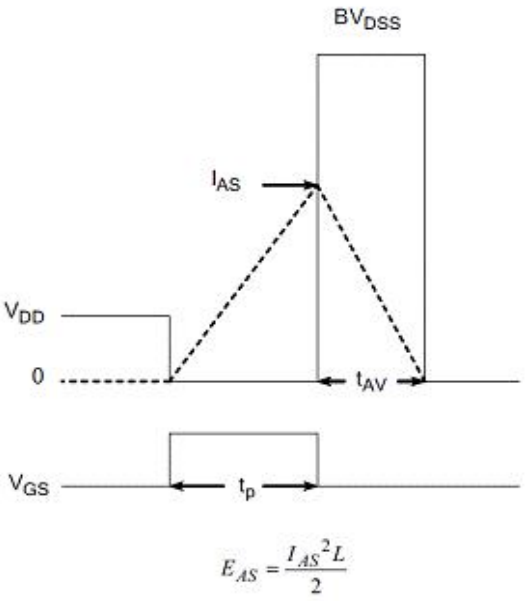
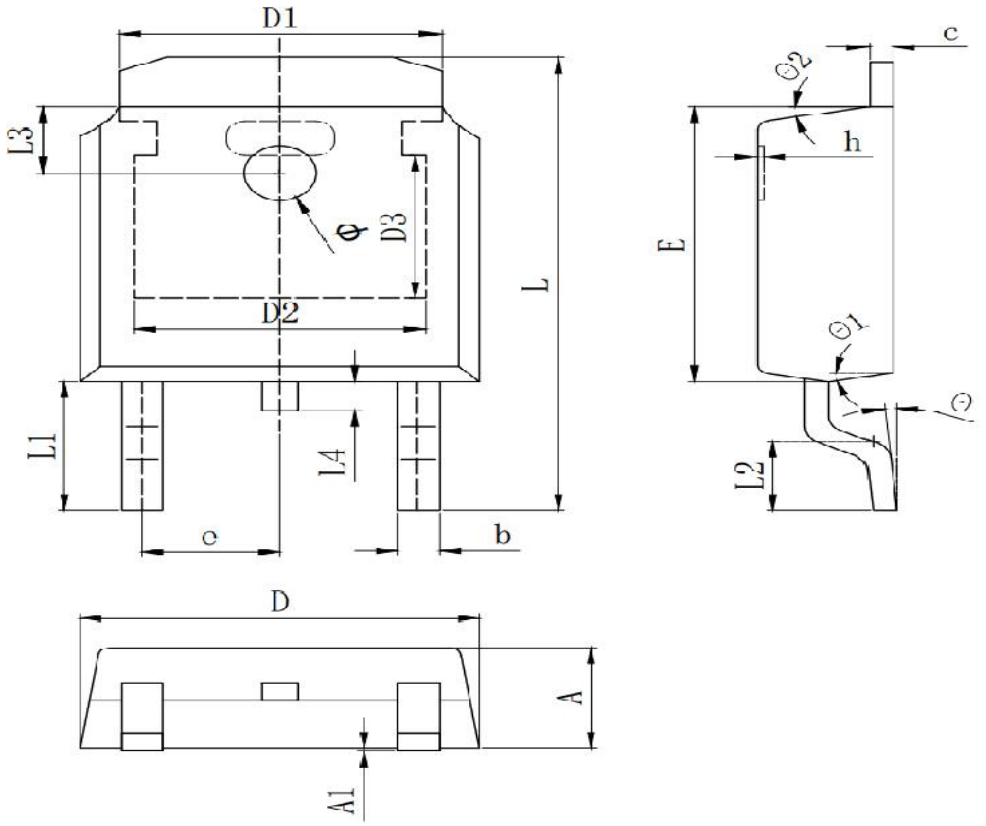


Figure21.Unclamped Inductive Switching Waveform

TO-252 Package Information



Symbol	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	2.200	2.300	2.400
A1	0.000		0.127
b	0.640	0.690	0.740
c(电镀后)	0.460	0.520	0.580
D	6.500	6.600	6.700
D1	5.334 REF		
D2	4.826 REF		
D3	3.166 REF		
E	6.000	6.100	6.200
e	2.286 TYP		
h	0.000	0.100	0.200
L	9.900	10.100	10.300
L1	2.888 REF		
L2	1.400	1.550	1.700
L3	1.600 REF		
L4	0.600	0.800	1.000
Φ	1.100	1.200	1.300
θ	0°		8°
θ1	9° TYP		
θ2	9° TYP		