**Product Summary**

- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

| $V_{(BR)DSS}$ | $R_{DS(ON)}$ | $I_D$ |
|---|---|---|
| -30V | 7.5mΩ @-10V | -15A |
| | 12mΩ @ -4.5V | |

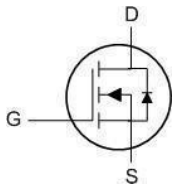
## ■ Description

The AO4409 isthe high cell density trenched N-ch MOSFETs , which provide excellent RDSON and gate charge for most of the synchronous buck converter-applications.
The AO4409 meet the RoHS and Green Product requirement , 100 % EAS guaranteed with full function reliability approved

SOP8




**pin assignment**




**Schematic diagram**

## ■ Order Information

| Product | Package | Marking | Packing | Min Unit Quantity |
|---|---|---|---|---|
| AO4409 | SOP8 | * | 3000PCS/Reel | 3000PCS |

## ■ Absolute Maximum Ratings Ta = 25℃

| Parameter | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -30 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | |
| Continuous Drain Current | $T_A$=25°C | $I_D$ | -15 | A |
| | $T_A$=70°C | | -12.8 | |
| Pulsed Drain Current | | $I_{DM}$ | -80 | |
| Avalanche Current | | $I_{AS}$,$I_{AR}$ | 30 | |
| Avalanche energy | L=0.1mH | $E_{AS}$,$E_{AR}$ | 135 | mJ |
| Power Dissipation | $T_A$=25°C | $P_D$ | 3.1 | W |
| | $T_A$=70°C | | 2 | |
| Thermal Resistance.Junction- to-Ambient | t ⩽ 10s | $R_{thJA}$ | 40 | ℃/W |
| | Steady-State | | 75 | |
| Thermal Resistance.Junction- to-Lead | | $R_{thJL}$ | 24 | |
| Junction Temperature | | $T_J$ | 150 | ℃ |
| Junction Storage Temperature Range | | $T_{stg}$ | -55 to 150 | |

## ■ Electrical Characteristics Ta = 25℃

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $V_{DSS}$ | $I_D$=-250 μA, $V_{GS}$=0V | -30 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=-30V, $V_{GS}$=0V | | | -5 | uA |
| | | $V_{DS}$=-30V, $V_{GS}$=0V, $T_J$=55℃ | | | -25 | |
| Gate-Body leakage current | $I_{GSS}$ | $V_{DS}$=0V, $V_{GS}$=±20V | | | ±100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$ $I_D$=-250 μA | -1.4 | | -2.7 | V |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | $V_{GS}$=-10V, $I_D$=-15A | | | 7.5 | mΩ |
| | | $V_{GS}$=-10V, $I_D$=-15A $T_J$=125℃ | | | 11.5 | |
| | | $V_{GS}$=-4.5V, $I_D$=-10A | | | 12 | |
| On state drain current | $I_{D(ON)}$ | $V_{GS}$=-10V, $V_{DS}$=-5V | -80 | | | A |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$=-5V, $I_D$=-15A | 35 | 50 | | S |
| Input Capacitance | $C_{iss}$ | $V_{GS}$=0V, $V_{DS}$=-15V, f=1MHz | | 5270 | 6400 | pF |
| Output Capacitance | $C_{oss}$ | | | 945 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 745 | | |
| Gate resistance | $R_g$ | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | | 2 | 3 | Ω |
| Total Gate Charge (10V) | $Q_g$ | $V_{GS}$=-10V, $V_{DS}$=-15V, $I_D$=-15A | | 100 | 120 | nC |
| Total Gate Charge (4.5V) | | | | 51.5 | | |
| Gate Source Charge | $Q_{gs}$ | | | 14.5 | | |
| Gate Drain Charge | $Q_{gd}$ | | | 23 | | |
| Turn-On DelayTime | $t_{d(on)}$ | $V_{GS}$=-10V, $V_{DS}$=-15V, $R_L$=1Ω, $R_{GEN}$=3Ω | | 14 | | ns |
| Turn-On Rise Time | $t_r$ | | | 16.5 | | |
| Turn-Off DelayTime | $t_{d(off)}$ | | | 76.5 | | |
| Turn-Off Fall Time | $t_f$ | | | 37.5 | | |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $I_F$=-15A, $dI/dt$=100A/us | | 36.7 | 45 | |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | | 28 | | nC |
| Maximum Body-Diode Continuous Current | $I_S$ | | | | -5 | A |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=-1A,$V_{GS}$=0V | | | -1 | V |

Note : The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

## ■ Typical Performance Characteristics

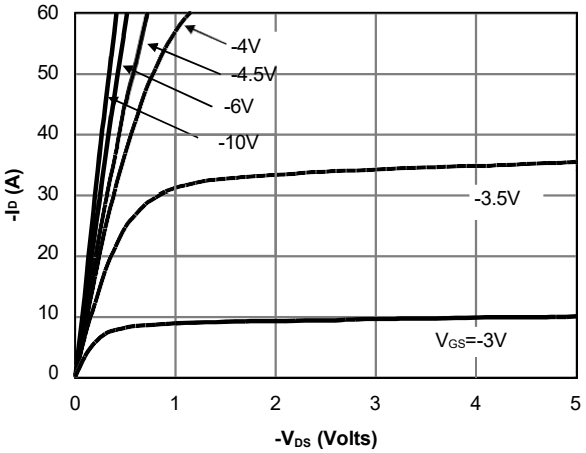



Fig 1: On-Region Characteristics (Note E)

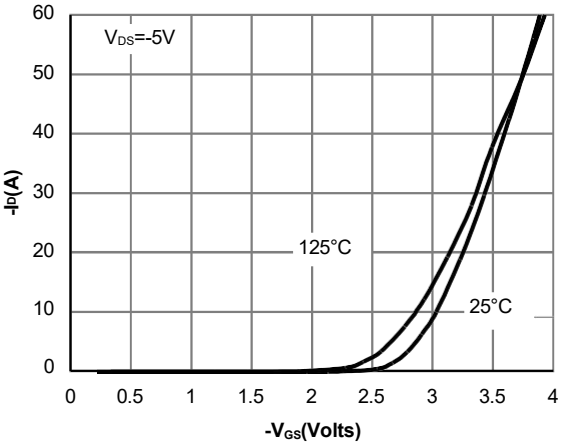



Figure 2: Transfer Characteristics (Note E)

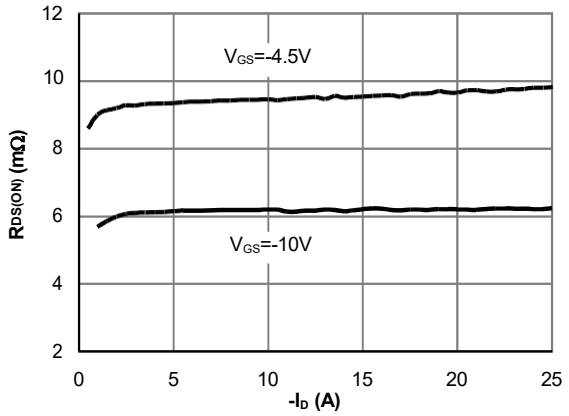



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

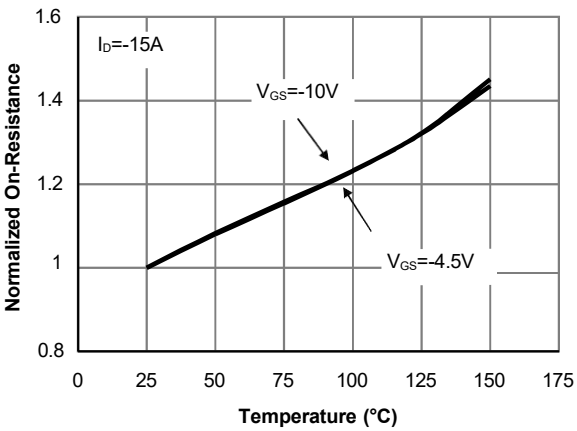



Figure 4: On-Resistance vs. Junction Temperature (Note E)

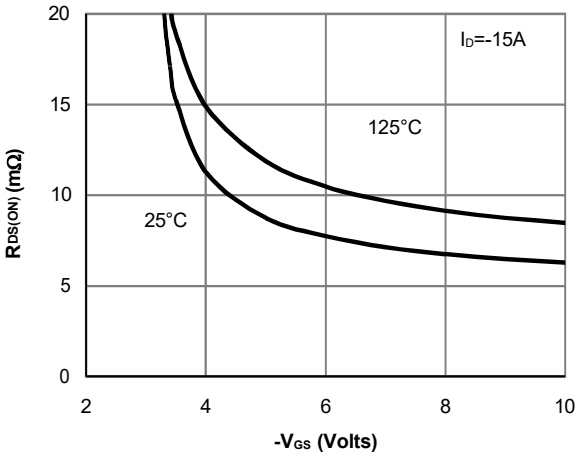



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

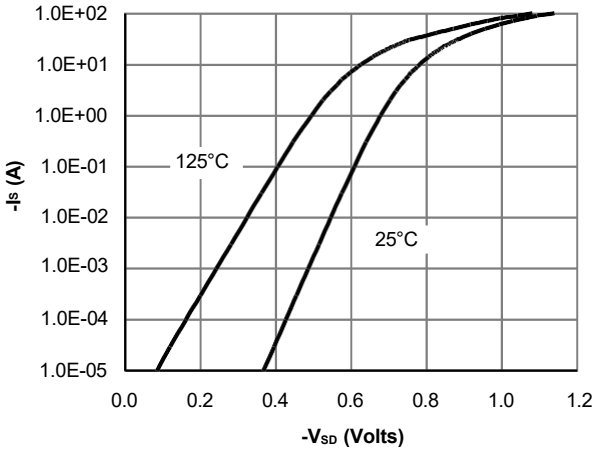



Figure 6: Body-Diode Characteristics (Note E)

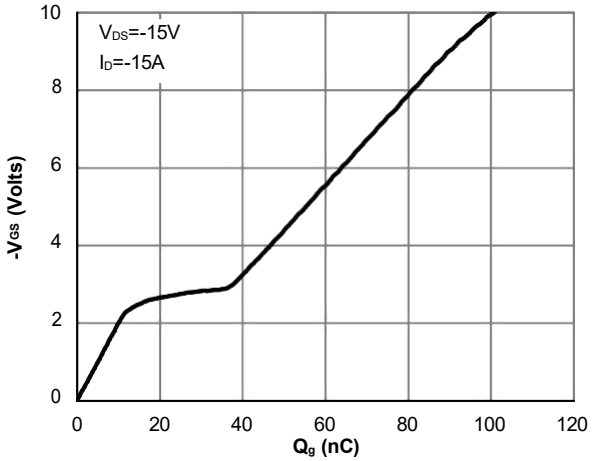



**Figure 7: Gate-Charge Characteristics**

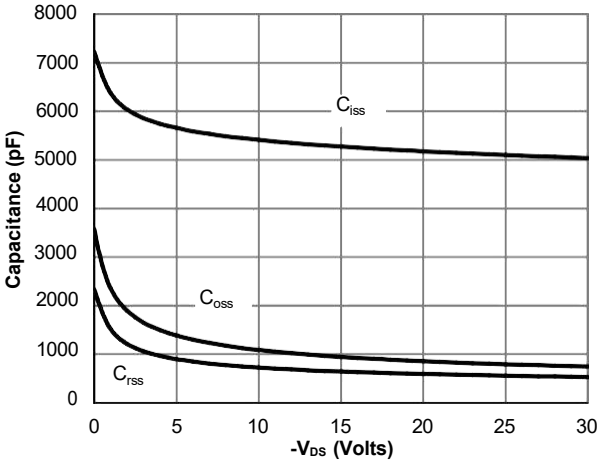



**Figure 8: Capacitance Characteristics**

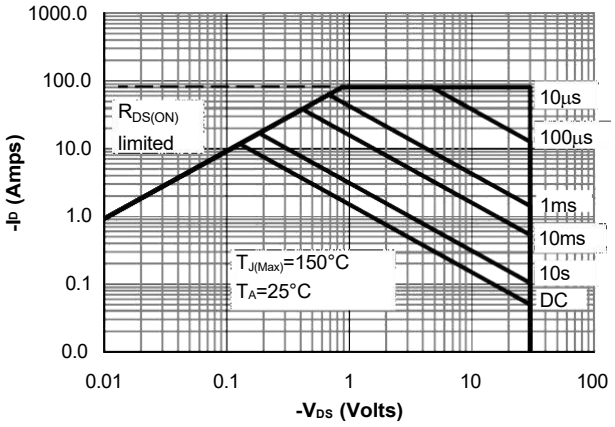



**Figure 9: Maximum Forward Biased. Safe Operating Area (Note F)**

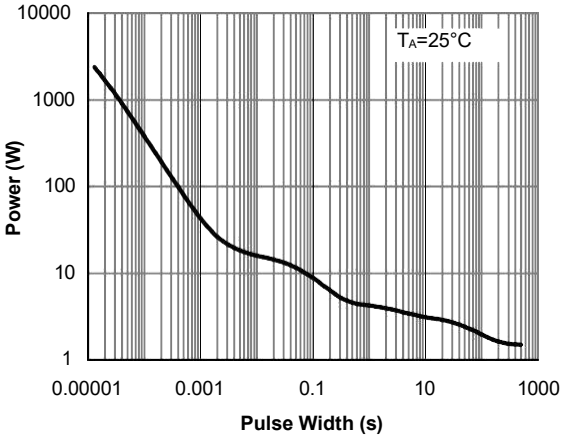



**Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)**

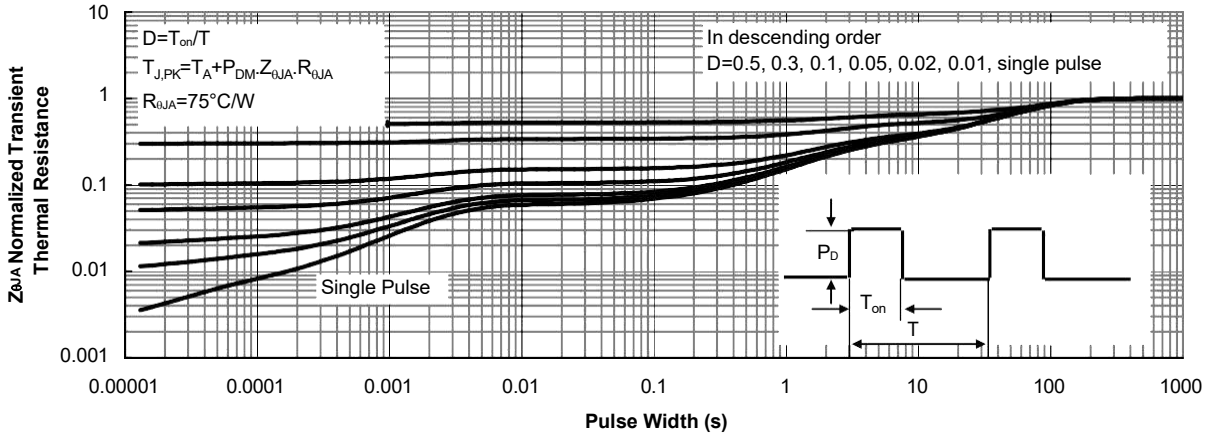
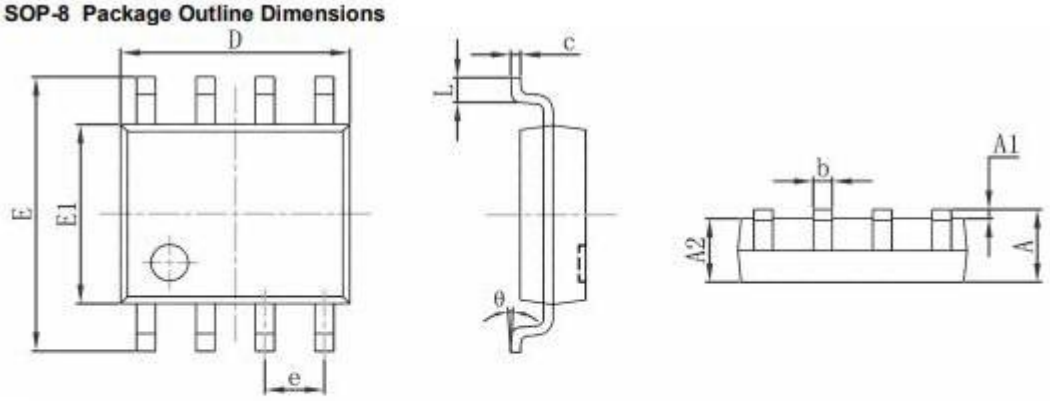


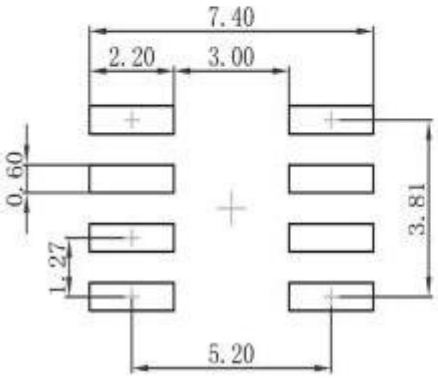

**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**SOP-8 Package Outline Dimensions**




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.007 | 0.010 |
| D | 4.800 | 5.000 | 0.189 | 0.197 |
| e | 1.270(BSC) | | 0.050（BSC） | |
| E | 5.800 | 6.200 | 0.228 | 0.244 |
| E1 | 3.800 | 4.000 | 0.150 | 0.157 |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

**SOP-8 Suggested Pad Layout**




**Note:**

1.Controlling dimension: in millimeters

2.General tolerance: ±0.05mm

3.The pad layout is for reference purposes only