SGM895/SGM896/SGM897/SGM898/SGM899
Ultra-Small, Supervisory Circuits with Adjustable Sequencing

GENERAL DESCRIPTION

The SGM895/SGM896/SGM897/SGM898/SGM899 are ultra-small, low-power and high-accuracy micro-processor supervisory circuits with adjustable sequencing capability. Since the high-impedance detection input pin (IN) with a 0.5V threshold voltage is separated from the power supply, these devices provide great flexibility with adjustable thresholds by using an external resistive divider. Moreover, the delay time can be adjusted by an external capacitor connected to the CDELAY pin. The devices are suitable for some power sequencing, reset sequencing and power-switching equipment.

When the input voltage at IN (V_{IN}) exceeds the V_{TH} threshold voltage (0.5V, TYP) and the ENABLE input is high (or nENABLE is low), the OUT is high (or nOUT is low). When V_{IN} is lower than V_{TL} (0.495V, TYP) or when the ENABLE input is low (or nENABLE is high), the OUT is low (or nOUT is high). The devices all have a capacitor-adjustable input delay time (t_{DELAY}) between V_{IN} greater than V_{TH} and the output assertion. The SGM89_A has a capacitor-adjustable enable output delay time while the SGM89_P has a 350ns (TYP) fixed delay time.

All devices are available in ultra-small Green UTDFN-1.45×1-6AL and TSOT-23-6 packages.

FEATURES

- **High Voltage Threshold Accuracy:**
  - **+25℃: ±1%**
  - **-40℃ to +125℃: ±1.6%**
- **Low Power Consumption: 2.1μA (TYP)**
- **Operating Supply Voltage Range: 1.6V to 5.5V**
- **Capacitor-Adjustable Delay**
- **Enable Input Options:**
  - **Active-High: SGM895 and SGM897**
  - **Active-Low: SGM896, SGM898 and SGM899**
- **Output Options:**
  - **Active-High Push-Pull: SGM895 and SGM899**
  - **Active-Low Push-Pull: SGM896**
  - **Active-High Open-Drain (28V Tolerant): SGM897**
  - **Active-Low Open-Drain (28V Tolerant): SGM898**
- **Available in Ultra-Small Green UTDFN-1.45×1-6AL and TSOT-23-6 Packages**

APPLICATIONS

Portable Equipment
Computers
μC Power Monitoring
Medical Equipment
Intelligent Instruments

TYPICAL APPLICATION

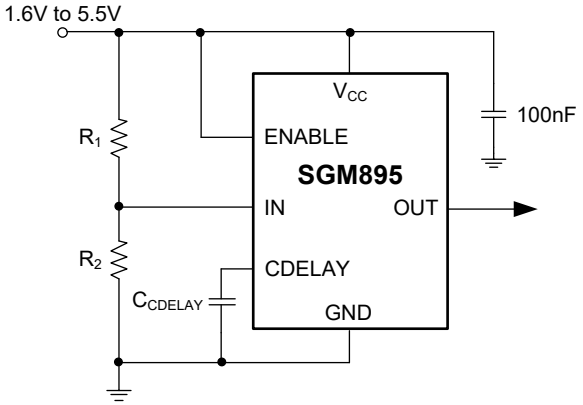


Figure 1. Typical Application Circuit of SGM895

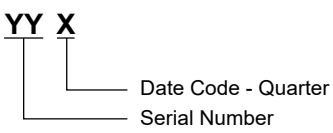
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM895A	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM895AXUDL6G/TR	J9X	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM895AXTN6G/TR	CICXX	Tape and Reel, 3000
SGM895P	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM895PXUDL6G/TR	IAX	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM895PXTN6G/TR	CKFXX	Tape and Reel, 3000
SGM896A	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM896AXUDL6G/TR	QBX	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM896AXTN6G/TR	CL0XX	Tape and Reel, 3000
SGM896P	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM896PXUDL6G/TR	QCX	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM896PXTN6G/TR	CL1XX	Tape and Reel, 3000
SGM897A	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM897AXUDL6G/TR	I8X	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM897AXTN6G/TR	CIDXX	Tape and Reel, 3000
SGM897P	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM897PXUDL6G/TR	IBX	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM897PXTN6G/TR	CL2XX	Tape and Reel, 3000
SGM898A	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM898AXUDL6G/TR	QDX	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM898AXTN6G/TR	CL3XX	Tape and Reel, 3000
SGM898P	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM898PXUDL6G/TR	QEX	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM898PXTN6G/TR	CL4XX	Tape and Reel, 3000
SGM899A	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM899AXUDL6G/TR	I9X	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM899AXTN6G/TR	CIEXX	Tape and Reel, 3000
SGM899P	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM899PXUDL6G/TR	ICX	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM899PXTN6G/TR	CL5XX	Tape and Reel, 3000

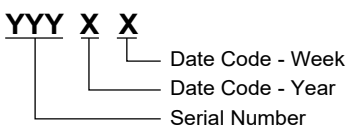
MARKING INFORMATION

NOTE: X = Date Code. XX = Date Code

UTDFN-1.45×1-6AL



TSOT-23-6



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{CC}, ENABLE, nENABLE, IN ..... -0.3V to 6V
OUT, nOUT (Push-Pull) .....-0.3V to V_{CC} + 0.3V
OUT, nOUT (Open-Drain) ..... -0.3V to 30V
CDELAY.....-0.3V to V_{CC} + 0.3V
Output Current (All Pins).....±20mA
Package Thermal Resistance
UTDFN-1.45×1-6AL, θ_{JA} ..... 233.3℃/W
UTDFN-1.45×1-6AL, θ_{JB} ..... 121.5℃/W
UTDFN-1.45×1-6AL, θ_{JC} ..... 173.8℃/W
TSOT-23-6, θ_{JA} ..... 153.8℃/W
TSOT-23-6, θ_{JB} ..... 41.1℃/W
TSOT-23-6, θ_{JC} ..... 93℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....±4000V
CDM .....±1000V

RECOMMENDED OPERATING CONDITIONS

Operating Junction Temperature Range .....-40℃ to +125℃
Operating Ambient Temperature Range.....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

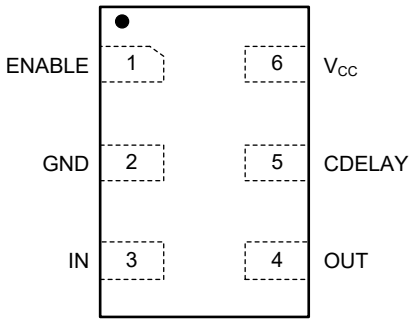
SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

SELECTOR GUIDE

DEVICE	ENABLE INPUT	OUTPUT	INPUT DELAY TIME	ENABLE DELAY TIME
SGM895A	Active-High	Active-High, Push-Pull	Capacitor-Adjustable	Capacitor-Adjustable
SGM895P	Active-High	Active-High, Push-Pull	Capacitor-Adjustable	350ns Delay
SGM896A	Active-Low	Active-Low, Push-Pull	Capacitor-Adjustable	Capacitor-Adjustable
SGM896P	Active-Low	Active-Low, Push-Pull	Capacitor-Adjustable	350ns Delay
SGM897A	Active-High	Active-High, Open-Drain	Capacitor-Adjustable	Capacitor-Adjustable
SGM897P	Active-High	Active-High, Open-Drain	Capacitor-Adjustable	350ns Delay
SGM898A	Active-Low	Active-Low, Open-Drain	Capacitor-Adjustable	Capacitor-Adjustable
SGM898P	Active-Low	Active-Low, Open-Drain	Capacitor-Adjustable	350ns Delay
SGM899A	Active-Low	Active-High, Push-Pull	Capacitor-Adjustable	Capacitor-Adjustable
SGM899P	Active-Low	Active-High, Push-Pull	Capacitor-Adjustable	350ns Delay

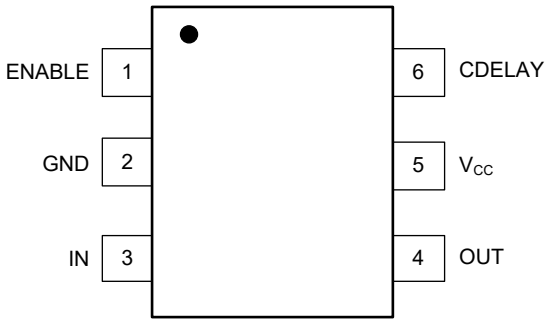
PIN CONFIGURATIONS

SGM895/SGM897 (TOP VIEW)



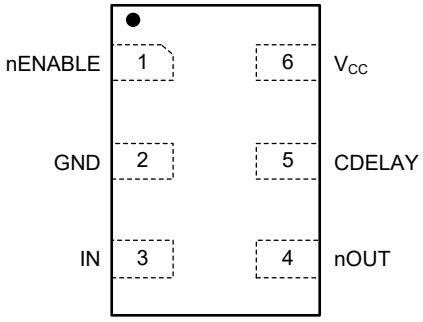
UTDFN-1.45×1-6AL

SGM895/SGM897 (TOP VIEW)



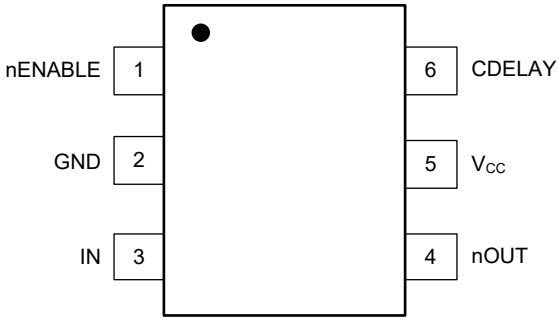
TSOT-23-6

SGM896/SGM898 (TOP VIEW)



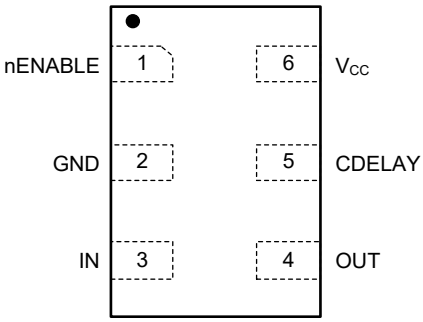
UTDFN-1.45×1-6AL

SGM896/SGM898 (TOP VIEW)



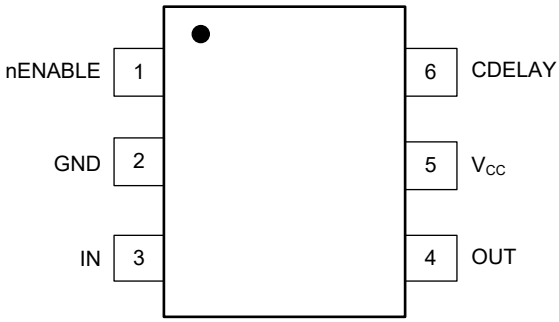
TSOT-23-6

SGM899 (TOP VIEW)



UTDFN-1.45×1-6AL

SGM899 (TOP VIEW)



TSOT-23-6

PIN DESCRIPTION

PIN						NAME	FUNCTION
SGM895/SGM897		SGM896/SGM898		SGM899			
UTDFN-1.45×1-6AL	TSOT-23-6	UTDFN-1.45×1-6AL	TSOT-23-6	UTDFN-1.45×1-6AL	TSOT-23-6		
1	1	—	—	—	—	ENABLE	Active-High Enable Input Pin. If ENABLE is set to low, the output will immediately enter into false state (OUT is low or nOUT is high) regardless of V_{IN}. If V_{IN} exceeds V_{TH}, the output will enter into true state (OUT is high or nOUT is low) by setting ENABLE high after the enable output delay time (adjustable delay time for the SGM89_A and 350ns delay time for the SGM89_P).
—	—	1	1	1	1	nENABLE	Active-Low Enable Input Pin. If nENABLE is set to high, the output will immediately enter into false state (OUT is low or nOUT is high) regardless of V_{IN}. If V_{IN} exceeds V_{TH}, the output will enter into true state (OUT is high or nOUT is low) by setting nENABLE low after the enable output delay time (adjustable delay time for the SGM89_A and 350ns delay time for the SGM89_P).
2	2	2	2	2	2	GND	Ground.
3	3	3	3	3	3	IN	High-Impedance Detection Input. The detection threshold can be adjusted by an external resistive divider connected to IN pin. The output state changes when V_{IN} exceeds V_{TH} (0.5V, TYP) or when V_{IN} drops below V_{TL} (0.495V, TYP).
4	4	—	—	4	4	OUT	Active-High, Push-Pull (SGM895/SGM899) or Open-Drain (SGM897) Output Pin. And the open-drain output needs a pull-up resistor. The OUT is logic low when the enable input is in the false state (ENABLE is low or nENABLE is high) or when V_{IN} drops below V_{TL} (0.495V, TYP). The OUT is logic high after the CDELAY adjustable delay period when the enable input is in the true state (ENABLE is high or nENABLE is low) and V_{IN} exceeds V_{TH}.
—	—	4	4	—	—	nOUT	Active-Low, Push-Pull (SGM896) or Open-Drain (SGM898) Output Pin. And the open-drain output needs a pull-up resistor. The nOUT is logic high when the enable input is in the false state (ENABLE is low or nENABLE is high) or when V_{IN} drops below V_{TL} (0.495V, TYP). The nOUT is logic low after the CDELAY adjustable delay period when the enable input is in the true state (ENABLE is high or nENABLE is low) and V_{IN} exceeds V_{TH}.
5	6	5	6	5	6	CDELAY	Capacitor-Adjustable Delay. The delay time can be set by an external capacitor (C_{CDELAY}) between CDELAY and GND. t_{DELAY} (ms) = 3.95 × C_{CDELAY} (nF) + 0.048ms There is a 50μs (TYP) fixed delay for the output deasserting when V_{IN} falls below V_{TL}.
6	5	6	5	6	5	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.6V to 5.5V, Full = -40℃ to +125℃, typical values are at V_{CC} = 3.3V and T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Supply							
Operating Voltage Range	V_{CC}		Full	1.6		5.5	V
Under-Voltage Lockout (1)	V_{UVLO}	V_{CC} falling	Full	1.31		1.49	V
V_{CC} Supply Current	I_{CC}		Full		2.1	7.8	μA
IN							
Rising Threshold Voltage	V_{TH}	V_{IN} rising, 1.6V < V_{CC} < 5.5V	+25℃	0.495	0.500	0.505	V
			Full	0.492	0.500	0.508	
Falling Threshold Voltage	V_{TL}	V_{IN} falling, 1.6V < V_{CC} < 5.5V	+25℃	0.489	0.495	0.501	V
			Full	0.487	0.495	0.503	
Hysteresis	V_{HYST}	V_{IN} falling	Full		5		mV
Input Current	I_{IN}	V_{IN} = 0V or V_{CC}	Full	-20		20	nA
CDELAY							
Delay Charge Current	I_{CD}		Full	210	253	290	nA
Delay Threshold	V_{TCD}	CDELAY rising	Full	0.96	1.00	1.04	V
CDELAY Pull-Down Resistance	R_{CDELAY}		Full		120	350	Ω
ENABLE/nENABLE							
Input Low Voltage	V_{IL}		Full			0.4	V
Input High Voltage	V_{IH}		Full	1.4			V
Input Leakage Current	I_{LEAK}	ENABLE, nENABLE = V_{CC} or GND	Full	-50		50	nA
OUT/nOUT							
Output Low Voltage (Open-Drain or Push-Pull)	V_{OL}	V_{CC} ≥ 1.2V, I_{SINK} = 90μA, SGM895/SGM897/SGM899 only	Full			0.3	V
		V_{CC} ≥ 2.25V, I_{SINK} = 0.5mA	Full			0.3	
		V_{CC} ≥ 4.5V, I_{SINK} = 1mA	Full			0.4	
Output High Voltage (Push-Pull)	V_{OH}	V_{CC} ≥ 2.25V, I_{SOURCE} = 500μA	Full	0.8 × V_{CC}			V
		V_{CC} ≥ 4.5V, I_{SOURCE} = 800μA	Full	0.8 × V_{CC}			
Output Open-Drain Leakage Current	I_{LKG}	Output high impedance, V_{OUT} = 28V	Full			1	μA
Timing							
IN to OUT/nOUT Propagation Delay	t_{DELAY}	V_{IN} rising, C_{CDELAY} = 0nF	Full		48		μs
		V_{IN} rising, C_{CDELAY} = 47nF	Full		185		ms
	t_{DL}	V_{IN} falling	Full		50		μs
ENABLE/nENABLE Minimum Input Pulse Width	t_{PW}		Full	1.1			μs
ENABLE/nENABLE Glitch Rejection			Full		210		ns
ENABLE/nENABLE to OUT/nOUT Delay	t_{OFF}	From device enabled to device disabled	Full		350		ns
ENABLE/nENABLE to OUT/nOUT Delay	t_{PROPP}	From device disabled to device enabled (SGM89_P)	Full		350		ns
	t_{PROPA}	From device disabled to device enabled (SGM89_A), C_{CDELAY} = 0nF	Full		30		μs
		From device disabled to device enabled (SGM89_A), C_{CDELAY} = 47nF	Full		185		ms

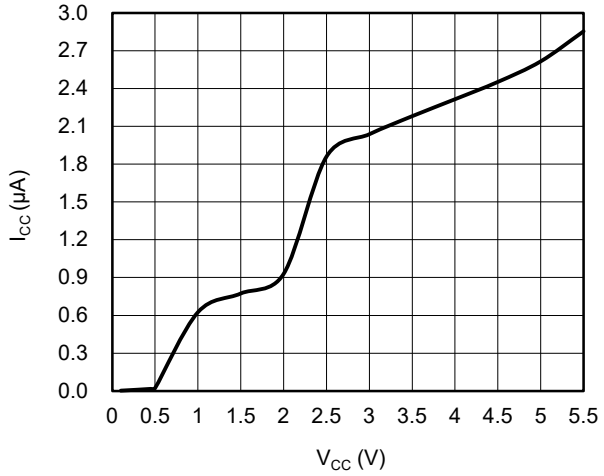
NOTES:

1. If V_{CC} is lower than V_{UVLO}, the OUT will be low (or nOUT will be high).
2. The output state is not guaranteed if V_{CC} is lower than 1.2V.
3. In the initial power-on phase, V_{CC} must be greater than 1.6V and no less than 2ms to ensure correct output state.

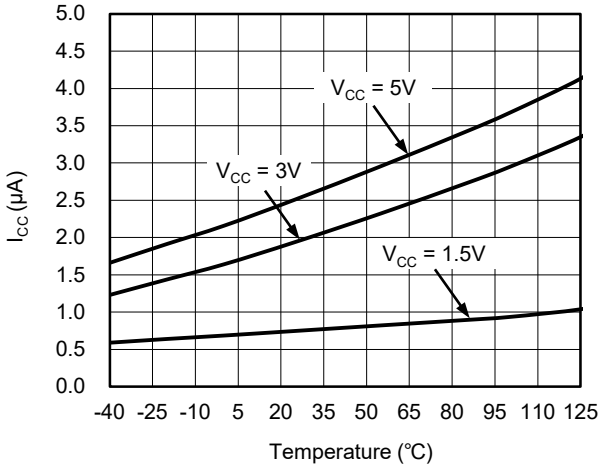
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V and T_J = +25℃, unless otherwise noted.

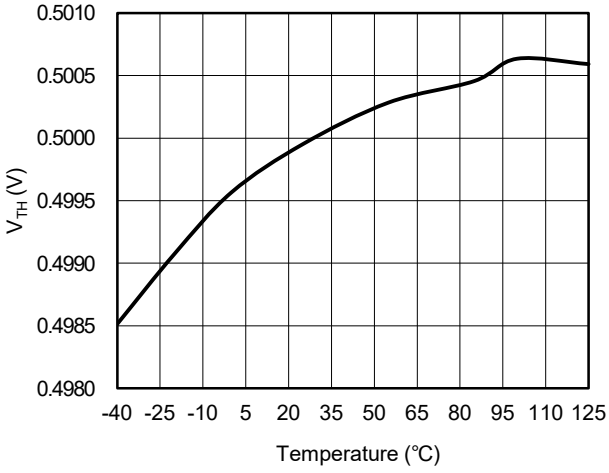
Supply Current vs. Supply Voltage



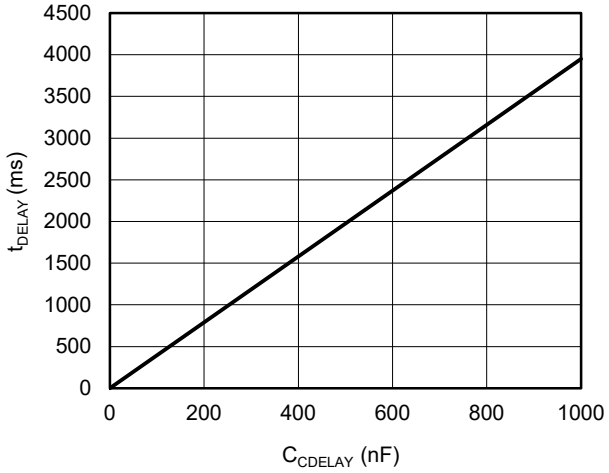
Supply Current vs. Temperature



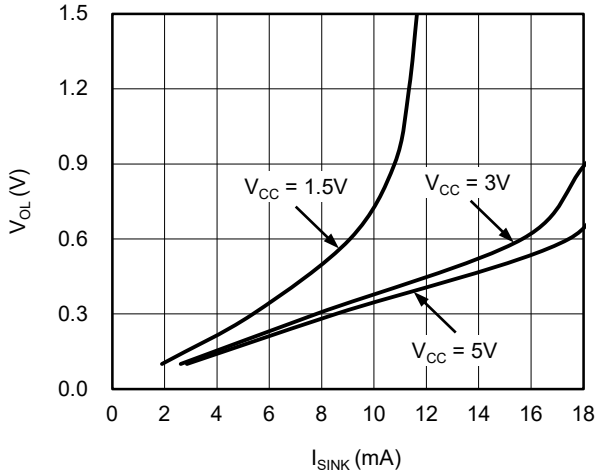
IN Threshold vs. Temperature



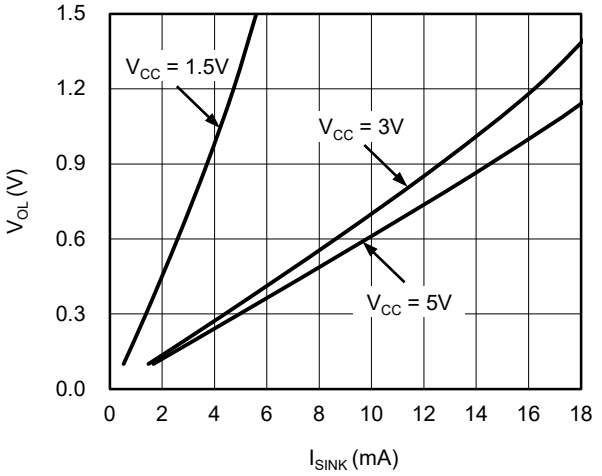
OUT Delay vs. C_{CDELAY}



Output Low Voltage vs. Sink Current
(SGM895/SGM896/SGM899)



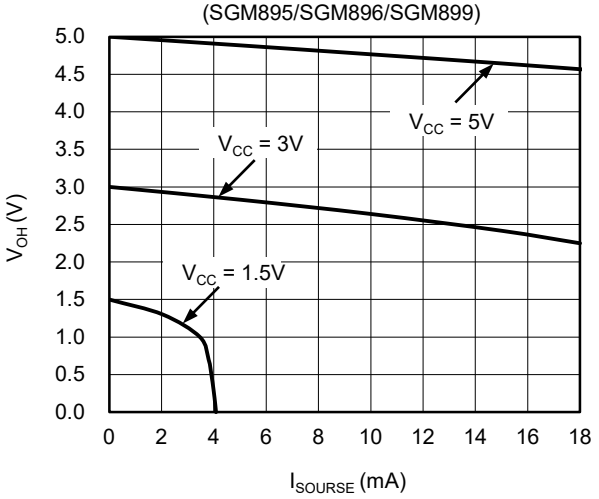
Output Low Voltage vs. Sink Current
(SGM897/SGM898)



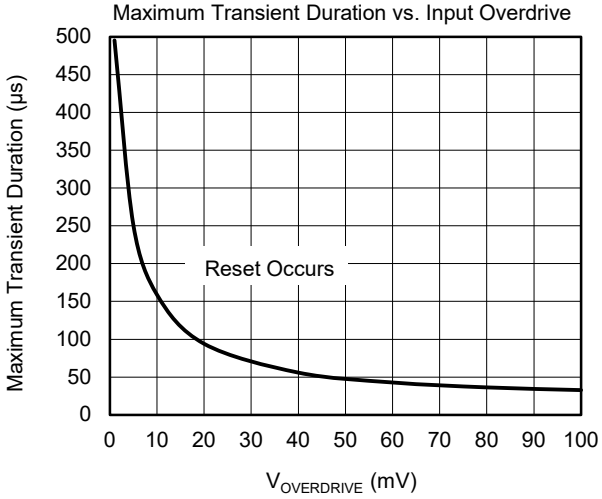
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{CC} = 3.3V and T_J = +25℃, unless otherwise noted.

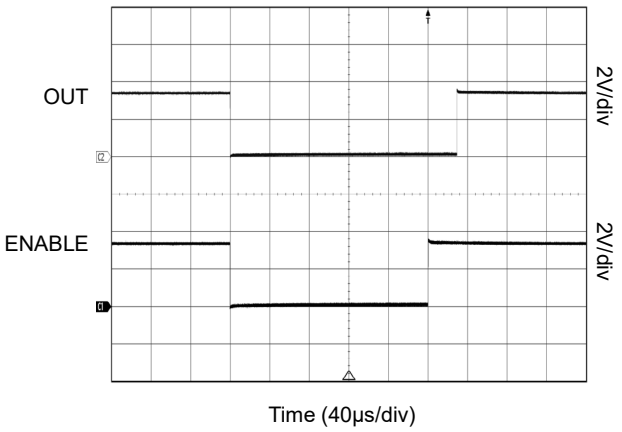
Output High Voltage vs. Source Current
(SGM895/SGM896/SGM899)



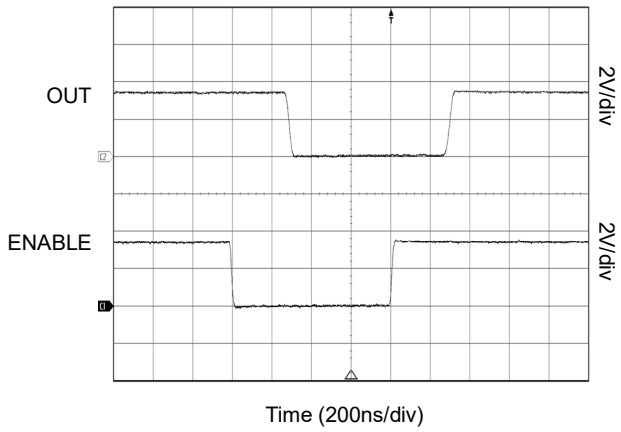
Maximum Transient Duration vs. Input Overdrive



Enable Turn-On/Off Delay (SGM895A)



Enable Turn-On/Off Delay (SGM895P)



FUNCTIONAL BLOCK DIAGRAM

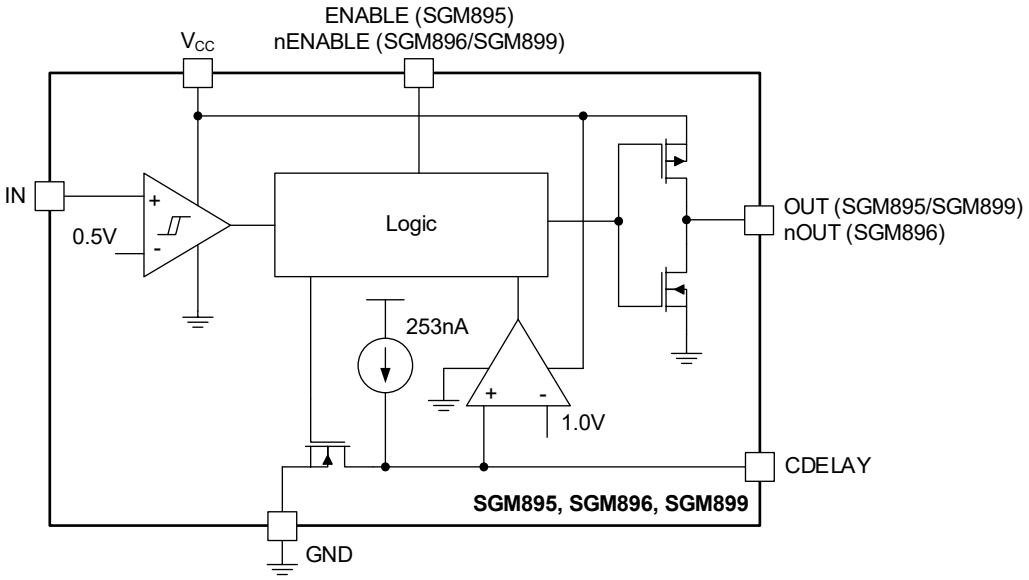


Figure 2. SGM895/SGM896/SGM899 Block Diagram

DETAILED DESCRIPTION

The SGM895/SGM896/SGM897/SGM898/SGM899 are low-power and high-accuracy microprocessor supervisory circuits with adjustable sequencing capability.

When V_{IN} exceeds V_{TH}, set enable input to assert or deassert output. After the enable input is asserted, the output asserts with the CDELAY adjusted delay period (SGM89_A) or with a 350ns fixed propagation delay (SGM89_P). The output pin states of all devices are based on various V_{IN} and ebable input shown in Table 1, 2, and 3.

Table 1. SGM895/SGM897 Output

IN Pin	ENABLE Pin	OUT Pin
$V_{IN} < V_{TH}$	Low	Low
$V_{IN} < V_{TH}$	High	Low
$V_{IN} > V_{TH}$	Low	Low
$V_{IN} > V_{TH}$	High	OUT = V_{CC} (SGM895)
		OUT = high-impedance (SGM897)

Table 2. SGM896/SGM898 Output

IN Pin	nENABLE Pin	nOUT Pin
$V_{IN} < V_{TH}$	Low	nOUT = V_{CC} (SGM896)
		nOUT = high-impedance (SGM898)
$V_{IN} < V_{TH}$	High	nOUT = V_{CC} (SGM896)
		nOUT = high-impedance (SGM898)
$V_{IN} > V_{TH}$	Low	Low
$V_{IN} > V_{TH}$	High	nOUT = V_{CC} (SGM896)
		nOUT = high-impedance (SGM898)

Table 3. SGM899 Output

IN Pin	nENABLE Pin	OUT Pin
$V_{IN} < V_{TH}$	Low	Low
$V_{IN} < V_{TH}$	High	Low
$V_{IN} > V_{TH}$	Low	High
$V_{IN} > V_{TH}$	High	Low

Supply Voltage Input (V_{CC})

The V_{CC} voltage range is from 1.6V to 5.5V, When V_{CC} falls below V_{UVLO}, the device deasserts. However, the output state is not guaranteed if V_{CC} is lower than 1.2V. For noisy systems, it is recommended to place a 100nF bypass capacitor close to the V_{CC} pin. A 100kΩ pull-down resistor should be connected to ground for push-pull output device to ensure correct logic low state.

Detection Input (IN)

IN pin is used to monitor external voltage, with low leakage current, and larger-value resistive divider will not cause significant bias voltage. The rising threshold V_{TH} is 0.5V and falling threshold V_{TL} is 0.495V (V_{HYST} = 5mV). Refer to Table 1, 2 and 3. With asserted ENABLE/nENABLE pin, when V_{IN} is above V_{TH}, OUT goes high (nOUT goes low) after a t_{DELAY} period. When V_{IN} falls below 0.495V, OUT goes low (nOUT goes high) after a delay time of 50μs.

Adjustable Delay (CDELAY)

An external capacitor connected between CDELAY pin and GND is used to adjust delay time. With asserted ENABLE/nENABLE pin, when V_{IN} is above V_{TH}, the internal current I_{CD} is 253nA (TYP). The current source starts charging capacitor to 1V, OUT goes high (nOUT goes low), and the capacitor is immediately discharged to ensure next t_{DELAY} period. Adjust the delay time according to the equation:

$$t_{DELAY}\,(ms) = 3.95 \times C_{CDELAY}\,(nF) + 0.048ms \quad (1)$$

where C_{CDELAY} is the external capacitor from CDELAY to GND.

Under the condition of $V_{IN} > V_{TH}$, the output state depends on the state of ENABLE (nENABLE). For devices SGM89_A, the delay time can be adjusted by external capacitor. For devices SGM89_P, the propagation delay is fixed (t_{OFF} = 350ns). Timing diagrams of all devices are shown in Figure 3 to Figure 8.

DETAILED DESCRIPTION (continued)

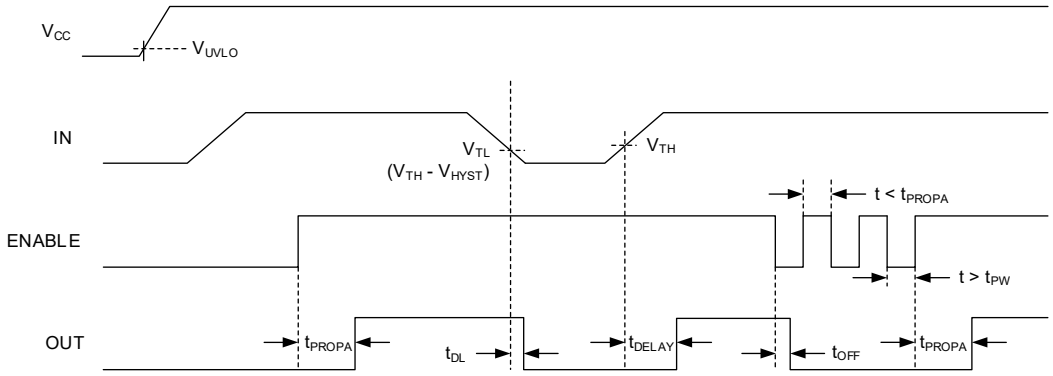


Figure 3. SGM895A/SGM897A Timing Diagram

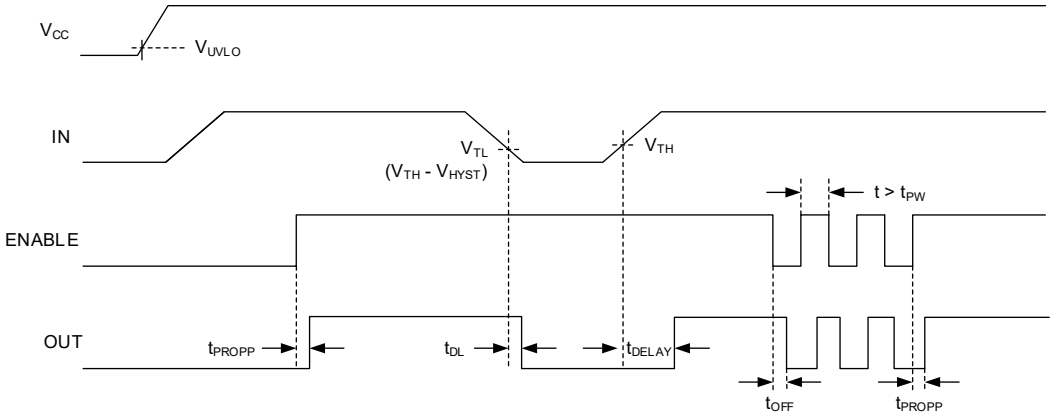


Figure 4. SGM895P/SGM897P Timing Diagram

DETAILED DESCRIPTION (continued)

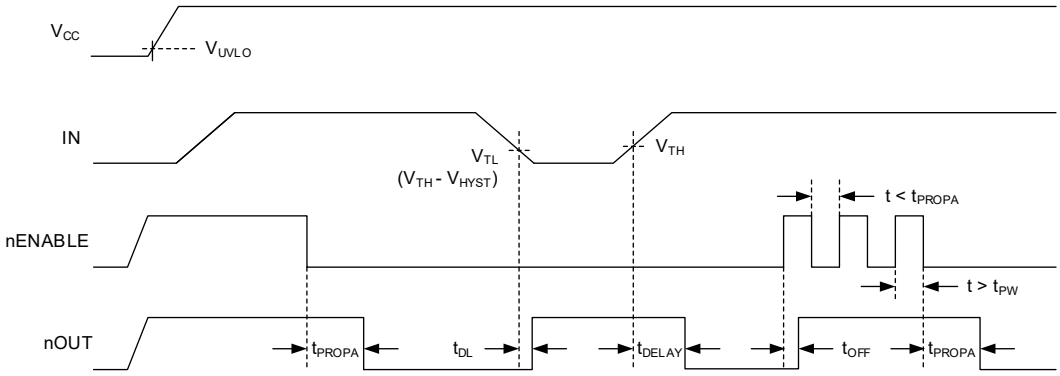


Figure 5. SGM896A/SGM898A Timing Diagram

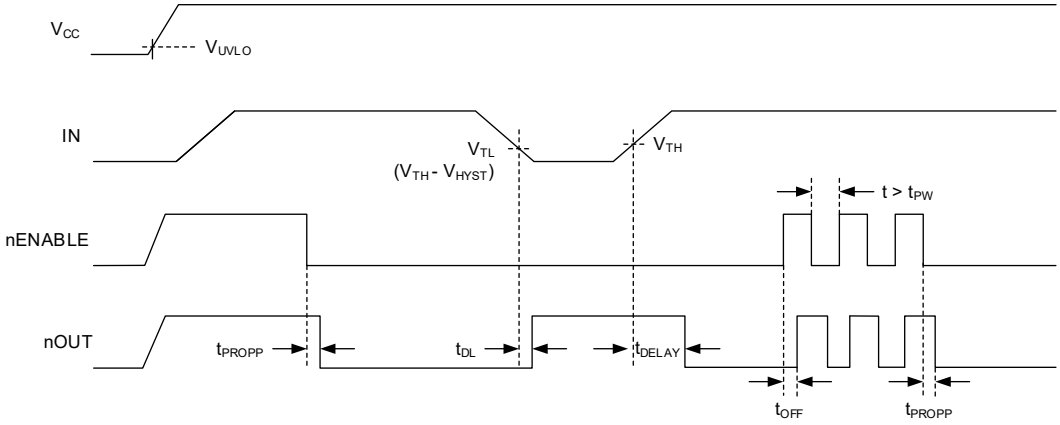


Figure 6. SGM896P/SGM898P Timing Diagram

DETAILED DESCRIPTION (continued)

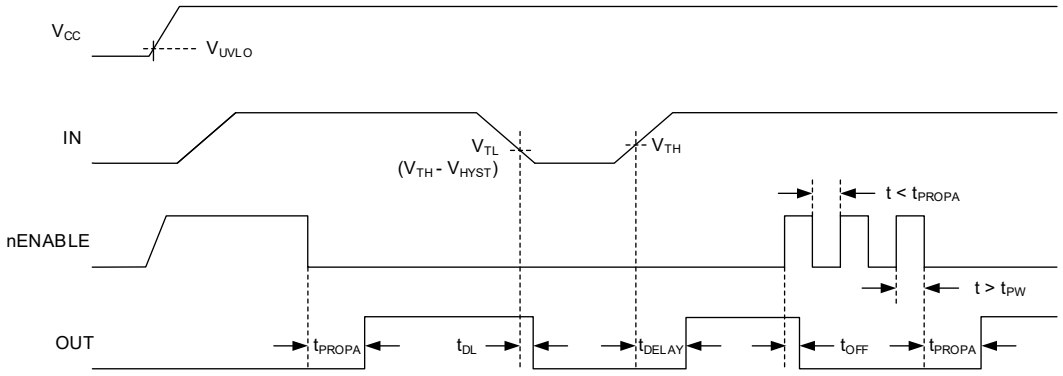


Figure 7. SGM899A Timing Diagram

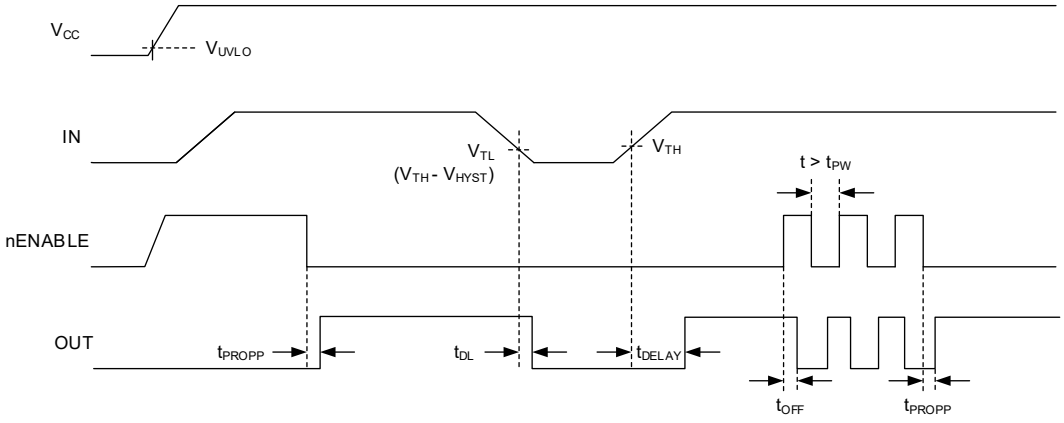


Figure 8. SGM899P Timing Diagram

Enable Input (ENABLE or nENABLE)

When V_{IN} is above V_{TH}, two types enable input ENABLE/nENABLE determine the output state. The SGM895/SGM897 are active-high enable input and SGM896/SGM898/SGM899 are active-low enable input. For devices SGM89_A, the delay time can be adjusted by an external capacitor. For devices SGM89_P, the propagation delay is fixed of 350ns.

The maximal logic-low threshold V_{IL} is 0.4V and minimal logic-high threshold V_{IH} is 1.4V.

Output (OUT/nOUT)

There are four selectable output options. The SGM895/SGM899 are active-high, push-pull output. the SGM897 is active-high, open-drain output. the SGM896 is active-low, push-pull output. And the SGM898 is active-low, open-drain output. The reference voltage of push-pull outputs are V_{CC}, and the pull-up reference voltage of open-drain outputs are up to 28V.

APPLICATION INFORMATION

Input Threshold

IN pin can be used to monitor external voltage through resistive divider. With low leakage current, larger-value resistors reduce current consumption without significant bias voltage. According to typical application circuit in Figure 1, for a given R_2, R_1 can be calculated based on desired detection voltage through the following equation:

$$R_1 = R_2 \times \left[\frac{V_{MONITOR}}{V_{TH}} - 1 \right] \quad (2)$$

$V_{MONITOR}$ is the desired detection voltage. V_{TH} is the detector input threshold of 0.5V.

Pull-Up Resistor Values (SGM897/SGM898)

To ensure proper output logic-low voltage, pull-up resistor value should be limited. Refer to Electrical Characteristics section, if V_{CC} is 2.25V, the pull-up voltage is 28V, and for an output voltage lower than 0.3V, the pull-up resistor should be limited to 56kΩ. if V_{CC} is 4.5V and the pull-up voltage is 28V, and for an output voltage lower than 0.4V, the pull-up resistor should be limited to 28kΩ. The sink current ability dependents on the VCC supply voltage.

Typical Application Circuits

Three types typical applications are shown in.Figure 9, 10 and 11. Figure 9 shows that the SGM897 is used as an over-voltage protection circuit by a P-channel MOSFET. Figure 10 shows that the SGM895 is used as a low-voltage sequencing with an N-channel MOSFET. Figure 11 shows that the SGM895 is used in a multiple-output sequencing circuit.

Using an N-Channel Device for Sequencing

In higher power applications, the power loss of N-channel MOSFET can be reduced due to its lower on-resistance. However, it requires a sufficient positive V_{GS} voltage to fully turn on. Figure 10 shows the switch sequencing circuit by using an N-channel MOSFET. Up to 28V pull-up voltage provides sufficient V_{GS} voltage for higher voltage applications.

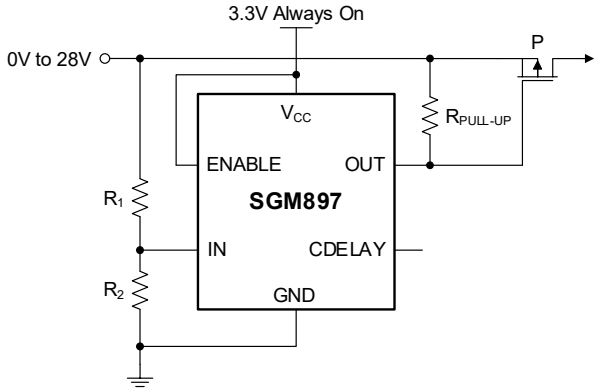


Figure 9. Over-Voltage Protection

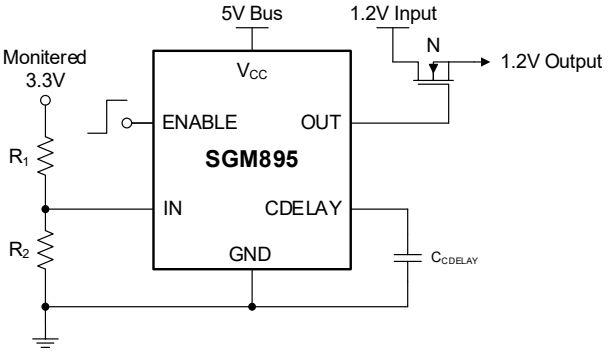


Figure 10. Low-Voltage Sequencing Using an N-Channel MOSFET

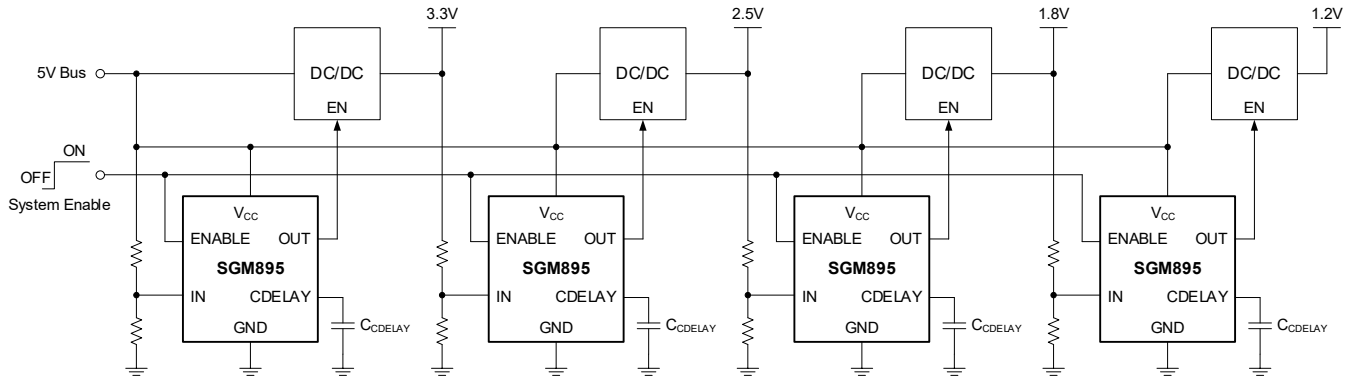


Figure 11. Multiple-Output Sequencing

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

MAY 2026 – REV.A.4 to REV.B	Page
Updated Absolute Maximum Ratings section	3

MAY 2023 – REV.A.3 to REV.A.4	Page
Changed Electrical Characteristics section	6
Updated Detail Description section	10-13
Updated Application Information section	14, 15

OCTOBER 2021 – REV.A.2 to REV.A.3	Page
Updated Package Outline Dimensions section	10, 11

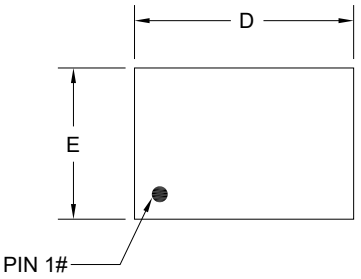
OCTOBER 2021 – REV.A.1 to REV.A.2	Page
Updated UTDFN-1.45×1-6AL Package	4, 16

JULY 2021 – REV.A to REV.A.1	Page
Changed Package/Ordering Information section	2

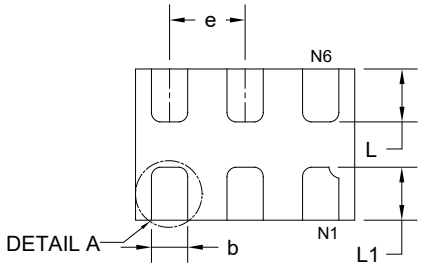
Changes from Original to REV.A (JULY 2020)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

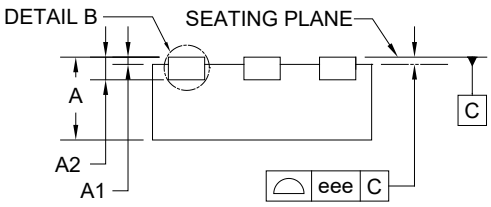
UTDFN-1.45×1-6AL



TOP VIEW



BOTTOM VIEW



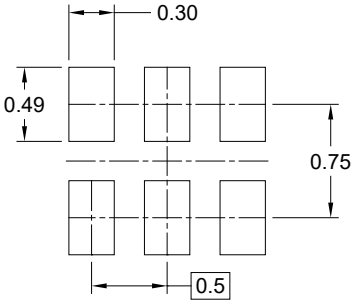
SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



DETAIL B
ALTERNATE CONSTRUCTION



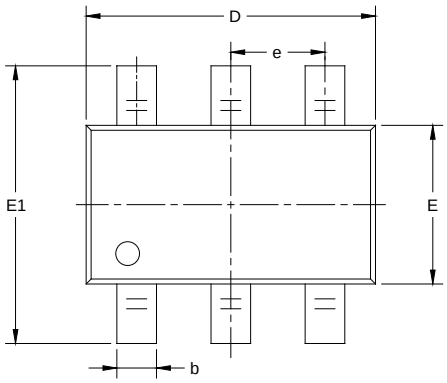
RECOMMENDED LAND PATTERN (Unit: mm)

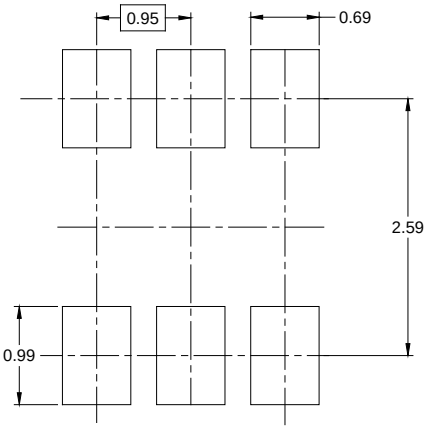
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.450	-	0.600
A1	-0.004	-	0.050
A2	0.150 REF		
b	0.150	-	0.300
D	1.374	-	1.526
E	0.924	-	1.076
e	0.500 BSC		
L	0.250	-	0.450
L1	0.250	-	0.500
L2	0.000	-	0.100
eee	0.050		

NOTE: This drawing is subject to change without notice.

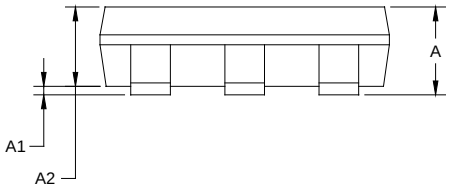
PACKAGE OUTLINE DIMENSIONS

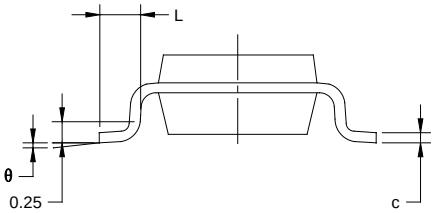
TSOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)





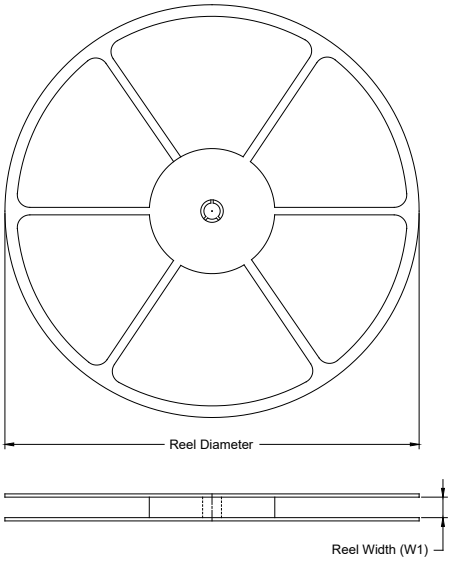
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.100
A1	0.000	-	0.100
A2	0.700	-	1.000
b	0.300	-	0.500
c	0.080	-	0.200
D	2.820	-	3.050
E	1.550	-	1.700
E1	2.650	-	2.950
e	0.950 BSC		
L	0.300	-	0.600
θ	0°	-	8°

NOTES:

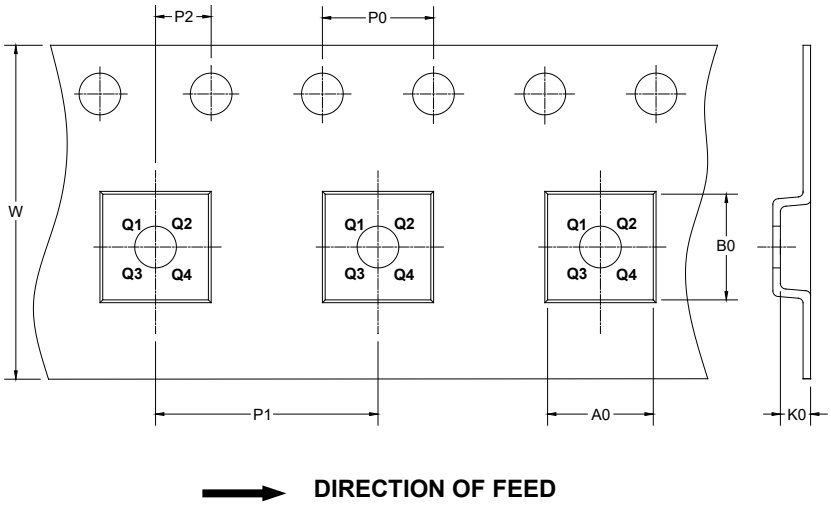
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



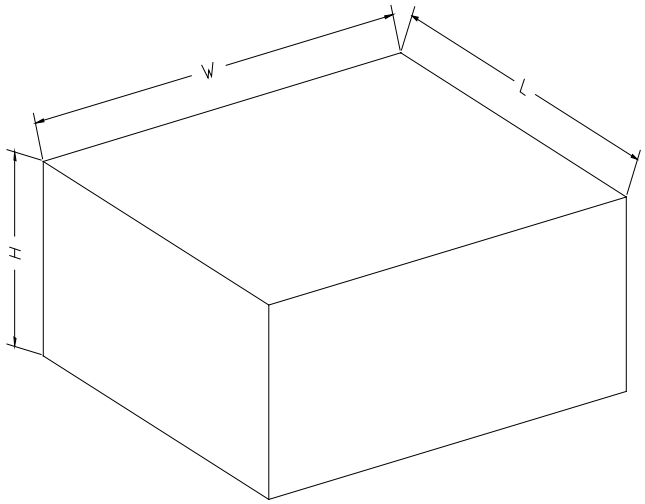
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTDFN-1.45×1-6AL	7″	9.5	1.15	1.60	0.75	4.0	4.0	2.0	8.0	Q1
TSOT-23-6	7″	9.5	3.20	3.10	1.10	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002