SGM865
Quad UV/OV Positive/Negative Voltage Supervisor

GENERAL DESCRIPTION

The SGM865 is a quad voltage monitoring IC designed for supervising multiple power rails in various applications. Each monitored rail features two input pins, VHx and VLx (x = 1, 2, 3, 4), enabling simultaneous detection of over-voltage (OV) and under-voltage (UV) conditions. A shared active-low output pin, nUV/nOV, indicates the status of all monitored rails.

The SGM865 provides a 1V buffered reference output (REF), which can be used as an offset when detecting negative voltages. Additionally, the three-state SEL pin allows configuration of the polarity for VH3/VL3 and VH4/VL4, supporting both positive and negative supply monitoring.

The device integrates an internal shunt regulator, allowing it to operate in high-voltage systems. To protect the VCC pin, a resistor must be added between the main supply rail and VCC, limiting current flow to no more than 10mA. If the supply voltage exceeds 5.5V, the internal shunt regulator will automatically regulate the VCC voltage.

The SGM865 offers two models. The SGM865A/C latches the nOV pin under OV condition by pulling down the nLATCH pin and can be cleared by toggling the nLATCH pin. The SGM865B/D can pull high the nOV and nUV pins with the DIS pin no matter what the monitored signal voltage is.

The SGM865 is available in Green SSOP-16 and TQFN-3×3-16L packages. It operates over the junction temperature range of -40℃ to +125℃.

FEATURES

- **Quad UV/OV Positive/Negative Supervisor**
- **Supervise Up to 2 Negative Rails**
- **High Threshold Accuracy: ±2%**
- **Low Supply Current: 35μA (TYP)**
- **Adjustable UV and OV Input Thresholds**
- **Adjustable Reset Timeout with Disable Option**
- **1V Buffered Reference Output**
- **Open-Drain OV/UV Reset Outputs**
- **Guaranteed Outputs Valid at V_{CC} = 1V**
- **Glitch Immunity**
- **Available in Green SSOP-16 and TQFN-3×3-16L Packages**

APPLICATIONS

Communication Equipment
Enterprise Servers
FPGA/DSP Voltage Monitoring
Medical Equipment

TYPICAL APPLICATION

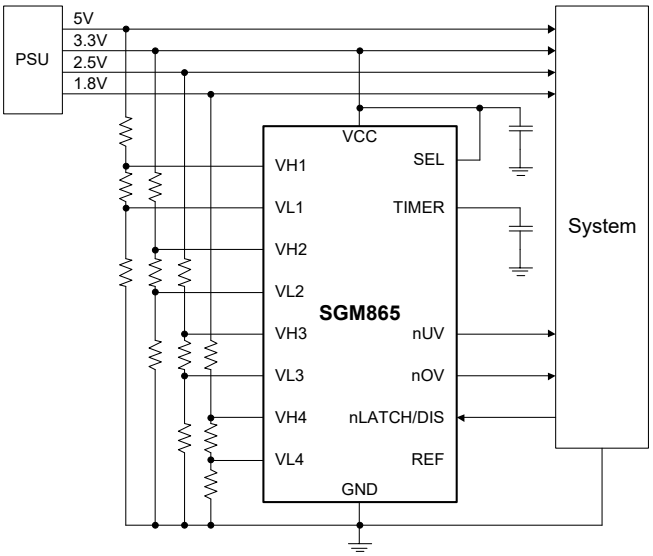


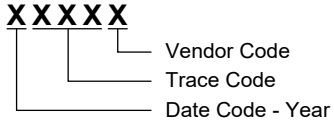
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM865A	SSOP-16	-40℃ to +125℃	SGM865AXQS16G/TR	SGM865A XQS16 XXXXX	Tape and Reel, 4000
SGM865B	SSOP-16	-40℃ to +125℃	SGM865BXQS16G/TR	SGM865B XQS16 XXXXX	Tape and Reel, 4000
SGM865C	TQFN-3×3-16L	-40℃ to +125℃	SGM865CXTQ16G/TR	865CTQ XXXXX	Tape and Reel, 4000
SGM865D	TQFN-3×3-16L	-40℃ to +125℃	SGM865DXTQ16G/TR	865DTQ XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... -0.3V to V_{SHUNT}
nUV, nOV Voltage ..... -0.3V to 16V
TIMER, SEL Voltage ..... -0.3V to V_{CC} + 0.3V
VLx, VHx, nLATCH, DIS Voltage ..... -0.3V to 7V
Supply Current, I_{CC} 10mA
Reference Load Current, I_{REF} ..... ±1mA
nUV, nOV Current, I_{nUV}, I_{nOV} 10mA
Package Thermal Resistance
SSOP-16, θ_{JA} ..... 91.3℃/W
SSOP-16, θ_{JB} ..... 52.7℃/W
SSOP-16, θ_{JC} ..... 55.5℃/W
TQFN-3×3-16L, θ_{JA} ..... 39.1℃/W
TQFN-3×3-16L, θ_{JB} ..... 18.3℃/W
TQFN-3×3-16L, $\theta_{JC\ (TOP)}$ ..... 47.7℃/W
TQFN-3×3-16L, $\theta_{JC\ (BOT)}$ ..... 7.5℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

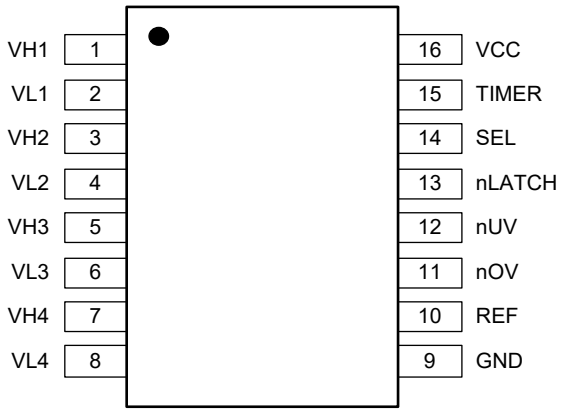
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

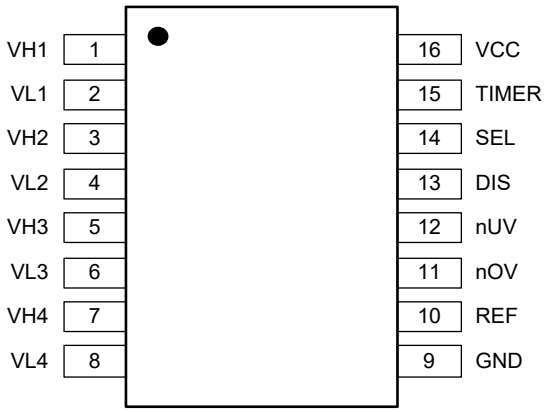
PIN CONFIGURATIONS

SGM865A (TOP VIEW)



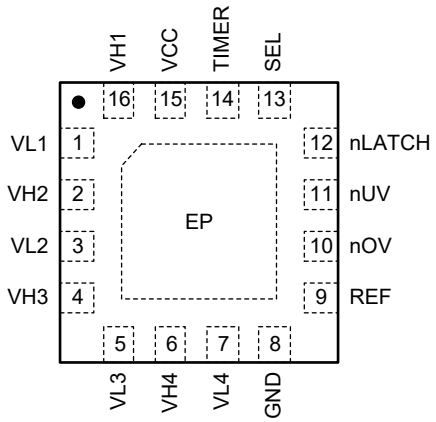
SSOP-16

SGM865B (TOP VIEW)



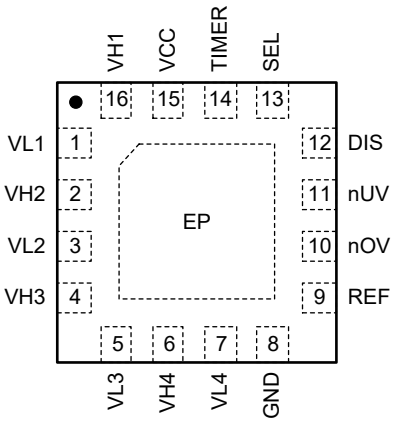
SSOP-16

SGM865C (TOP VIEW)



TQFN-3×3-16L

SGM865D (TOP VIEW)



TQFN-3×3-16L

PIN DESCRIPTION

PIN		NAME	FUNCTION
SSOP	TQFN		
1	16	VH1	UV Detector Input 1. If the VH1 voltage drops below 0.5V, an under-voltage condition is detected. Connect it to VCC if not used.
2	1	VL1	OV Detector Input 1. If the VL1 voltage rises above 0.5V, an over-voltage condition is detected. Connect it to GND if not used.
3	2	VH2	UV Detector Input 2. If the VH2 voltage drops below 0.5V, an under-voltage condition is detected. Connect it to VCC if not used.
4	3	VL2	OV Detector Input 2. If the VL2 voltage rises above 0.5V, an over-voltage condition is detected. Connect it to GND if not used.
5	4	VH3	UV Detector Input 3. The polarity of this input is determined by the state of the SEL pin as shown in Table 1. When the SEL pin is tied to VCC or left floating, and the VH3 voltage drops below 0.5V, an under-voltage condition is detected. On the contrary, when the SEL pin is tied to GND and the input drops below 0.5V, an over-voltage condition is detected. Connect it to VCC if not used.
6	5	VL3	OV Detector Input 3. The polarity of this input is determined by the state of the SEL pin as shown in Table 1. When the SEL pin is tied to VCC or left floating, and the VL3 voltage rises above 0.5V, an over-voltage condition is detected. On the contrary, when the SEL pin is tied to GND and the input rises above 0.5V, an under-voltage condition is detected. Connect it to GND if not used.

PIN DESCRIPTION (continued)

PIN		NAME	FUNCTION
SSOP	TQFN		
7	6	VH4	UV Detector Input 4. The polarity of this input is determined by the state of the SEL pin (see Table 1). When the SEL pin is tied to VCC and the VH4 voltage drops below 0.5V, an under-voltage condition is detected. On the contrary, when the SEL pin is tied to GND or left floating, and the input drops below 0.5V, an over-voltage condition is detected. Connect it to VCC if not used.
8	7	VL4	OV Detector Input 4. The polarity of this input is determined by the state of the SEL pin (see Table 1). When the SEL pin is tied to VCC and the VL4 voltage rises above 0.5V, an over-voltage condition is detected. On the contrary, when the SEL pin is tied to GND or left floating, and the input rises above 0.5V, an under-voltage condition is detected. Connect it to GND if not used.
9	8	GND	Ground.
10	9	REF	Buffered Reference Output. The typical output voltage is 1V and is designed to supervise negative voltages. It can supply ±1mA current and drive loads no larger than 1nF. Note that larger capacitive loads can cause instability. Leave it floating if not used.
11	10	nOV	Over-Voltage Reset Output. nOV is asserted low if an over-voltage event is monitored from VL1 to VL4 inputs. The SGM865A and SGM865C allow nOV to be latched low. The SGM865B and SGM865D hold nOV low for an adjustable timeout period determined by the TIMER capacitor. This pin has a weak pull-up to VCC and can be pulled up to 16V externally.
12	11	nUV	Under-Voltage Reset Output. nUV is asserted low if an under-voltage event is monitored from VH1 to VH4 inputs. The nUV pin remains low for an adjustable timeout set by the external capacitor on the TIMER pin. This pin has a weak pull-up to VCC and can be pulled up to 16V externally.
13	12	nLATCH	For SGM865A/SGM865C: nOV Latch Bypass Input/Clear Pin. If this pin is pulled high, the nOV latch will be cleared and work as what the nUV output does. If this pin is pulled low, the nOV output will be latched when asserted.
		DIS	For SGM865B/SGM865D: nOV and nUV Disable Input. If this pin is pulled high, the nOV and nUV outputs are held high no matter what the monitored voltages of the VHx and VLx input pins are. However, if a UVLO condition occurs, the nUV output is pulled low. DIS pin has a weak pull-down (1.6μA) to GND internally. Leave it floating if not used.
14	13	SEL	Input Polarity Select. Connect it to VCC or GND, or leave it open to select the polarity of VH3, VL3, VH4, and VL4 as shown in Table 1.
15	14	TIMER	Adjustable Reset Delay Timer. Adjust the reset timeout delay by connecting the external capacitor to this pin. Connect it to VCC to bypass the timer.
16	15	VCC	Supply Voltage. Usually, the VCC pin works in the ranges of 2.3V to 5V. For voltages greater than 5.5V, this pin maintains 5.5V if a shunt resistor is used to limit the current flowing into the VCC pin to less than 10mA. If the resistor is not adopted, the voltage at this pin must not exceed 5V. A 0.1μF bypass capacitor or greater is recommended.
—	Exposed Pad	EP	Exposed Pad. Connect it to GND.

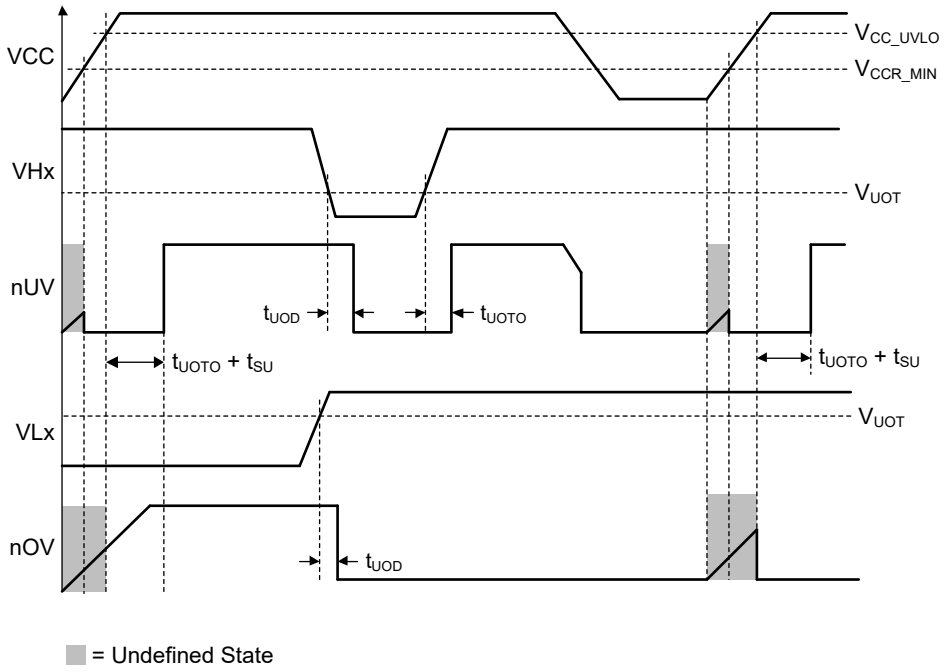
ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.3V to V_{SHUNT}, VLx = 0.45V, VHx = 0.55V, nLATCH = SEL = V_{CC}, DIS = Open, T_J = −40℃ to +125℃, typical values are measured at V_{CC} = 3.3V and T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Shunt Regulator						
VCC Shunt Regulator Voltage	V_{SHUNT}	I_{CC} = 5mA	5.3	5.5	5.7	V
VCC Shunt Regulator Load Regulation	ΔV_{SHUNT}	I_{CC} = 2mA to 10mA		10	200	mV
Supply						
Supply Voltage (1)	V_{CC}		2.3		V_{SHUNT}	V
Minimum VCC Output Valid	V_{CCR_MIN}	DIS = 0V			1	V
Supply Under-Voltage Lockout	V_{CC_UVLO}	DIS = 0V, VCC rising	2.0	2.16	2.3	V
Supply Under-Voltage Lockout Hysteresis	ΔV_{CC_HYST}	DIS = 0V	5	30	60	mV
Supply Current	I_{CC}	V_{CC} = 2.3V to 5V, SEL = VCC (external source)		35	75	μA
Reference Output						
Reference Output Voltage	V_{REF}	I_{VREF} = ±1mA	0.970	1	1.030	V
Under-Voltage/Over-Voltage Characteristics						
Under-Voltage/Over-Voltage Threshold	V_{UOT}		490	500	510	mV
Under-Voltage/Over-Voltage Threshold to Output Delay	t_{UOD}	VHx = V_{UOT} - 5mV or VLx = V_{UOT} + 5mV		125		μs
VHx, VLx Input Current	I_{VHL}	T_J = +25℃		1	±15	nA
		T_J = -40℃ to +125℃		1	±50	
nUV/nOV Timeout Period	t_{UOTO}	C_{TIMER} = 1nF	6.6	8.9	11	ms
nOV Latch Clear Input (SGM865A/SGM865C)						
nOV Latch Clear Threshold Input High	V_{LATCH_IH}		1.2			V
nOV Latch Clear Threshold Input Low	V_{LATCH_IL}				0.8	V
nLATCH Input Current	I_{LATCH}	V_{nLATCH} > 0.5V		0.01	±0.5	μA
Disable Input (SGM865B/SGM865D)						
DIS Input High	V_{DIS_IH}		1.2			V
DIS Input Low	V_{DIS_IL}				0.8	V
DIS Input Current	I_{DIS}	V_{DIS} > 0.5V	0.8	1.6	2.4	μA
Timer Characteristics						
TIMER Pull-Up Current	I_{TIMER_UP}	V_{TIMER} = 0V	-1.35	-2	-2.6	μA
TIMER Pull-Down Current	I_{TIMER_DOWN}	V_{TIMER} = 1.6V	1.35	2	2.6	μA
TIMER Disable Voltage	V_{TIMER_DIS}	Referenced to V_{CC}	-90	-250		mV
Output Voltage						
Output Voltage High, nUV/nOV	V_{OH}	V_{CC} = 2.3V, I_{nUV} = I_{nOV} = -1μA	1			V
Output Voltage Low, nUV/nOV	V_{OL}	V_{CC} = 2.3V, I_{nUV} = I_{nOV} = 2.5mA		0.1	0.2	V
		V_{CC} = 1V, I_{UV} = 100μA		0.005	0.03	
Three-State Input SEL						
High Level Input Voltage	V_{IH}		1.4			V
Low Level Input Voltage	V_{IL}				0.4	V
SEL Pin Voltage When Left in High-Z State	V_Z	I_{SEL} = ±10μA	0.8	0.9	1.0	V
Maximum SEL Input Current	I_{SEL_MAX}	SEL tied to VCC or GND			±35	μA

NOTE: 1. For the VCC pin, a shunt regulator begins to work when the VCC voltage rises above 5.5V and the current flowing into this pin must be constrained to no larger than 10mA. Usually, a shunt resistor is adopted to undertake the voltage drop.

TIMING DIAGRAM



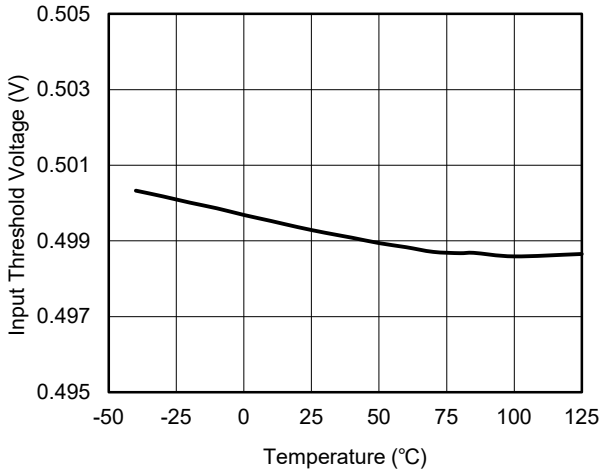
NOTES:

1. SEL = V_{CC}, TIMER = CAP.
2. t_{SU} is about 150μs. It is recommended that VHx and VLx are powered on 1ms after V_{CC} is above V_{CC_UVLO}.

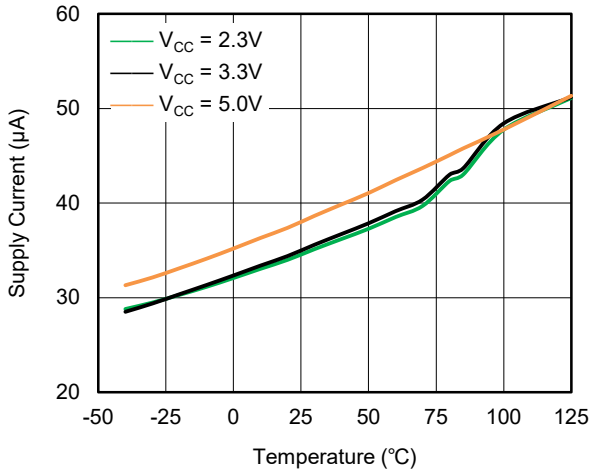
Figure 2. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

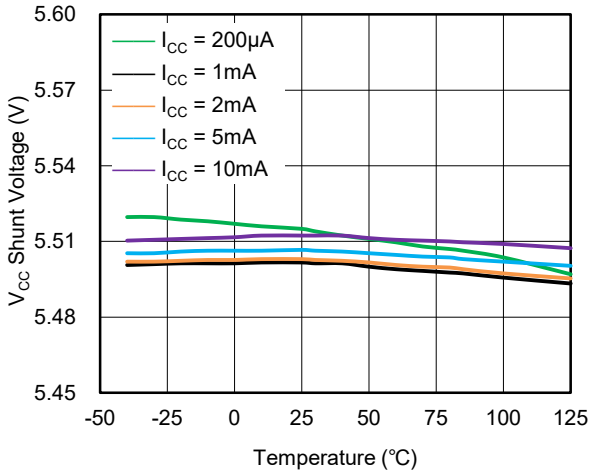
Input Threshold Voltage vs. Temperature



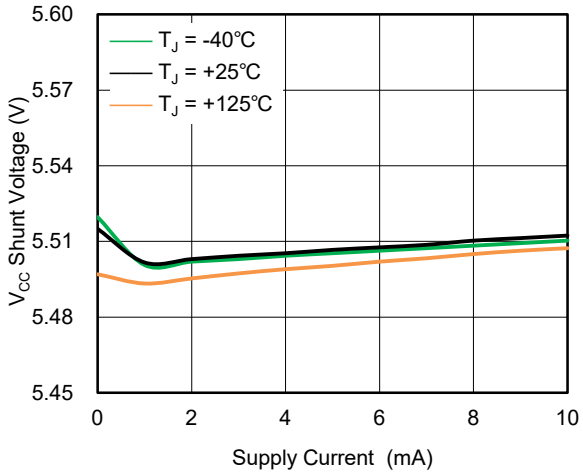
Supply Current vs. Temperature



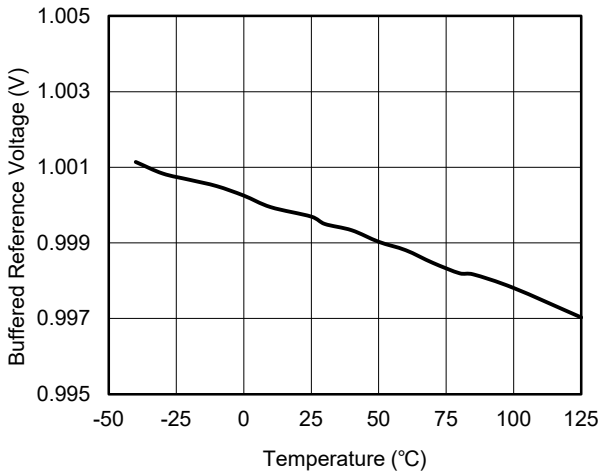
V_{CC} Shunt Voltage vs. Temperature



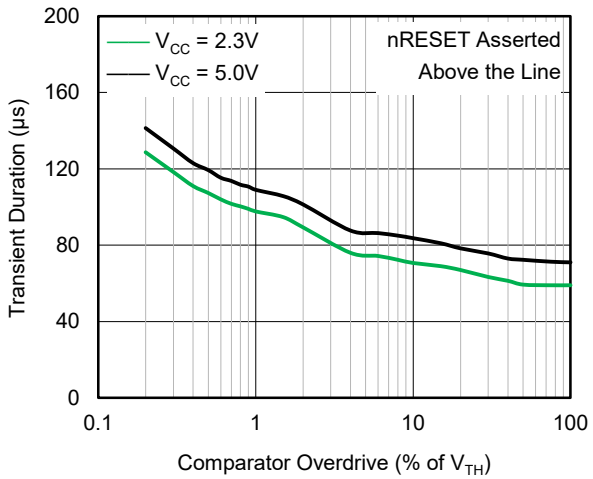
V_{CC} Shunt Voltage vs. Supply Current



Buffered Reference Voltage vs. Temperature

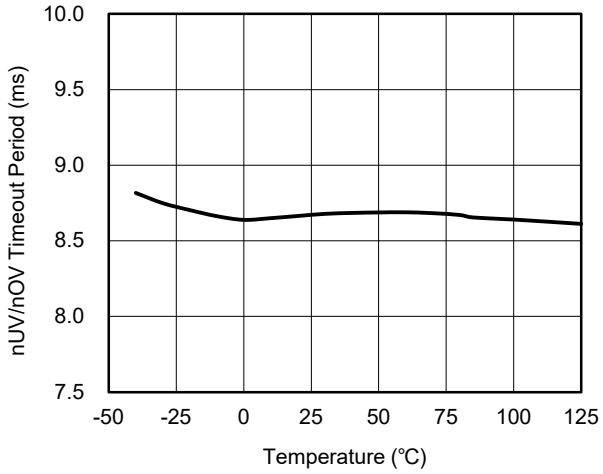


Transient Duration vs. Comparator Overdrive

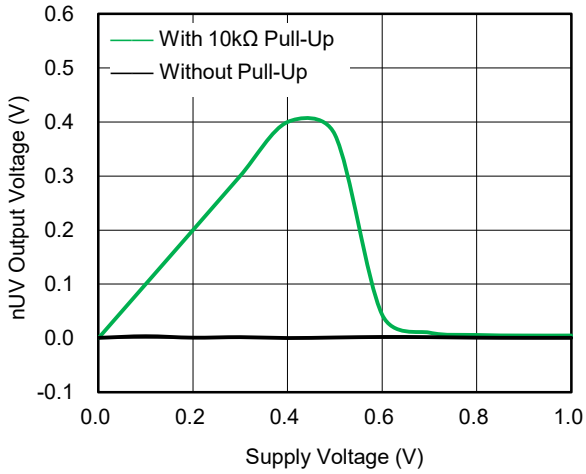


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

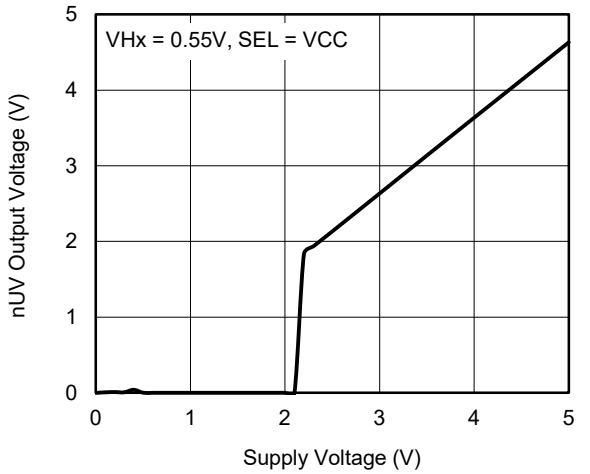
nUV/nOV Timeout Period vs. Temperature



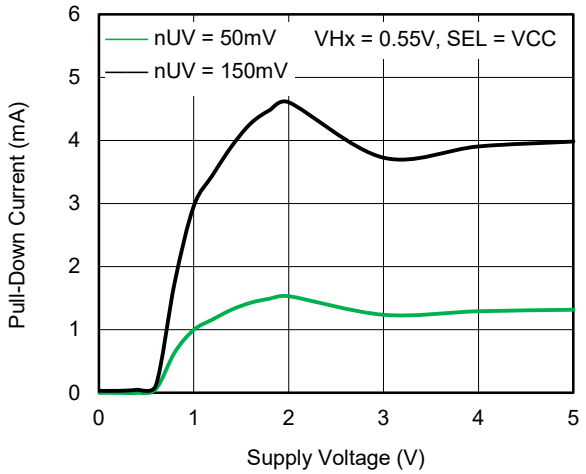
nUV Output Voltage vs. Supply Voltage



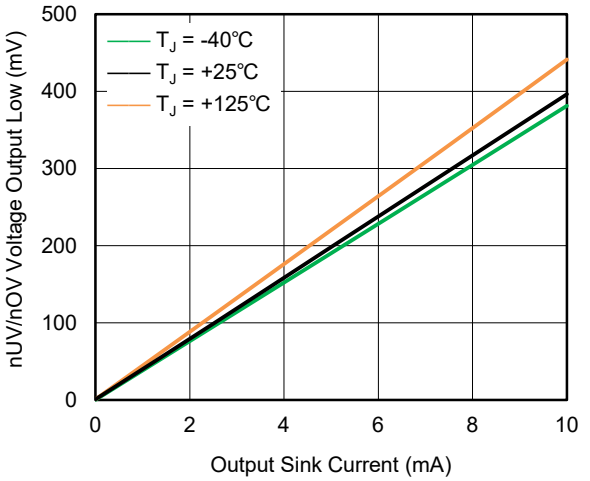
nUV Output Voltage vs. Supply Voltage



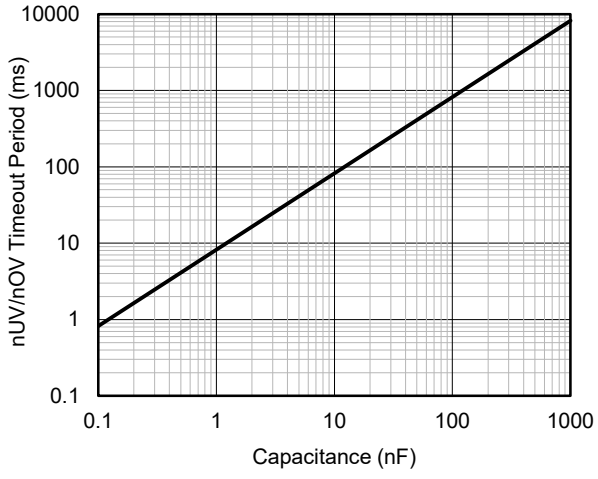
Pull-Down Current vs. Supply Voltage



nUV/nOV Voltage Output Low vs. Output Sink Current



nUV/nOV Timeout Period vs. Capacitance



FUNCTIONAL BLOCK DIAGRAM

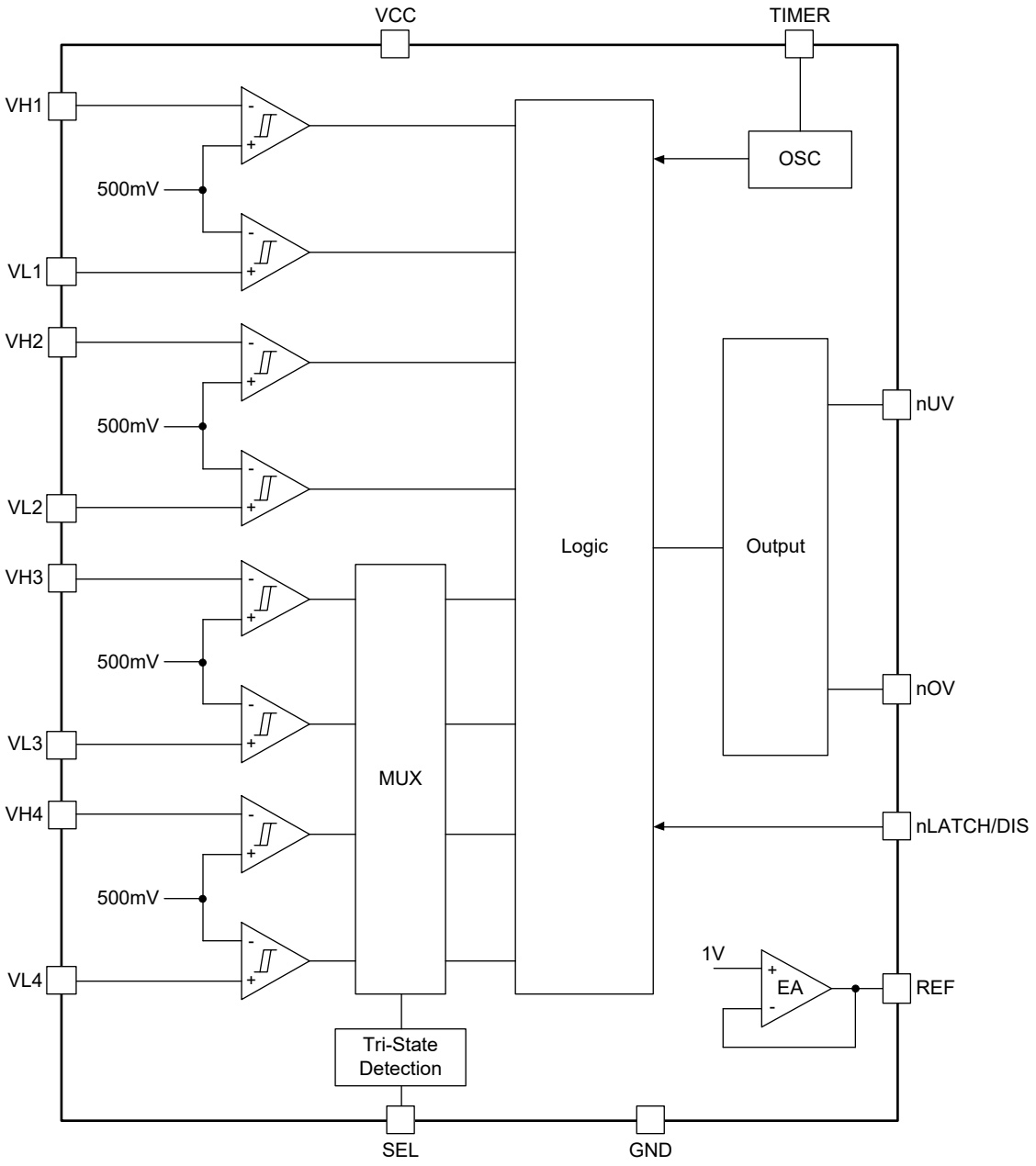


Figure 3. Block Diagram

DETAILED DESCRIPTION

Voltage Supervision

The SGM865 is designed to monitor over-voltage and under-voltage conditions across up to four voltage rails. Each rail utilizes two dedicated pins of VLx and VHx. VLx is used to detect over-voltage, and VHx is used to detect under-voltage. These pins are fed into independent internal voltage comparators, where the input voltages are compared against a 0.5V reference voltage with ±2% accuracy.

All under-voltage comparator outputs are connected to a shared nUV output terminal, while over-voltage comparator outputs converge at a centralized nOV output terminal. This configuration enables consolidated signaling for voltage anomaly detection.

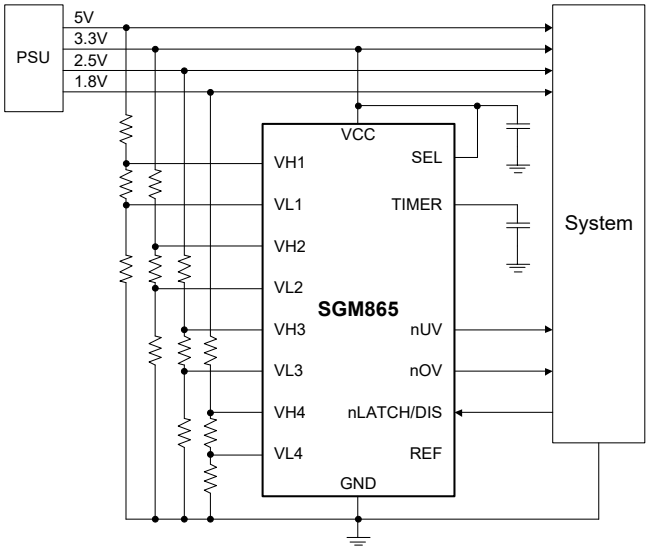


Figure 4. Typical Applications Diagram

Polarity Configuration

The SGM865 monitors both positive and negative voltage polarities for supply rails. The SEL pin, as a tri-state input, can be connected to VCC, GND, or left unconnected to define the polarity configuration of Inputs 3 and 4 (See Table 1). Note that the inputs 1 and 2 are positive polarity in default whatever the SEL pin state is.

When monitoring a positive voltage, the input employs the three-resistor divider configuration shown in Figure 5. Here, VHx (under-voltage detection pin) is connected to the high-side node of the resistor divider, while VLx (over-voltage detection pin) connects to the low-side node.

For negative voltage monitoring, the internal functional paths of VLx and VHx are automatically rerouted. As illustrated in Figure 6, the negative supply voltage is connected using the same physical pin arrangement: VHx remains attached to the high-side divider node and VLx stays at the low-side node.

Monitoring Pin Connections

Positive Voltage Monitoring Scheme

Figure 5 shows the positive voltage monitoring input connection, where V_M is the monitored supply voltage, and I_M is the current flowing through the resistor divider. V_{OV} is the over-voltage trip point, and V_{UV} is the under-voltage trip point.

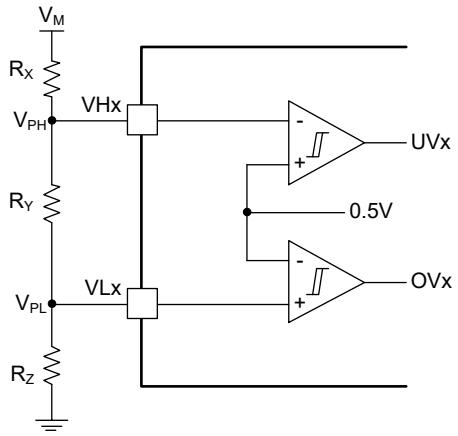


Figure 5. Positive UV/OV Monitoring Configuration

Table 1. Polarity Configuration

SEL Pin	Input 3			Input 4		
	Polarity	UV	OV Condition	Polarity	UV Condition	OV Condition
Connected to VCC	Positive	VH3 < 0.5V	VL3 > 0.5V	Positive	VH4 < 0.5V	VL4 > 0.5V
Left Unconnected	Positive	VH3 < 0.5V	VL3 > 0.5V	Negative	VL4 > 0.5V	VH4 < 0.5V
Connected to GND	Negative	VL3 > 0.5V	VH3 < 0.5V	Negative	VL4 > 0.5V	VH4 < 0.5V

DETAILED DESCRIPTION (continued)

Three external resistors (R_X, R_Y and R_Z) split V_M into two divided voltages: the high-side voltage (V_{PH}) and the low-side voltage (V_{PL}). V_{PH} is linked to the VHx terminal, while V_{PL} is connected to the VLx terminal. An over-voltage event is triggered when the measured V_{PL} voltage on the VLx pin surpasses the 0.5V threshold. The formula for calculating V_{PL} (the low-side voltage) is provided below:

$$V_{PL} = V_{OV} \times \left(\frac{R_Z}{R_X + R_Y + R_Z} \right) = 0.5V \quad (1)$$

Also,

$$R_X + R_Y + R_Z = \frac{V_M}{I_M} \quad (2)$$

Therefore, juggle the two equations mentioned above, and yield the value of R_Z:

$$R_Z = \frac{0.5 \times V_M}{V_{OV} \times I_M} \quad (3)$$

Likewise, the formula for calculating V_{PH} is provided below:

$$V_{PH} = V_{UV} \times \left(\frac{R_Y + R_Z}{R_X + R_Y + R_Z} \right) = 0.5V \quad (4)$$

And R_Y can be calculated through R_Z mentioned above:

$$R_Y = \frac{0.5 \times V_M}{V_{UV} \times I_M} - R_Z \quad (5)$$

Then, R_X can be calculated through R_Y and R_Z:

$$R_X = \frac{V_M}{I_M} - R_Z - R_Y \quad (6)$$

The calculation result is affected by the values of V_M, I_M, V_{OV} and V_{UV}.

Negative Voltage Monitoring Scheme

Figure 6 shows the negative voltage monitoring input connection. A 1V reference voltage generated by the REF pin is required to provide the bias for negative voltage monitoring.

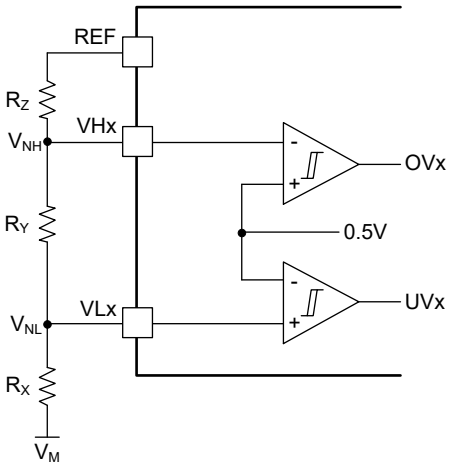


Figure 6. Negative UV/OV Monitoring Configuration

The equations in Positive Voltage Monitoring Scheme section require slight adjustments for negative voltage applications. Since a 1V reference is included in the total voltage drop calculation, this value must be subtracted from V_M, V_{UV}, and V_{OV} parameters before applying them in the original formulas.

When monitoring negative voltages, the resistor divider network splits the voltage difference between the 1V reference and the negative supply rail into two components: high-side voltage (V_{NH}) and low-side voltage (V_{NL}). Like the positive voltage configuration, V_{NH} connects to the VHx pin while V_{NL} connects to the VLx pin. Additional implementation details can be found in the Voltage Monitoring Example section.

Threshold Accuracy

Ensuring precise reset threshold accuracy is critical, particularly at lower voltage levels. For instance, an FPGA system requiring a 1V core supply within ±6% tolerance, whose power source maintains ±1% regulation range, necessitates continuous voltage monitoring to stay within operational limits. As demonstrated in Figure 7, UV/OV detection must account for inherent supply voltage fluctuations that narrow the allowable threshold-setting window. In this scenario, all threshold parameters (including tolerances) must fit within a 0.05V monitoring range. Utilizing 0.1%-tolerance resistors, the SGM865 is able to achieve this precision requirement.

DETAILED DESCRIPTION (continued)

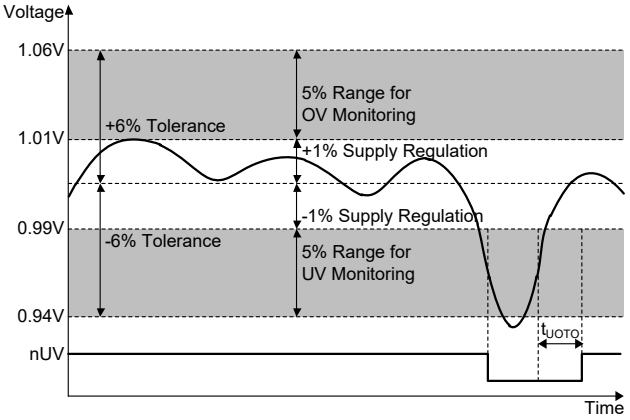


Figure 7. Monitoring Threshold Accuracy Example

Voltage Monitoring Example

To demonstrate the functionality of SGM865 in practice, refer to the 1V input scenario in Figure 7, which incorporates a -12V power rail. The initial step involves selecting the baseline current through both resistor divider networks, which is assumed to be 5μA here.

Given the 1V core supply requirement for FPGA (±6% tolerance) and the power source (±1% regulation accuracy), the UV and OV thresholds must be positioned within the center of the allowable monitoring window. Specifically, the thresholds are set at ±3.25% of the nominal supply voltage. This results in a UV threshold of 0.9675V and an OV threshold of 1.0325V to ensure safe operation within the constrained voltage band.

Thus, the value of R_Z can be calculated as:

$$R_Z = \frac{0.5 \times 1}{1.0325 \times \left(5 \times 10^{-6}\right)} \approx 96.5\text{k}\Omega \quad (7)$$

Take the value of R_Z into Equation 8.

$$R_Y = \frac{0.5 \times 1}{0.9675 \times \left(5 \times 10^{-6}\right)} - 96.5\text{k}\Omega \approx 6.8\text{k}\Omega \quad (8)$$

And R_X can be calculated by Equation 9 with R_Z and R_Y.

$$R_X = \frac{1}{5 \times 10^{-6}} - 96.5\text{k}\Omega - 6.8\text{k}\Omega \approx 96.5\text{k}\Omega \quad (9)$$

The design method aligns with the application requirements. As outlined, the 1V power rail has a ±6% input tolerance and a ±1% supply accuracy. This means the OV monitoring threshold, accounting for all tolerance factors, must fall within the window from 1.01V to 1.06V. Similarly, the UV threshold must stay between 0.94V and 0.99V. The four extreme scenarios for minimum/maximum UV and OV thresholds are calculated below:

Minimum/maximum over-voltage threshold:

$$V_{OV_MIN} = 0.5\text{V} \times (1 - 2\%) \times \left(1 + \frac{(R_X - 0.1\%) + (R_Y - 0.1\%)}{R_Z + 0.1\%}\right)$$
$$= 0.49 \times \left(1 + \frac{(96500 + 6800) \times 0.999}{96500 \times 1.001}\right) = 1.013\text{V} > 1.01\text{V} \quad (10)$$

$$V_{OV_MAX} = 0.5\text{V} \times (1 + 2\%) \times \left(1 + \frac{(R_X + 0.1\%) + (R_Y + 0.1\%)}{R_Z - 0.1\%}\right) \quad (11)$$
$$= 1.057\text{V} < 1.06\text{V}$$

The maximum and minimum over-voltage threshold values lie within the 1.01V to 1.06V range specified.

Minimum/maximum under-voltage threshold:

$$V_{UV_MIN} = 0.5\text{V} \times (1 - 2\%) \times \left(1 + \frac{R_X - 0.1\%}{(R_Y + 0.1\%) + (R_Z + 0.1\%)}\right) \quad (12)$$
$$= 0.947\text{V} > 0.94\text{V}$$

$$V_{UV_MAX} = 0.5\text{V} \times (1 + 2\%) \times \left(1 + \frac{R_X + 0.1\%}{(R_Y - 0.1\%) + (R_Z - 0.1\%)}\right) \quad (13)$$
$$= 0.987\text{V} < 0.99\text{V}$$

The values stay within the under-voltage range, and all four worst-case scenarios pass the tolerance check, confirming the design approach as valid.

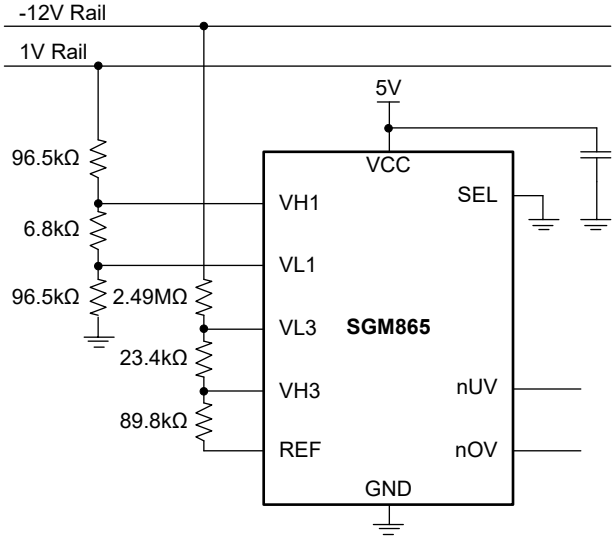


Figure 8. Positive and Negative Supply Monitor Example

DETAILED DESCRIPTION (continued)

Next, for a -12V input defined with a ±20% tolerance, the supply threshold precision is set to ±5% relative to the -12V rail. This establishes an over-voltage threshold of -13.5V and an under-voltage threshold of -10.5V. The negative voltage setup mandates incorporating the 1V reference voltage into Equations 14 to 16. Specifically, the 1V reference is subtracted from V_M, V_{UV}, and V_{OV}, with the absolute value of each result calculated.

Thus, the value of R_Z can be calculated as:

$$R_Z = \frac{0.5 \times \left(\left|-12-1\right|\right)}{\left(\left|-13.5-1\right|\right) \times \left(5 \times 10^{-6}\right)} \approx 89.8k\Omega \quad (14)$$

Take the value of R_Z into Equation 15.

$$R_Y = \frac{0.5 \times \left(\left|-12-1\right|\right)}{\left(\left|-10.5-1\right|\right) \times \left(5 \times 10^{-6}\right)} - 89.8k\Omega \approx 23.4k\Omega \quad (15)$$

And R_X can be calculated by Equation 16 with R_Z and R_Y.

$$R_X = \frac{\left|-12-1\right|}{5 \times 10^{-6}} - 89.8k\Omega - 23.4k\Omega \approx 2.49M\Omega \quad (16)$$

Power-Up and Power-Down

During power-up, when VCC reaches 1V, the active-low nUV pin is pulled to logic low, while the nOV pin rises to VCC. Once the VCC pin voltage stabilizes at 1V, the SGM865 ensures nUV is pulled low and nOV is driven high. When VCC exceeds V_{CC_UVLO}, the nUV and nOV states are determined by the VHx and VLx inputs. With valid VCC and VHx signals present, an internal timer initiates. After an adjustable delay period, nUV is weakly pulled up.

nUV/nOV Timing Characteristics

For the active-low nUV output, it triggers whenever any of the four monitored voltages drops below its designated threshold. When VCC exceeds V_{CC_UVLO}, an internal timer maintains nUV in the low state for a programmable duration (t_{UOTO}) following recovery of all monitored rails above their thresholds, providing stabilization time post-power-up. If any monitored voltage subsequently falls below its threshold, the timer resets. Once all rails return above thresholds, the timer restarts.

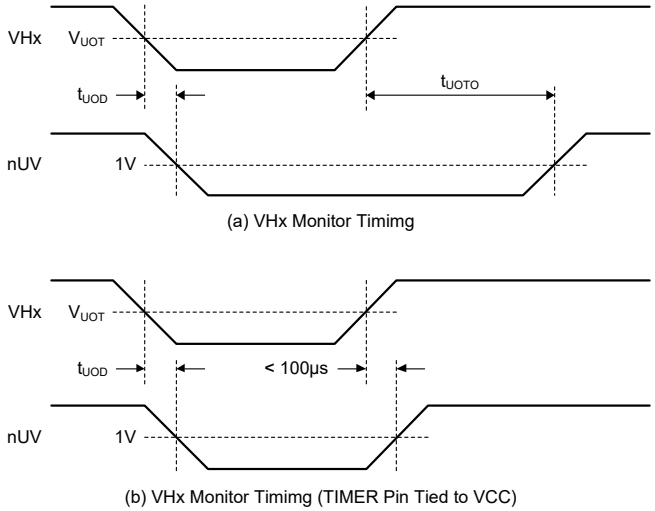
Both nUV and nOV outputs remain asserted for an adjustable hold period after all faults clear, with the timeout duration set by an external capacitor connected to the TIMER pin.

Timer Capacitor Selection

Note that the nUV and nOV outputs remain asserted for an adjustable hold period t_{UOTO} after all faults clear. The timeout duration t_{UOTO} is set by an external capacitor connected to the TIMER pin and can be calculated as:

$$C_{TIMER} = t_{UOTO} \times 112 \times 10^{-9} \left(F/\sec\right) \quad (17)$$

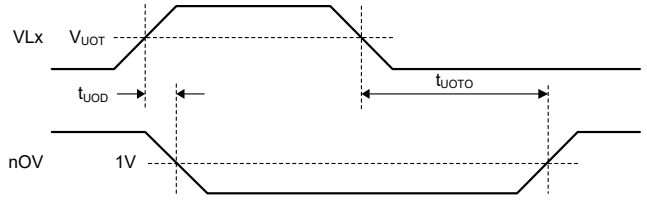
The nUV/nOV timeout period vs. capacitance curve in the Typical Performance Characteristics section shows the relationship between delay time and the timer capacitor value. A capacitor with a minimum value of 10pF is required. The selected timer capacitor must exhibit a leakage current higher than the minimum charging current of the TIMER pin (1.35μA). Connect the TIMER pin to VCC to disable the programmable timeout.



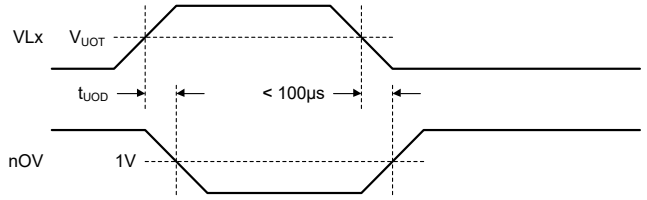
NOTE: If an input is set to monitor a negative voltage, VHx will indicate an over-voltage condition.

Figure 9. VHx Positive Voltage Monitoring

DETAILED DESCRIPTION (continued)



(a) VLx Monitor Timimg



(b) VLx Monitor Timimg (TIMER Pin Tied to VCC)

NOTE: If an input is set to monitor a negative voltage, VLx will indicate an under-voltage condition.

Figure 10. VLx Positive Voltage Monitoring

nUV/nOV Output Characteristics

The nOV and nUV outputs include a strong grounding pull-down and a weak internal pull-up to VCC. This setup allows the pins to function as open-drain outputs. When rise time is not a priority, the weak pull-up eliminates the need for an external pull-up resistor. The open-drain design supports wire-OR functionality, useful for scenarios requiring multiple signals to drive the output low.

At V_{CC} = 1V, the nUV output guarantees a maximum V_{OL} of 0.15V. For nOV at V_{CC} = 1V, its weak pull-up current is fully enabled. As a result, if maintaining the nOV pin's state and pull-up strength is critical at low V_{CC}, an external pull-up resistor smaller than 100kΩ is recommended to boost the pull-up strength. In wire-OR configurations, any device pull-down capability must therefore compensate for this increased pull-up strength requirement.

Glitch Immunity

The SGM865 can withstand brief voltage spikes on monitored power rails. Its built-in filtering mechanisms ensure protection against rapid transient disturbances. Transient Duration vs. Comparator Overdrive in the Typical Performance Characteristics section demonstrates the device tolerance by indicating the maximum allowable transient duration without triggering a reset pulse. This glitch immunity enables reliable operation in electrically noisy settings.

Under-Voltage Lockout (UVLO)

The SGM865 includes an under-voltage lockout circuit that tracks the voltage at the VCC pin. If the VCC voltage falls below V_{CC_UVLO}, the protection mechanism engages. This activates the nUV output while simultaneously holding the nOV output inactive and blocking its activation. Once VCC voltage recovers, the nUV output's timing response aligns with that observed during an under-voltage event on the input lines.

Shunt Regulator

The SGM865 derives power through its VCC pin, which can be connected directly to a supply rail up to 5.5V. Under this configuration, the device consumes current no more than 100μA. For voltages exceeding 5.5V, an internal shunt regulator enables operation by inserting a droop resistor in series between the supply and the VCC pin. This resistor extends input current range to no more than 10mA.

After establishing the input voltage (denoted as V_{IN}), calculate the optimal resistance as follows. First, compute the total supply current (I_{CC_TOTAL}) by combining the current drawn from REF pin, and/or other pins directly or indirectly connected to VCC pin with the device's maximum specified current. Values for the shunt regulator's minimum and maximum voltage thresholds (V_{SHUNT_MIN} and V_{SHUNT_MAX}) from the electrical specifications are required for these calculations.

Calculate the maximum and minimum dropper resistor values.

$$R_{MIN} = \frac{V_{IN_MIN} - V_{SHUNT_MAX}}{I_{CC_TOTAL}} \quad (18)$$

$$R_{MAX} = \frac{V_{IN_MAX} - V_{SHUNT_MIN}}{100\mu A} \quad (19)$$

Select a practical resistor value within the given range above. Considering the specified accuracy of the resistor, determine the minimum and maximum possible variations of the real resistor value, denoted as R_{REAL_MIN} and R_{REAL_MAX}, respectively. Calculate the maximum device power as follows:

$$P_{DEVICE_MAX} = V_{SHUNT_MAX} \times \frac{V_{IN_MAX} - V_{SHUNT_MAX}}{R_{REAL_MIN}} \quad (20)$$

DETAILED DESCRIPTION (continued)

Verify the acceptability of the calculated resistor value by determining the maximum temperature increase of the device.

$$T_{RISE_MAX} = \theta_{JA} \times P_{DEVICE_MAX} \quad (21)$$

Add T_{RISE_MAX} to the ambient operating temperature. If the resistor value is appropriate, the result will remain within the device's operating temperature range of -40℃ to +125℃.

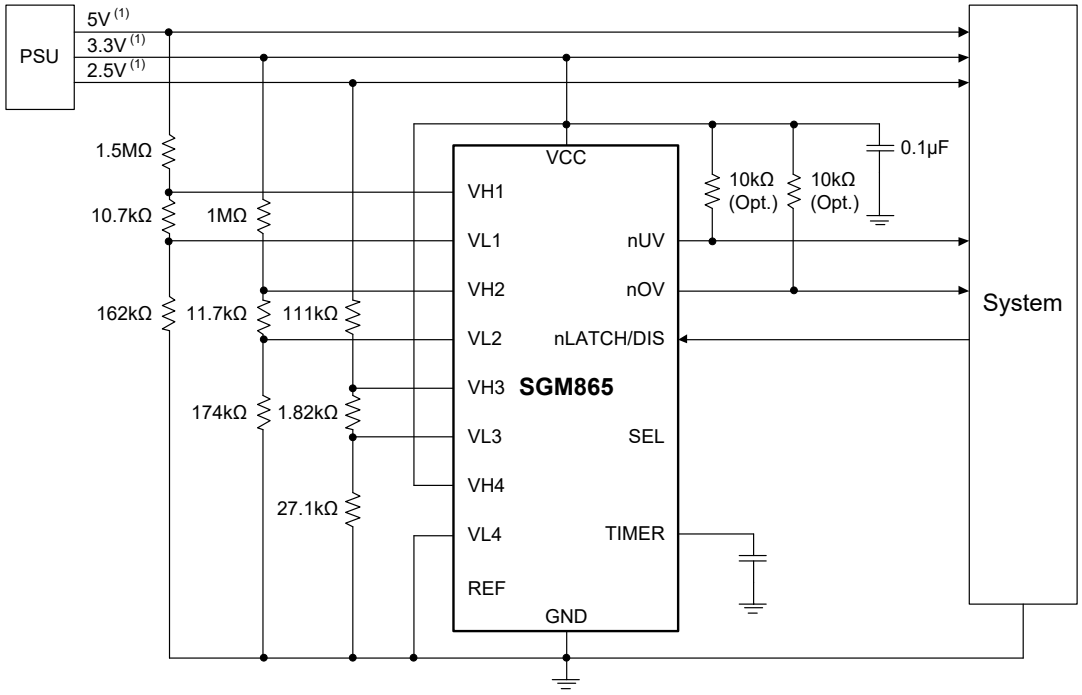
nOV Latch (SGM865A/C)

When the nLATCH pin is logic low and an over-voltage event occurs, the nOV output locks at the low state. Raising the nLATCH pin to high resets the latch state. If the over-voltage condition resolves while nLATCH is high, the latch mechanism is bypassed, and the nOV pin functions identically to the nUV pin, including a matching timeout duration. If the nLATCH pin is set low during an active timeout, the nOV output locks low, consistent with standard operation.

DISABLE (SGM865B/D)

When the DIS pin is driven to a high voltage level, it deactivates both the nUV and nOV outputs, maintaining them at a high logic state regardless of any detected faults. If a UVLO condition occurs, the nUV pin transitions to a low state immediately, but the timeout function is neglected. The nUV output returns to high as soon as the UVLO condition is resolved. To ensure stable operation when the DIS pin is unconnected, a 1.6μA weak internal pull-down current is integrated in SGM865B/D.

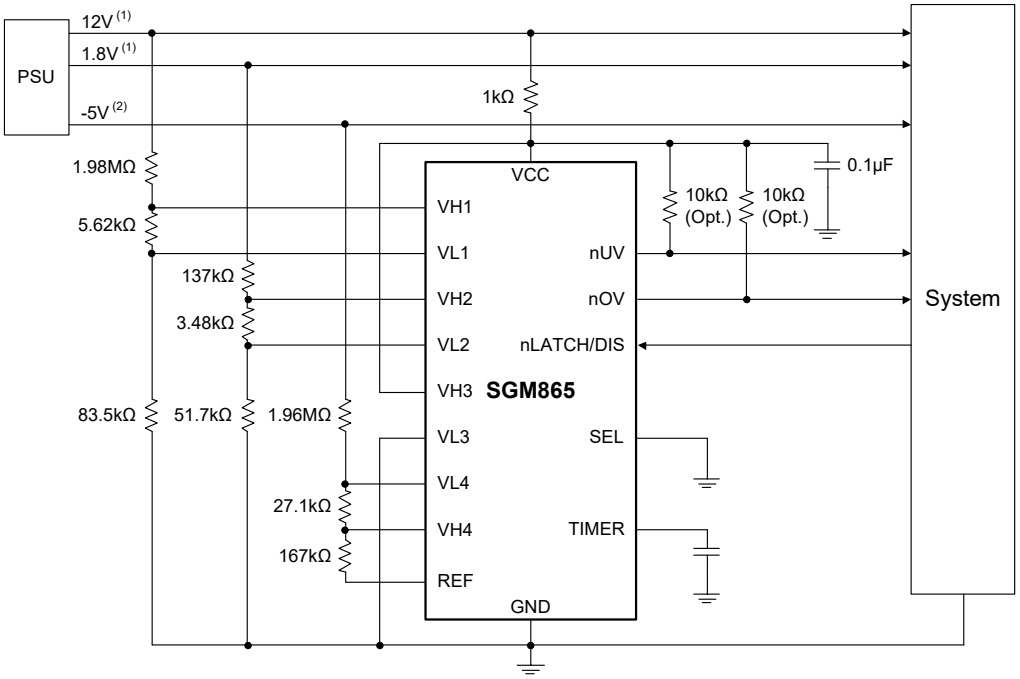
TYPICAL APPLICATION CIRCUITS



NOTE: 1. 1.5% supply tolerance, 5% input tolerance.

Figure 11. Typical Application Diagram for Monitoring 5V, 3.3V and 2.5V

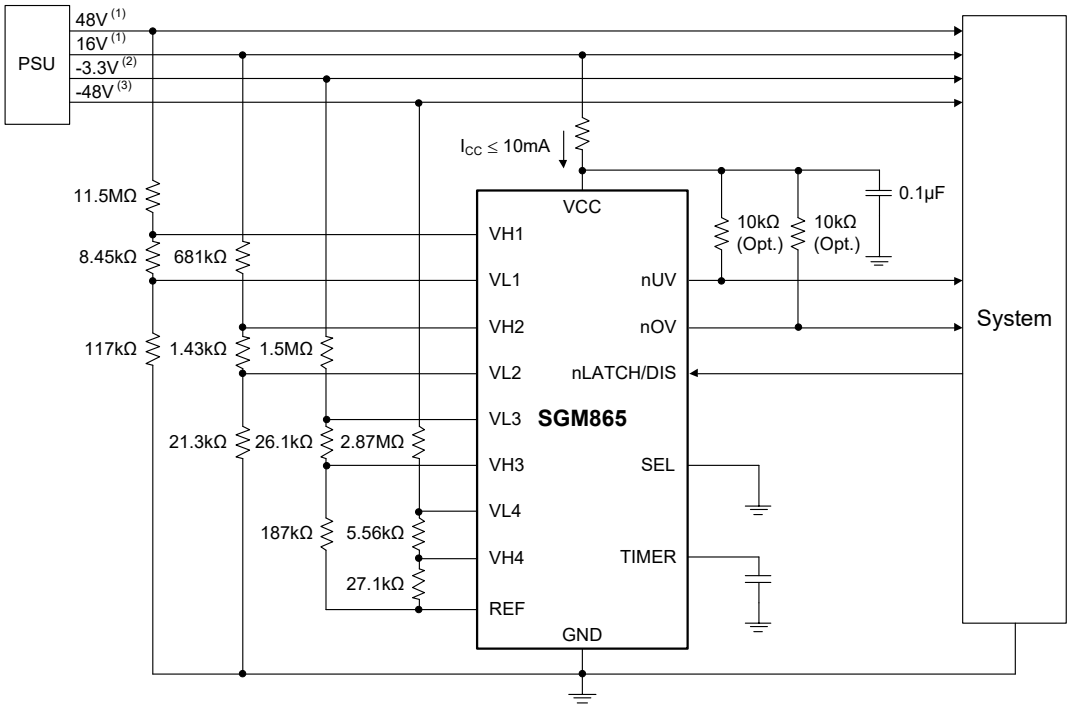
TYPICAL APPLICATION CIRCUITS (continued)



NOTES:

1. 1.5% supply tolerance, 5% input tolerance.
2. 3% supply tolerance, 15% input tolerance.

Figure 12. Typical Application Diagram for Monitoring 12V, 1.8V and -5V



NOTES:

1. 1.5% supply tolerance, 10% input tolerance.
2. 2% supply tolerance, 15% input tolerance.
3. 4% supply tolerance, 15% input tolerance.

Figure 13. Typical Application Diagram for Monitoring 48V, 16V, -3.3V, and -48V

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

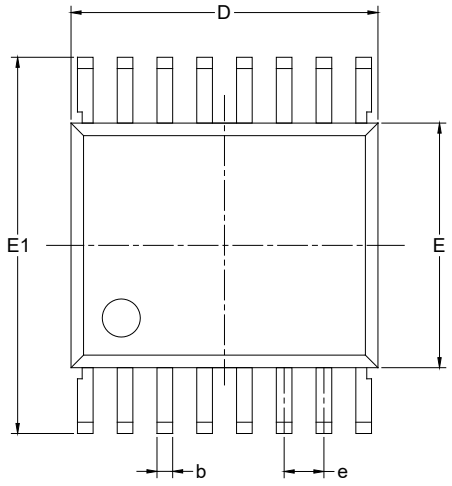
JULY 2026 – REV.A.1 to REV.A.2	Page
Updated Detailed Description section	12
Updated Typical Application Circuits section	16

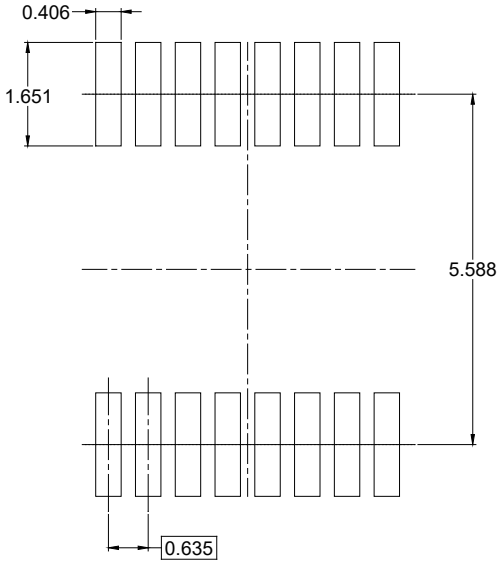
JANUARY 2026 – REV.A to REV.A.1	Page
Added Timing Diagram section	6
Updated Detailed Description section	13

Changes from Original to REV.A (JUNE 2025)	Page
Changed from product preview to production data	All

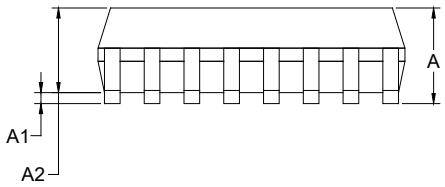
PACKAGE OUTLINE DIMENSIONS

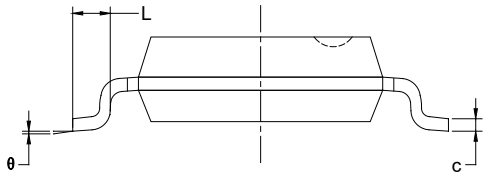
SSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)



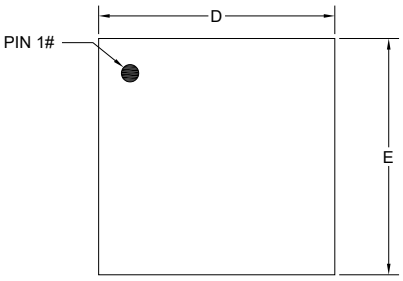


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.200	0.300	0.008	0.012
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	0.635 BSC		0.025 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

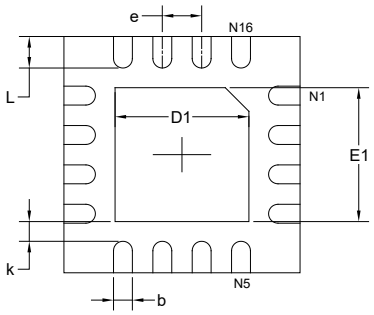
NOTES:
1. Body dimensions do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

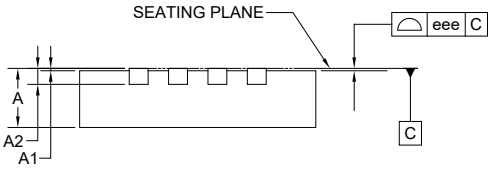
TQFN-3×3-16L



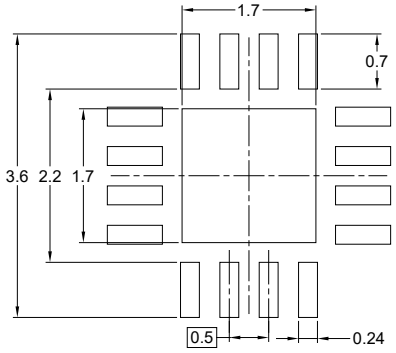
TOP VIEW



BOTTOM VIEW



SIDE VIEW



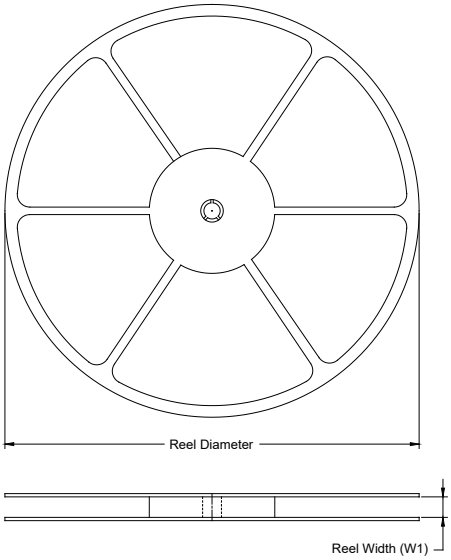
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020
eee	0.080		0.003	

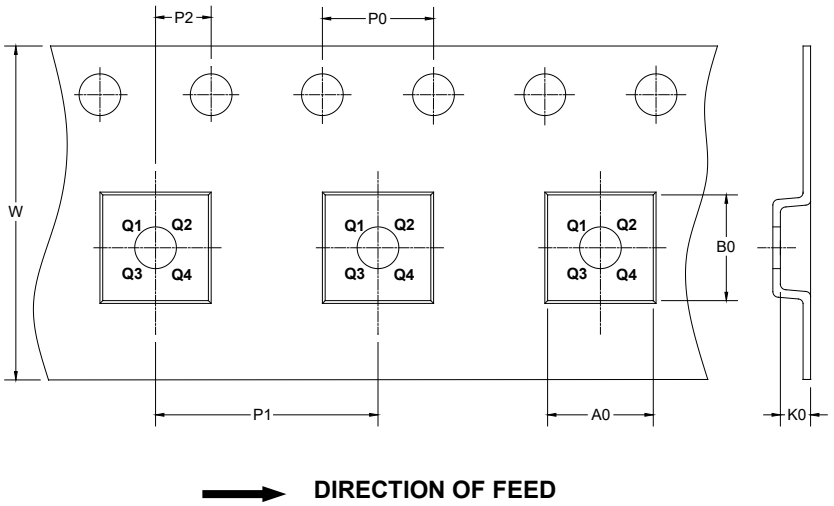
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



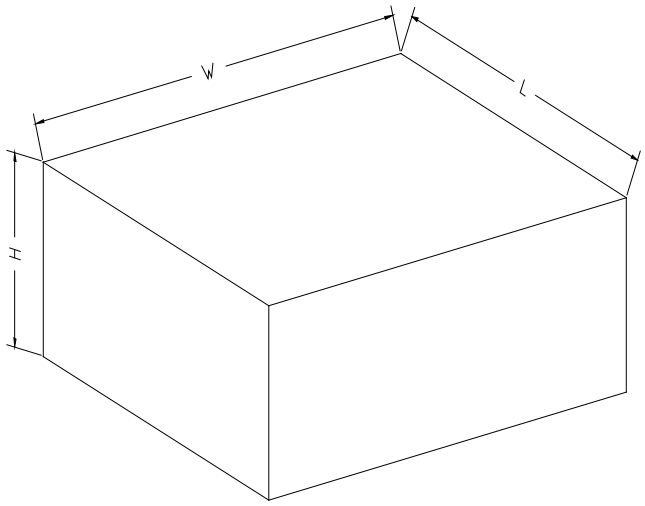
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SSOP-16	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
TQFN-3×3-16L	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002