SGM823A
Microprocessor Supervisory Circuit with Watchdog Timer and Manual Reset

GENERAL DESCRIPTION

The SGM823A is a complete microprocessor supervisory device which combines reset, watchdog and manual reset functions in a SOT-23-5 package. System reliability is significantly improved by such integration compared to the designs with individual ICs or discrete components. The SGM823A also features an excellent transient immunity to ignore fast V_{CC} transients.

This device has an active-low push-pull reset output (nRESET) that is activated by a logic low on the manual reset input (nMR), a watchdog expiry event or due to a low V_{CC} voltage. The nRESET output can still be in the correct logic state even if V_{CC} is 1V. The SGM823A is offered in three fixed V_{CC} reset threshold voltages.

The SGM823A is available in a Green SOT-23-5 package. It operates over a junction temperature range of -40℃ to +125℃.

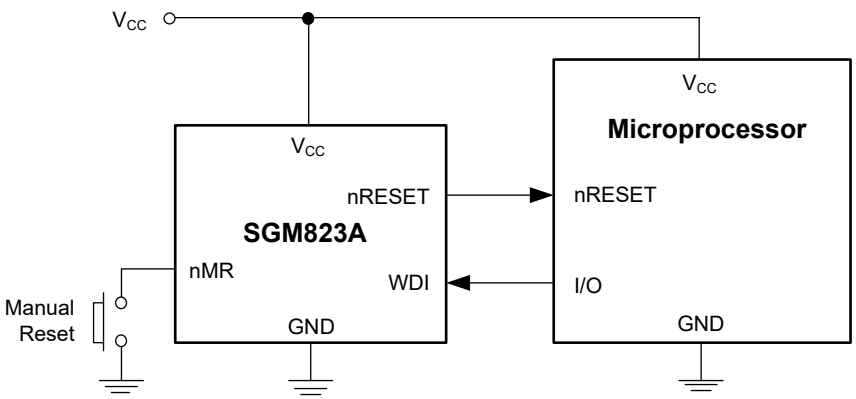
FEATURES

- **Ultra-Low Supply Current: 0.64μA (TYP)**
- **Precision Supply-Voltage Monitor**
  - **2.19V for SGM823A-Y**
  - **1.67V for SGM823A-W**
  - **1.58V for SGM823A-V**
- **Guaranteed nRESET Valid at V_{CC} = 1V**
- **Push-Pull nRESET Output**
- **Reset Pulse Width: 200ms (TYP)**
- **Debounced TTL/CMOS-Compatible**
- **Manual Reset Input**
- **Watchdog Timer with 1.6s (TYP) Timeout**
- **Fully Specified over Temperature**
- **Power-Supply Transient Immunity**
- **Without External Components**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green SOT-23-5 Package**

APPLICATIONS

Computers
Portable Equipment
Automotive Equipment
Intelligent Instruments
Critical μP Power Monitoring

TYPICAL APPLICATION

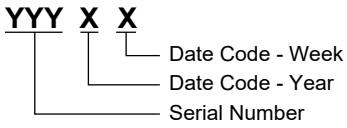


PACKAGE/ORDERING INFORMATION

MODEL	RESET THRESHOLD (V)	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM823A	2.19	SOT-23-5	SGM823A-YXN5G/TR	CV5XX	Tape and Reel, 3000
	1.67	SOT-23-5	SGM823A-WXN5G/TR	CV4XX	Tape and Reel, 3000
	1.58	SOT-23-5	SGM823A-VXN5G/TR	CV3XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with Respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- All Other Inputs ..... -0.3V to V_{CC} + 0.3V

Input Current
- V_{CC} 20mA
- GND 20mA

Output Current
- All Outputs 20mA

Package Thermal Resistance
- SOT-23-5, θ_{JA} ..... 180.8℃/W
- SOT-23-5, θ_{JB} ..... 59.3℃/W
- SOT-23-5, θ_{JC} ..... 100.3℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM ..... ±4000V
CDM ..... ±1000V

RECOMMENDED OPERATING CONDITIONS

Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

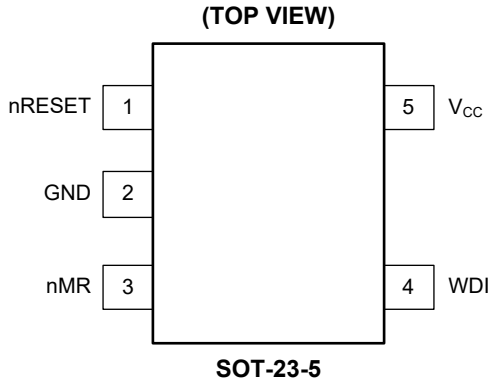
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	nRESET	O	Active-Low Reset Output Pin. It delivers a 200ms (TYP) low pulse when activated. nRESET remains low if V_{CC} is below the reset threshold or nMR is logic low. It remains low for 200ms after any of the following events: V_{CC} rises above the reset threshold, a watchdog expiry triggers a reset, or the nMR input goes from low to high.
2	GND	–	Ground.
3	nMR	I	Manual Reset Input Pin. nRESET keeps low when nMR is low. When nMR is high, nRESET becomes high after a 200ms timeout period. It is an active-low reset input with an internal 65kΩ pull-up resistor. nMR can be driven by a CMOS/TTL logic or by a switch shorting to GND. If not used, leave it open or connect it to V_{CC}.
4	WDI	I	Watchdog Input Pin. If the high or low state of WDI exceeds the watchdog timeout period, the internal watchdog timer is expired and a reset is triggered. The internal watchdog timer is clear while a reset is asserted. The timer is also cleared if the WDI input is changed (on rising or falling edges). The watchdog feature is disabled if the WDI is left open or if it is connected to a three-stated buffer output. If it requires the SGM823A to switch WDI from normal state to disable state, ensure that the WDI enters the high-Z state from logic low within the period of 1.4s after the last WDI falling edge.
5	V_{CC}	I	Supply Voltage Pin.

NOTE: I: input; O: output.

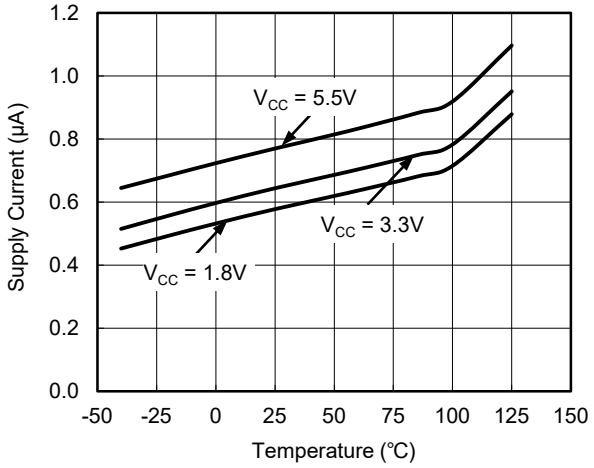
ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.1V to 2.75V for SGM823A-Y, V_{CC} = 1.53V to 2.0V for SGM823A-W/V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

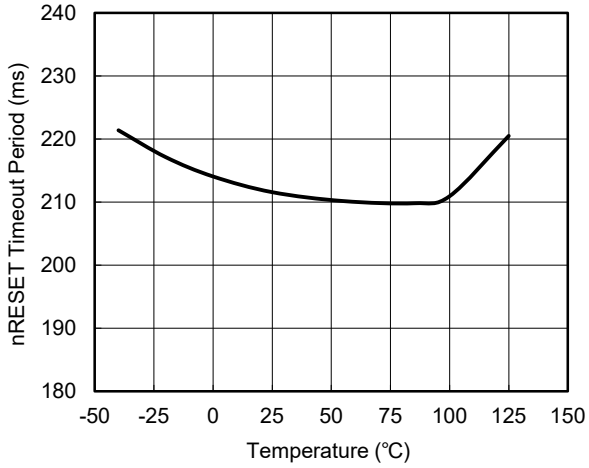
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range (V_{CC})				1		5.5	V
Supply Current (I_{SUPPLY})		V_{CC} = 3.3V			0.64	1.60	μA
		V_{CC} = 5.5V			0.77	1.80	
nRESET Threshold (V_{nRST})		SGM823A-Y	T_J = +25℃	2.155	2.195	2.235	V
			T_J = -40℃ to +85℃	2.150	2.195	2.240	
			T_J = -40℃ to +125℃	2.105	2.195	2.285	
		SGM823A-W	T_J = +25℃	1.640	1.675	1.710	
			T_J = -40℃ to +85℃	1.635	1.675	1.715	
			T_J = -40℃ to +125℃	1.590	1.675	1.760	
		SGM823A-V	T_J = +25℃	1.550	1.585	1.620	
			T_J = -40℃ to +85℃	1.545	1.585	1.625	
			T_J = -40℃ to +125℃	1.515	1.585	1.655	
nRESET Threshold Hysteresis (V_{HYS})		SGM823A-Y			11		mV
		SGM823A-W			8		
		SGM823A-V			8		
nRESET Threshold Temperature Coefficient		T_J = -40℃ to +85℃			20		ppm/℃
nRESET Pulse Width (t_{RP})				120	200	300	ms
nRESET Output Voltage	V_{OH}	V_{CC} ≥ 1.8V, I_{SOURCE} = 200μA, reset not asserted		0.8 × V_{CC}			V
		V_{CC} ≥ 3.15V, I_{SOURCE} = 500μA, reset not asserted		0.8 × V_{CC}			
		V_{CC} ≥ 4.75V, I_{SOURCE} = 800μA, reset not asserted		0.8 × V_{CC}			
	V_{OL}	V_{CC} ≥ 1.0V, I_{SINK} = 50μA, reset asserted				0.3	
		V_{CC} ≥ 1.2V, I_{SINK} = 100μA, reset asserted				0.3	
		V_{CC} ≥ 2.55V, I_{SINK} = 1.2mA, reset asserted				0.3	
		V_{CC} ≥ 4.25V, I_{SINK} = 3.2mA, reset asserted				0.4	
V_{CC} to Reset Delay (t_{RD})		V_{nRST} - V_{CC} = 100mV			90		μs
Watchdog Timeout Period (t_{WD})				1.1	1.6	2.4	s
WDI Pulse Width (t_{WP})		V_{IL} = 0V, V_{IH} = V_{CC}		90			ns
WDI Input Threshold	Low	V_{CC} = 5.5V				0.8	V
	High	V_{CC} = 5.5V		3.5			
	Low	$V_{nRST(MAX)}$ < V_{CC} < 3.3V				0.6	
	High	$V_{nRST(MAX)}$ < V_{CC} < 3.3V		0.7 × V_{CC}			
WDI Input Current		WDI = V_{CC}, time average			0.01	0.5	μA
		WDI = 0V, time average		-0.5	-0.01		
nMR Input Voltage	V_{IL}					0.6	V
	V_{IH}			0.7 × V_{CC}			
nMR Pulse Width (t_{MR})				300			ns
nMR Noise Immunity (Pulse Width with No Reset)					130		ns
nMR to nRESET Out Delay (t_{MD})						550	ns
nMR Pull-Up Resistance (Internal)				40	65	90	kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

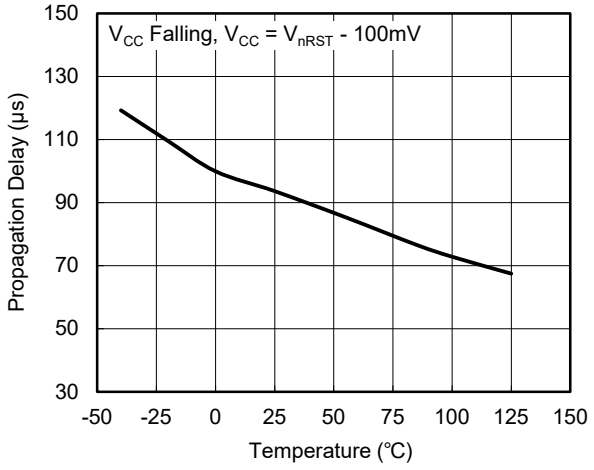
Supply Current vs. Temperature



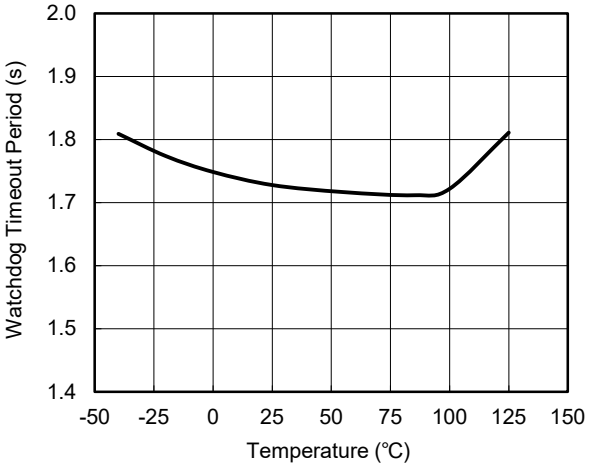
nRESET Timeout Period vs. Temperature



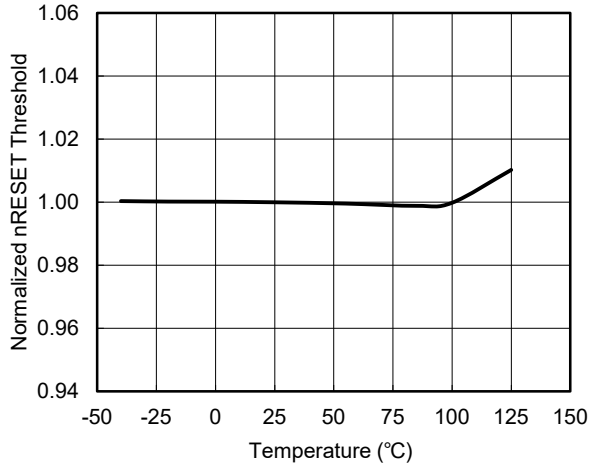
V_{CC} to nRESET Propagation Delay vs. Temperature



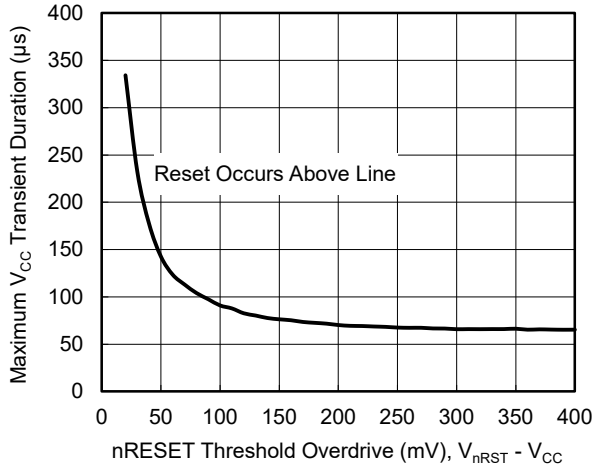
Watchdog Timeout Period vs. Temperature



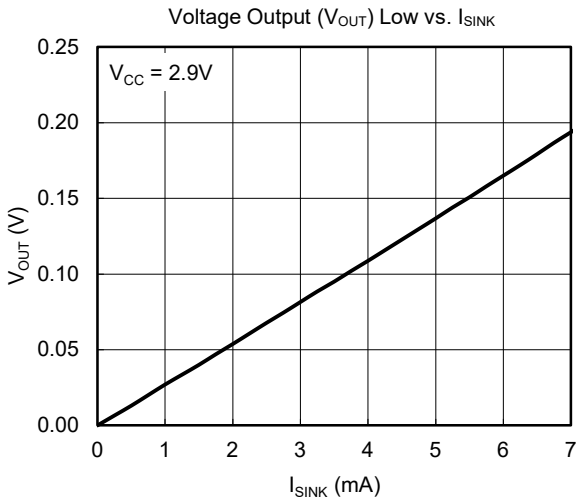
Normalized nRESET Threshold Voltage vs. Temperature

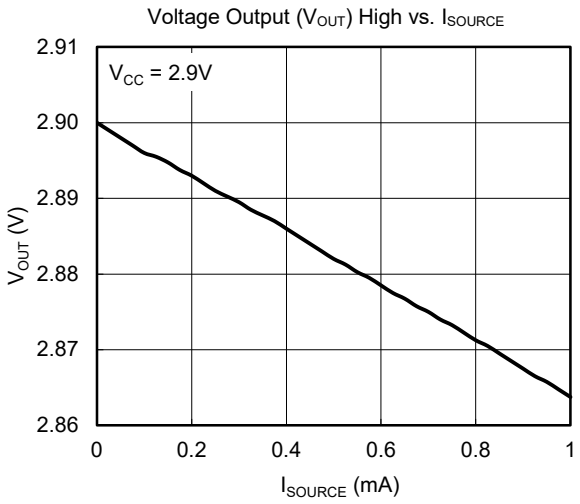


Maximum V_{CC} Transient Duration vs. nRESET Threshold Overdrive

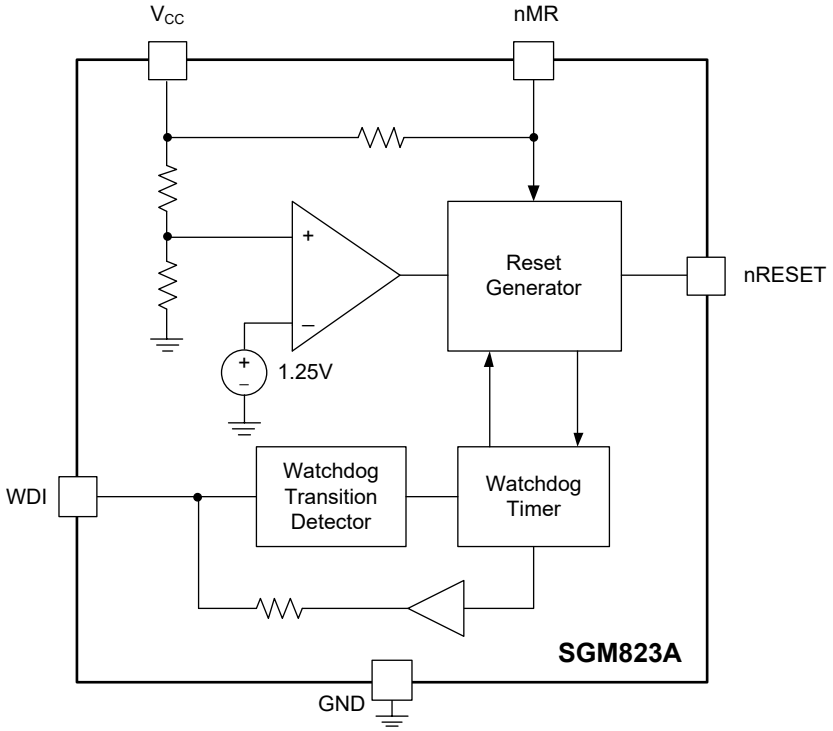


TYPICAL PERFORMANCE CHARACTERISTICS (continued)





FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

nRESET Output

The reset input of a microprocessor (μP) initiates it to a known state. The SGM823A supervisory circuit asserts a reset to the supervised μP to prevent the code-execution errors that may occur due to power-up, power-down, brownout conditions or other transients. The nRESET output is still in the correct logic state even if V_{CC} is lower than 1V. During power-up, when V_{CC} exceeds the rising threshold voltage (V_{nRST} + V_{HYS}), an internal timer keeps nRESET in low state for the reset timeout period (t_{RP}) before nRESET returns to the high state (Figure 1).

If V_{CC} drops below the falling threshold voltage (V_{nRST}) (a brownout condition occurs), a reset is asserted and nRESET goes low. In general, nRESET remains low for the t_{RP} (200ms, TYP) period every time after the last event. So, if during the low period of nRESET, V_{CC} goes up and dips below V_{nRST} again, the internal timer will restart for a new t_{RP} period. The nRESET output can source and sink current.

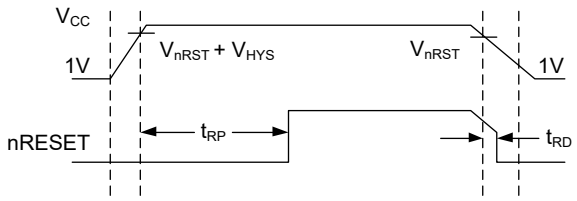


Figure 1. nRESET Timing Diagram

Manual Reset Input

Many μP-based products need manual-reset capability to let the operator or an external logic reset the μP. For the SGM823A, applying a logic low to the nMR input, asserts a reset (nRESET = low). nRESET remains low while nMR is low, and will stay low for the t_{RP} (200ms, TYP) period after nMR returns to high state. The nMR input is internally pulled up by a 65kΩ resistor and can be left floating if not used. It can be driven by a CMOS/TTL logic or by a switch shorting to GND. A normally open momentary switch connected between nMR and GND pins can be used as a manual reset. Switch debouncing is not needed. However, if long cables are used to drive the nMR input or if the environment is noisy, connect a 0.1μF capacitor between nMR and GND to immune the additional noise.

Watchdog Input

The internal watchdog circuit monitors the μP's activity by checking the WDI input. If the μP does not toggle the WDI within the watchdog t_{WD} (1.6s, TYP) period, nRESET will send a low pulse to reset the μP. So, the code should be written such that successive toggles on WDI occur in periods not longer than the lowest t_{WD} time to reset the internal watchdog timer and prevent μP reset when the code is running normally. The watchdog timer is cleared by either toggling WDI or by a pulse with a duration as short as 90ns. While the reset is asserted and nRESET is low, the watchdog timer is cleared and timer does not count. It starts counting when the reset is released and nRESET goes high (Figure 2).

To disable the watchdog function, leave the WDI pin open. If WDI is driven by a 3-state buffer, set it to the Hi-Z state. In this case the buffer leakage current should not exceed 10μA. The maximum capacitance seen on the WDI pin should be less than 200pF to assure that watchdog remains disabled. The watchdog input is internally oscillating when it is left open to clear the watchdog timer and prevent it from generating a reset. It is driven low during the first 7/8 of the watchdog timeout period and driven high in the last 1/8 of that. For example if WDI input is open and the watchdog timeout is 1.6s, the watchdog timer will automatically clear every 1.4s and reset will not occur.

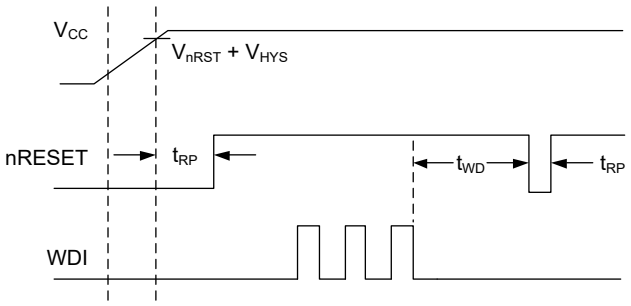


Figure 2. Watchdog Timing Relationship

APPLICATION INFORMATION

Using SGM823A with Microprocessors with Bidirectional Reset Pins

Some microprocessors can internally force their reset pins low to assert a reset (bidirectional reset pins). The low pull-up current of the SGM823A allows using of them along with the microprocessors with bidirectional resets like the 68HC11. The microprocessor can force nRESET low when nRESET is pulled high by the SGM823A with no issues (Figure 3).

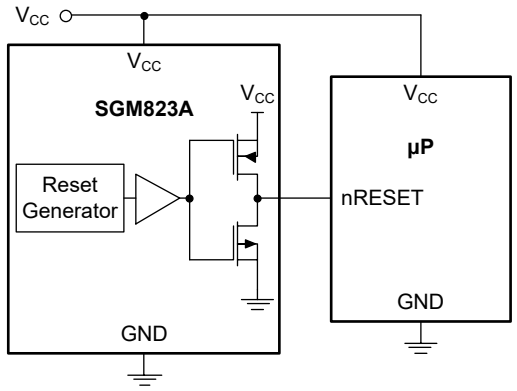


Figure 3. Interfacing to µP with Bidirectional Resets

Negative-Going V_{CC} Transient Immunity

The SGM823A has the ability to immune short time and negative V_{CC} transients or even glitches. It does not need to shut down the entire system. Resets are applied to the microprocessor during power-up, power-down and brownout conditions and not when an insignificant V_{CC} transient occurs.

A 0.1µF ceramic capacitor is recommended between the V_{CC} and GND pin to reduce the input supply noise.

Watchdog Input Current

The WDI input is internally driven by a buffer and series resistor from an internal counter chain stage of the watchdog. Therefore, when WDI is open, the watchdog timer is automatically cleared before timeout (by an internal low-high-low pulse).

To get the minimum WDI input current (minimum power loss), keep WDI low for the majority of the timeout period and send a high pulse at the first 7/8 of the timeout period for clearing the watchdog timer.

Watchdog Software Considerations

To have a more effective watchdog in software monitoring, rather than generating pulses by a code segment, set and reset the WDI input at different points of the program code. For example, set it in the main program and reset it in a periodic timing interrupt. For example, if WDI is toggled within an unwanted infinite loop, it will continuously reset watchdog as a normal condition and the processor is not reset.

An example of a watchdog flow is shown in Figure 4. The WDI is set high at the start of the program, and is set low at the start of every subroutine or loop, then is set high again when the program returns to the start. If the processor hangs in any subroutine, the WDI toggling will not occur and the watchdog will reset the processor and correct the situation.

The nRESET output may also be connected to an interrupt input of the µP for a corrective action if preferred.

Note that such watchdog control schemes may not be optimal if the total power consumption is critical as discussed in the Watchdog Input Current section.

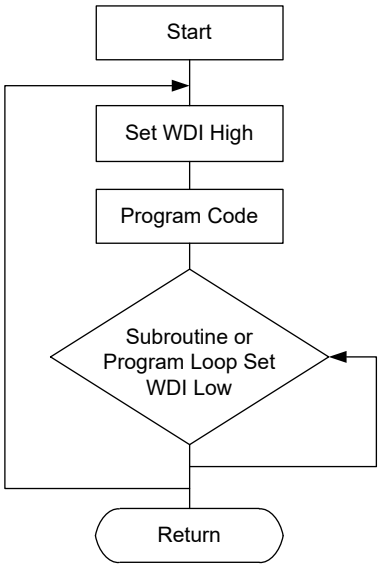


Figure 4. Watchdog Flow Diagram

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JUNE 2026 – REV.A.2 to REV.A.3	Page
Updated Absolute Maximum Ratings section	2
Updated Pin Description section	3

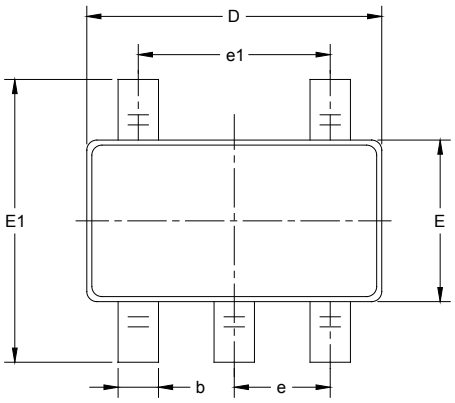
JULY 2022 – REV.A.1 to REV.A.2	Page
Updated Application Information section	9

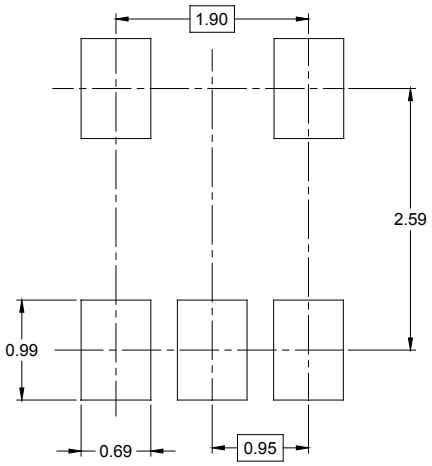
OCTOBER 2020 – REV.A to REV.A.1	Page
Added 2.19V Reset Threshold	1, 2, 4

Changes from Original to REV.A (JULY 2020)	Page
Changed from product preview to production data	All

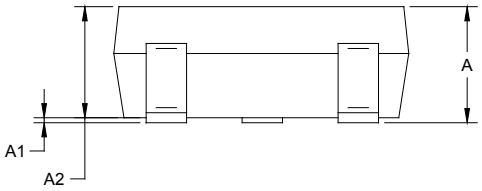
PACKAGE OUTLINE DIMENSIONS

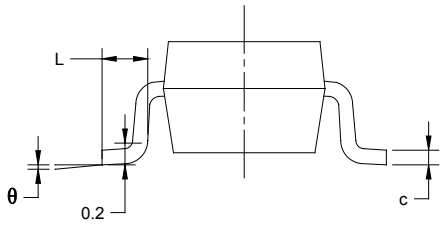
SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)

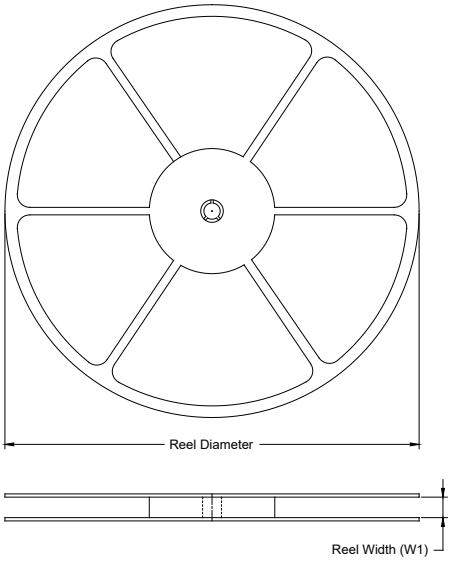




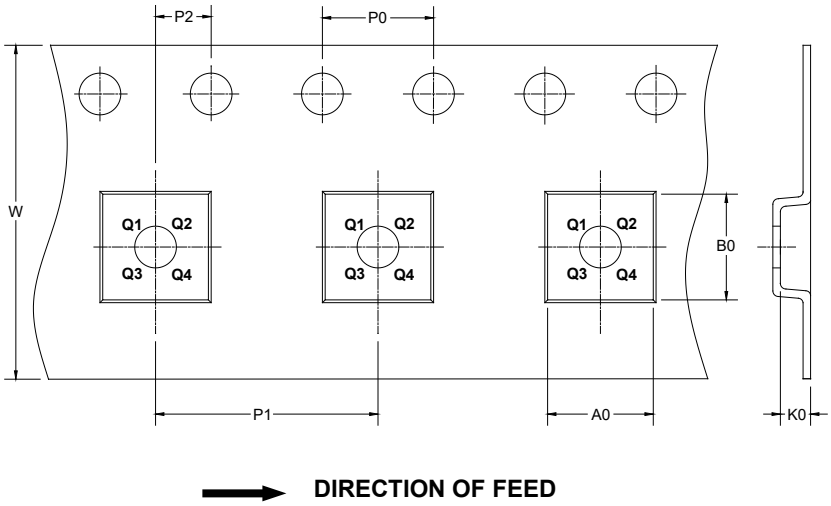
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



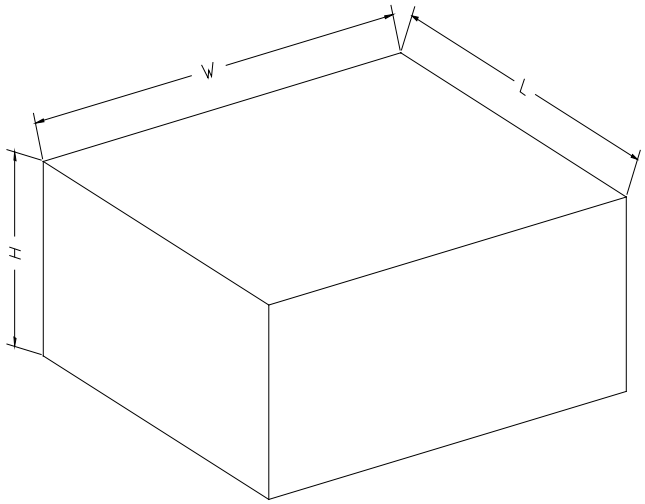
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7″	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002