SGM61234
28V, 2A, 5V Fixed Output, Non-Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61234 is a 5V fixed output, non-synchronous Buck converter with a wide input voltage range from 6.5V to 28V and 2A output current capability. This device uses peak current mode control with slope compensation. Pulse skip mode (PSM) feature is included to reduce losses at the light loads.

The switching frequency is adjustable from 50kHz to 1.1MHz with an external resistor (R_T). Spread spectrum technique is used for the switching frequency to avoid high power peaks in EMI. For further reduction of the EMI, an anti-ringing circuit is added on the switching node (SW) to damp the oscillations in DCM.

Natural cycle-by-cycle current limit and an included frequency foldback mechanism protect the device against over-current and short-circuit faults. Thermal shutdown protection is also provided to save the device if the junction temperature reaches +170℃.

The SGM61234 is available in the Green SOIC-8 and SOIC-8 (Exposed Pad) packages.

FEATURES

- **Wide 6.5V to 28V Input Voltage Range**
- **5V Fixed Output Voltage**
- **2A Maximum Continuous Output Current**
- **PSM Feature for Improved Light Load Efficiency**
- **Peak Current Mode Control**
- **Cycle-by-Cycle Over-Current Protection**
- **Frequency Foldback Output Short Protection**
- **50kHz to 1.1MHz Adjustable Switching Frequency**
- **120kHz Default Frequency (No Set Resistor)**
- **Spread Spectrum to Reduce EMI Peaks**
- **Switching Node Anti-Ringing for EMI Reduction**
- **Adjustable Soft-Start**
- **Available in the Green SOIC-8 (Exposed Pad) and SOIC-8 Packages**

APPLICATIONS

Home Appliances
Distributed Power Systems
CPE Equipment
Set-Top Boxes
LCD Displays
Battery Chargers

SIMPLIFIED SCHEMATIC

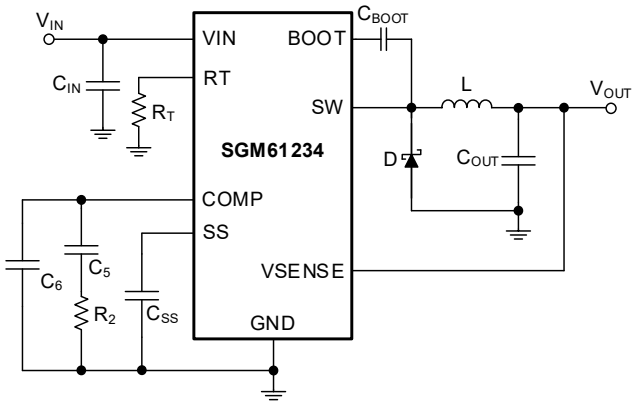


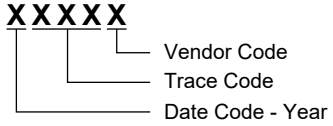
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61234	SOIC-8 (Exposed Pad)	-40℃ to +125℃	SGM61234XPS8G/TR	SGM 61234XPS8 XXXXX	Tape and Reel, 4000
	SOIC-8	-40℃ to +125℃	SGM61234XS8G/TR	SGM 61234XS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN, SW Voltages ..... -0.3V to 30V
SW (Maximum withstand Voltage Transient < 20ns) ..... -5V to 30V
BOOT to SW Voltage ..... -0.3V to 6V
VSENSE Voltage ..... -0.3V to 6V
RT, COMP Voltages ..... -0.3V to 3V
SS Voltage ..... -0.3V to 5V
Package Thermal Resistance
SOIC-8 (Exposed Pad), θ_{JA} ..... 52℃/W
SOIC-8, θ_{JA} ..... 111℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±3000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 6.5V to 28V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

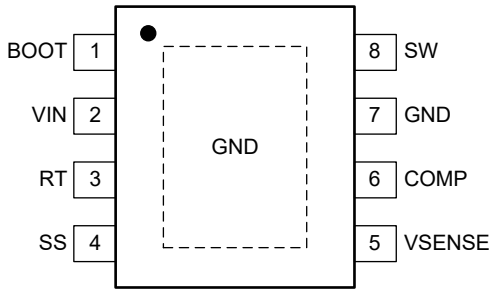
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

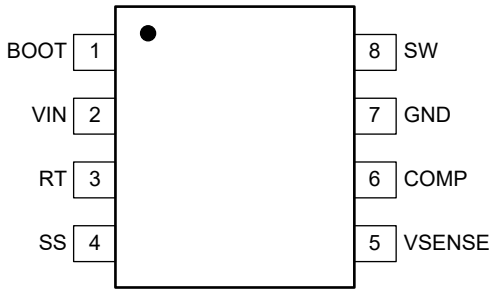
PIN CONFIGURATIONS

(TOP VIEW)



SOIC-8 (Exposed Pad)

(TOP VIEW)



SOIC-8

PIN DESCRIPTION

PIN		NAME	I/O	FUNCTION
SOIC-8 (Exposed Pad)	SOIC-8			
1	1	BOOT	O	Bootstrap Pin to Supply the Internal MOSFET Gate Driver. Place a 0.1μF bootstrap capacitor (C_{BOOT}) between the BOOT and SW pins.
2	2	VIN	P	Power Supply Input with 6.5V to 28V Range and 3.4V (TYP) UVLO Threshold.
3	3	RT	I	Input Pin for Setting the Switching Frequency. Place a programming resistor between this pin and GND to set the switching frequency from 50kHz to 1.1MHz. If this pin is left floating, f_{SW} will be set to 120kHz and if it is shorted to GND, the f_{SW} will be around 70kHz.
4	4	SS	I	Soft-Start Time Adjustment Pin. Place an external capacitor (C_{SS} < 27nF) between this pin and GND to adjust the output ramp-up time (10% to 90%) from 1ms to 10ms based on the following equation. A 2μA current source charges the external capacitor (V_{REF} = 0.8V). $t_{SS}\ (ms) = \frac{C_{SS}\ (nF) \times V_{REF}\ (V)}{I_{SS}\ (\mu A)}$
5	5	VSENSE	I	Output Voltage Feedback Input Pin. Connect this pin to the output regulation point.
6	6	COMP	O	Transconductance Error-Amplifier Output and the Input to the PWM Comparator. A frequency compensation network is placed between this pin and GND. The COMP pin voltage (V_{COMP}) determines the required output current for the PWM regulation.
7	7	GND	G	Ground Pin.
8	8	SW	P	Converter Switching Node. It connects to the external power diode cathode pin, the external inductor switching terminal and one terminal of the bootstrap capacitor.
Exposed Pad	—	GND	G	Exposed Pad. It helps cooling the device junction and must be connected to GND pin for proper operation.

NOTE: I = Input, O = Output, P = Power, G = Ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

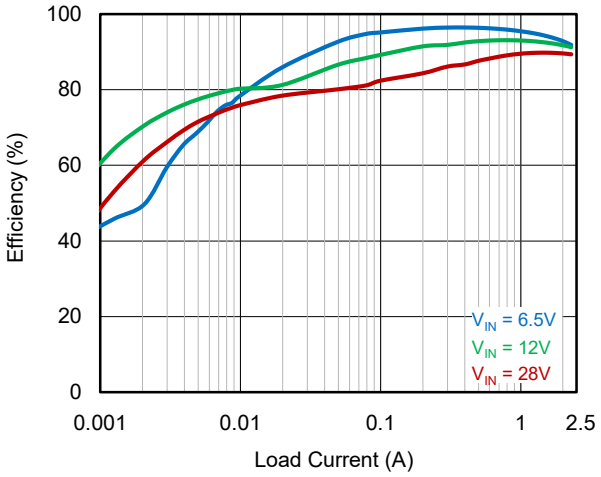
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply						
Input Voltage Range	V_{IN}	T_J = +25℃	6.5		28	V
Non-Switching Quiescent Supply Current	I_{DDQ_NSW}	V_{SENSE} = 6V, not switching		105		μA
VIN Under-Voltage Lockout	V_{UVLO}	Rising V_{IN}		3.4		V
		Hysteresis		220		mV
Feedback and Error Amplifier						
Regulated Output Voltage	V_{SENSE}	V_{IN} = 12V	4.87	5.02	5.23	V
Error Amplifier Transconductance (1)	G_{m_EA}	-2μA < I_{COMP} < 2μA, V_{COMP} = 1V		92		μA/V
Error Amplifier Source/Sink Current (1)	I_{gm}	V_{COMP} = 1V, with 100mV overdrive		±7		μA
Inductor Current to Comp Voltage Gain G_m (1)	G_{m_SRC}	V_{IN} = 12V		9		A/V
PSM and Soft-Start						
Switch Current Threshold to Enter Pulse Skip Mode	I_{TH}	V_{IN} = 12V		200		mA
SS Pin Charge Current Source	I_{SS}			2		μA
Internal Switching Oscillator						
Switching Frequency Range	f_{SW_BK}	Set by external resistor R_T, T_J = +25℃	50		1100	kHz
Programmable Frequency	f_{SW}	R_T = open		120		kHz
		R_T = short		70		
		R_T = 85.5kΩ		340		
Frequency Spread Spectrum in % of f_{SW}	f_{JITTER}	V_{IN} = 12V		±6		%
Jittering Swing Frequency	f_{SWING}	V_{IN} = 12V		f_{SW}/512		kHz
MOSFET Switch Minimum On-Time	t_{MIN_ON}	V_{IN} = 12V		200		ns
Maximum Duty Cycle	D_{MAX}	V_{IN} = 12V		93		%
Current Limit						
Peak Inductor Current Limit	I_{LIMIT}	V_{IN} = 12V		4.2		A
MOSFET						
On-Resistance	R_{DSON_HS}	V_{IN} = 12V		125	265	mΩ
Thermal Shutdown						
Thermal Shutdown Trip Temperature	T_{TRIP}	Rising temperature		170		℃
Thermal Shutdown Hysteresis	T_{HYS}			35		℃

NOTE:
1. Guaranteed by design. Not production tested.

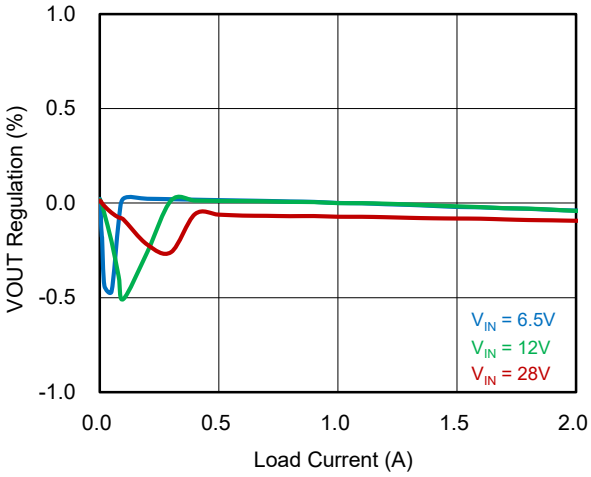
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 15μH, f_{SW} = 340kHz, unless otherwise noted.

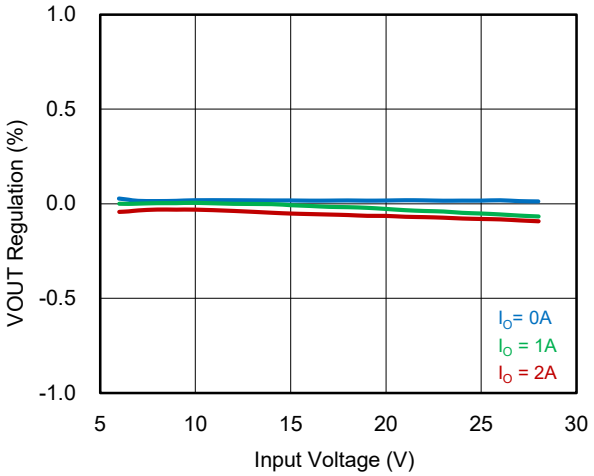
Efficiency



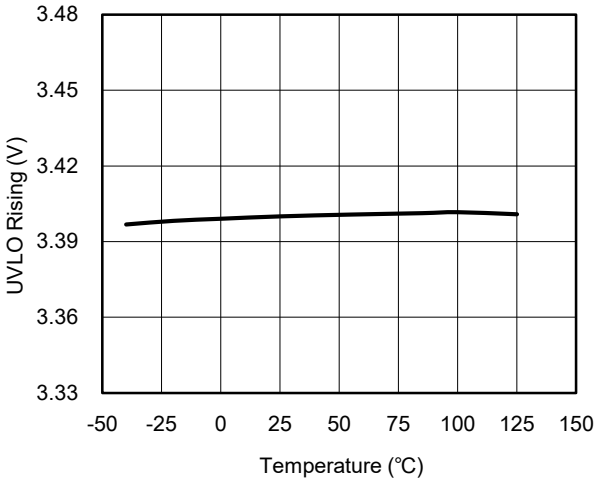
Load Regulation



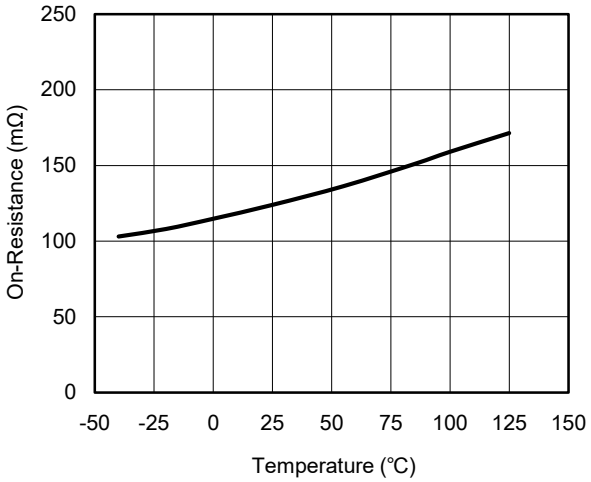
Line Regulation



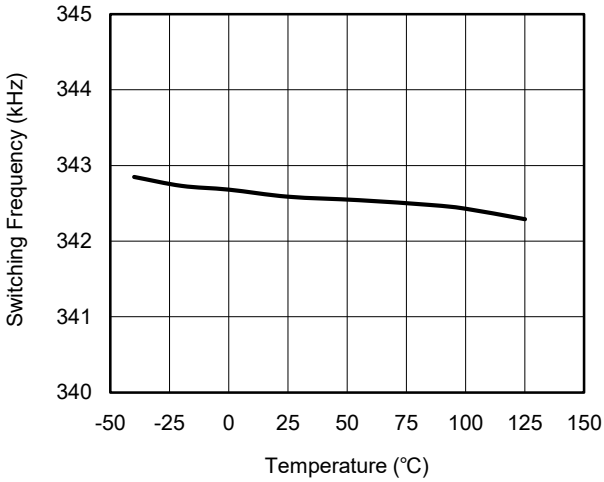
UVLO Rising vs. Temperature



On-Resistance vs. Temperature



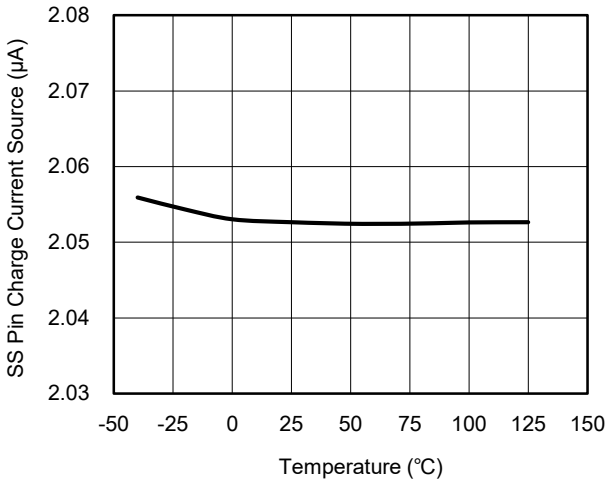
Switching Frequency vs. Temperature



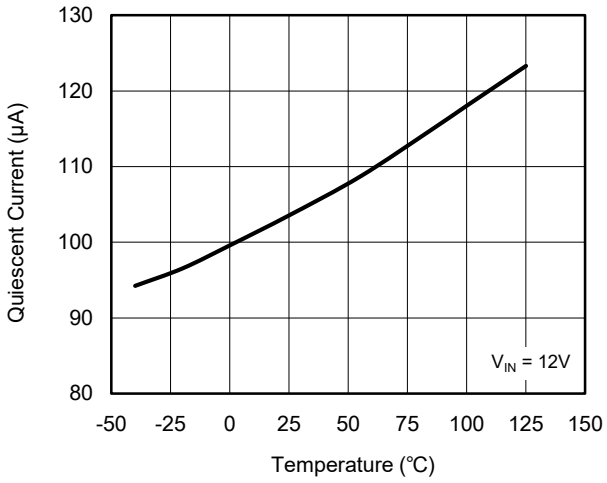
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 15μH, f_{SW} = 340kHz, unless otherwise noted.

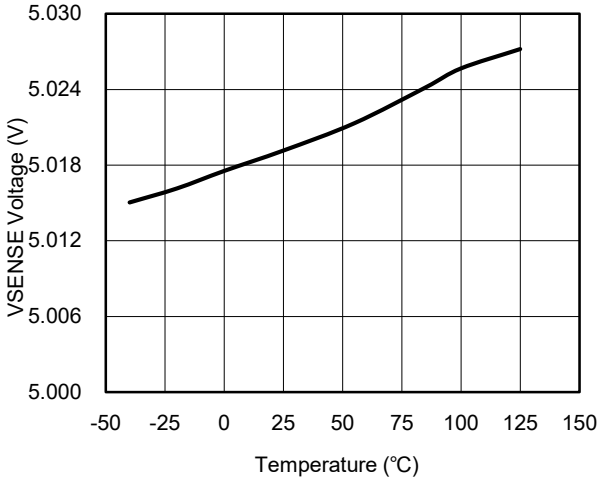
SS Pin Charge Current Source vs. Temperature



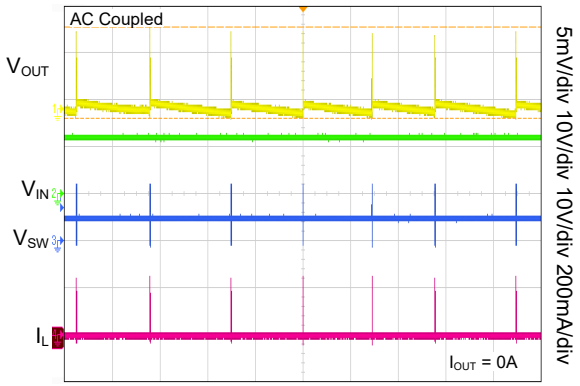
Quiescent Current vs. Temperature



VSENSE Voltage vs. Temperature

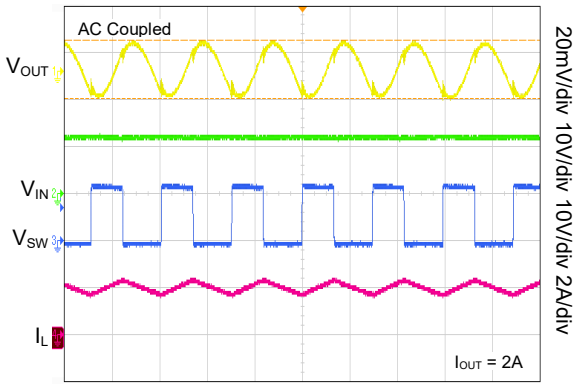


Output Voltage Ripple



Time (1ms/div)

Output Voltage Ripple

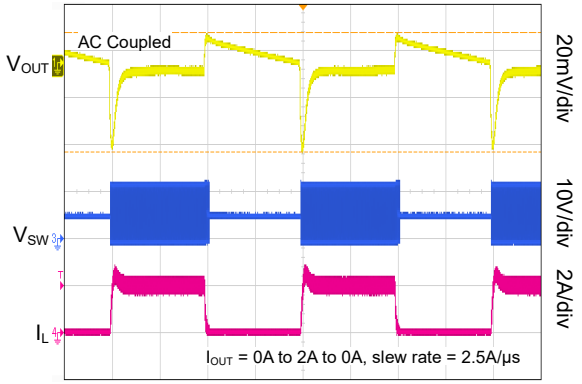


Time (2μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

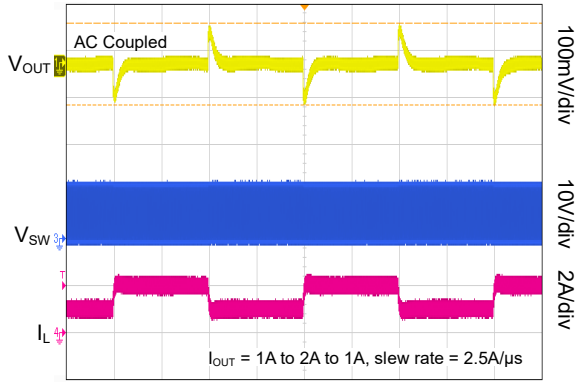
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 15μH, f_{SW} = 340kHz, unless otherwise noted.

Load Transient



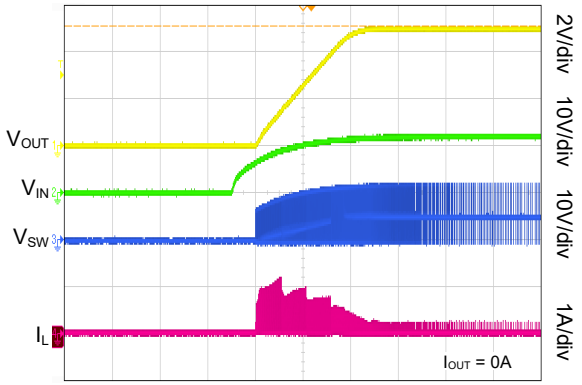
Time (1ms/div)

Load Transient



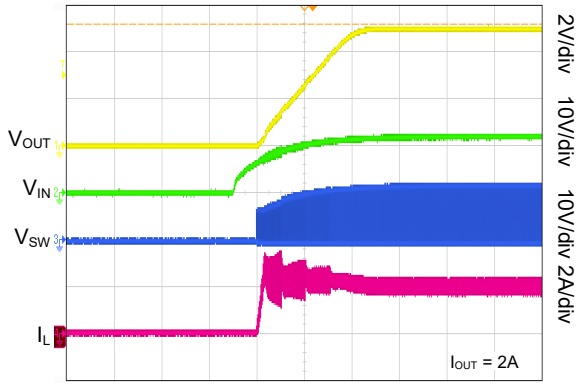
Time (1ms/div)

Power On



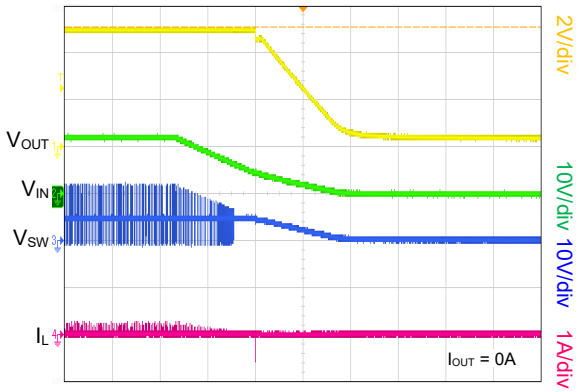
Time (2ms/div)

Power On



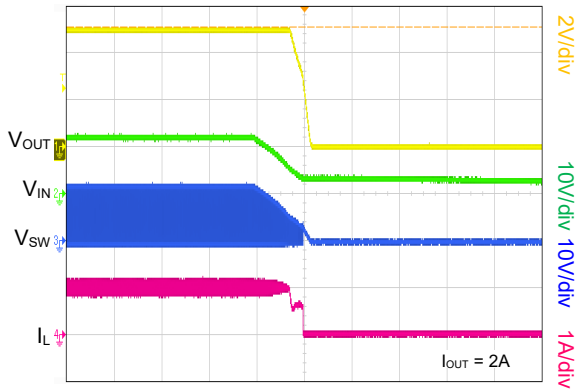
Time (2ms/div)

Power Off



Time (2ms/div)

Power Off

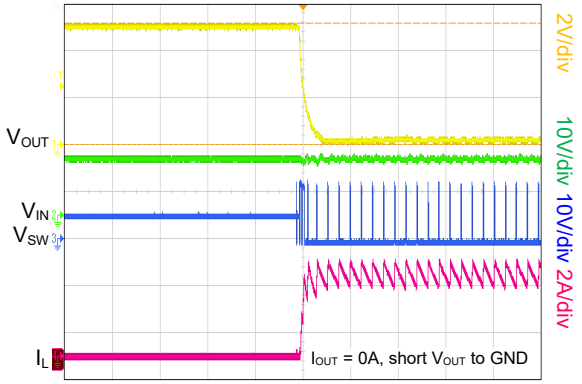


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

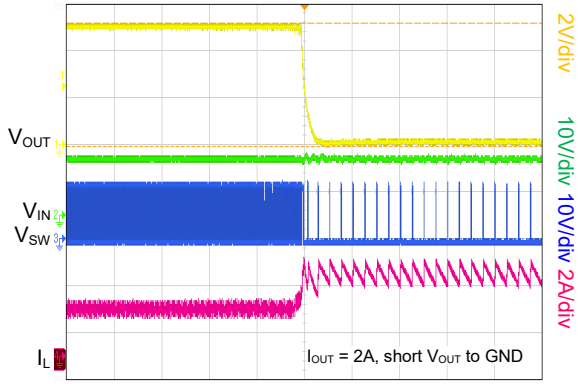
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 15μH, f_{SW} = 340kHz, unless otherwise noted.

SCP Entry



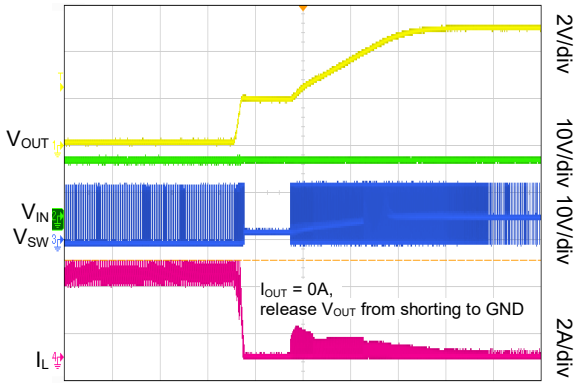
Time (100μs/div)

SCP Entry



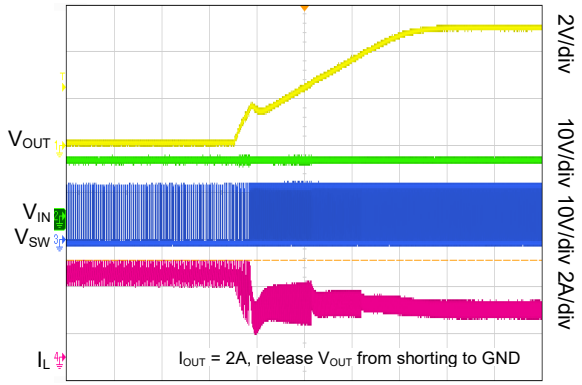
Time (100μs/div)

SCP Recovery



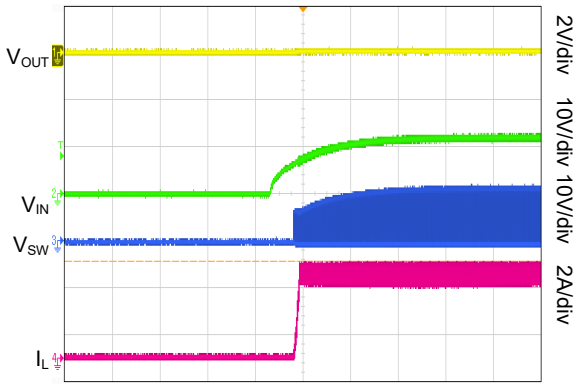
Time (1ms/div)

SCP Recovery



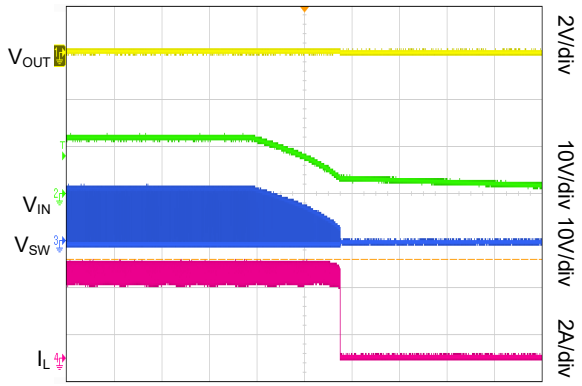
Time (1ms/div)

VIN Power On during SCP



Time (2ms/div)

VIN Power Off during SCP

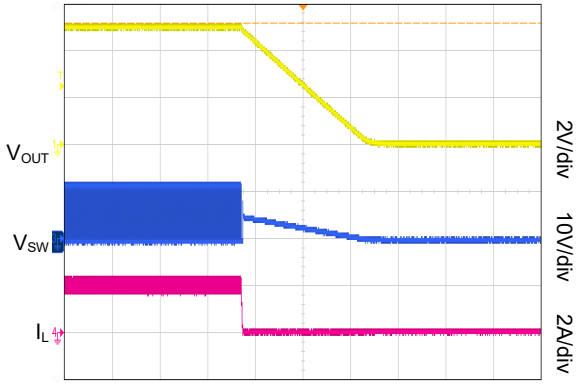


Time (20ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

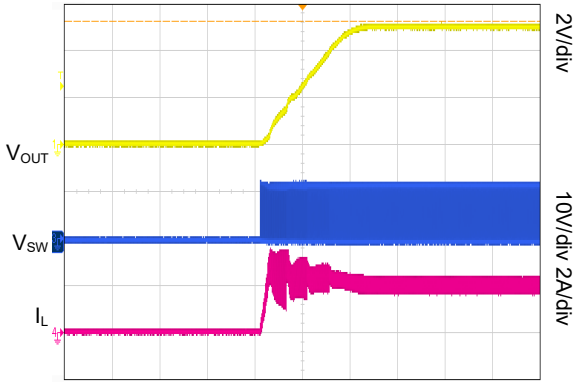
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 15μH, f_{SW} = 340kHz, unless otherwise noted.

Thermal Shutdown Entry



Time (200μs/div)

Thermal Shutdown Recovery



Time (2ms/div)

FUNCTIONAL BLOCK DIAGRAM

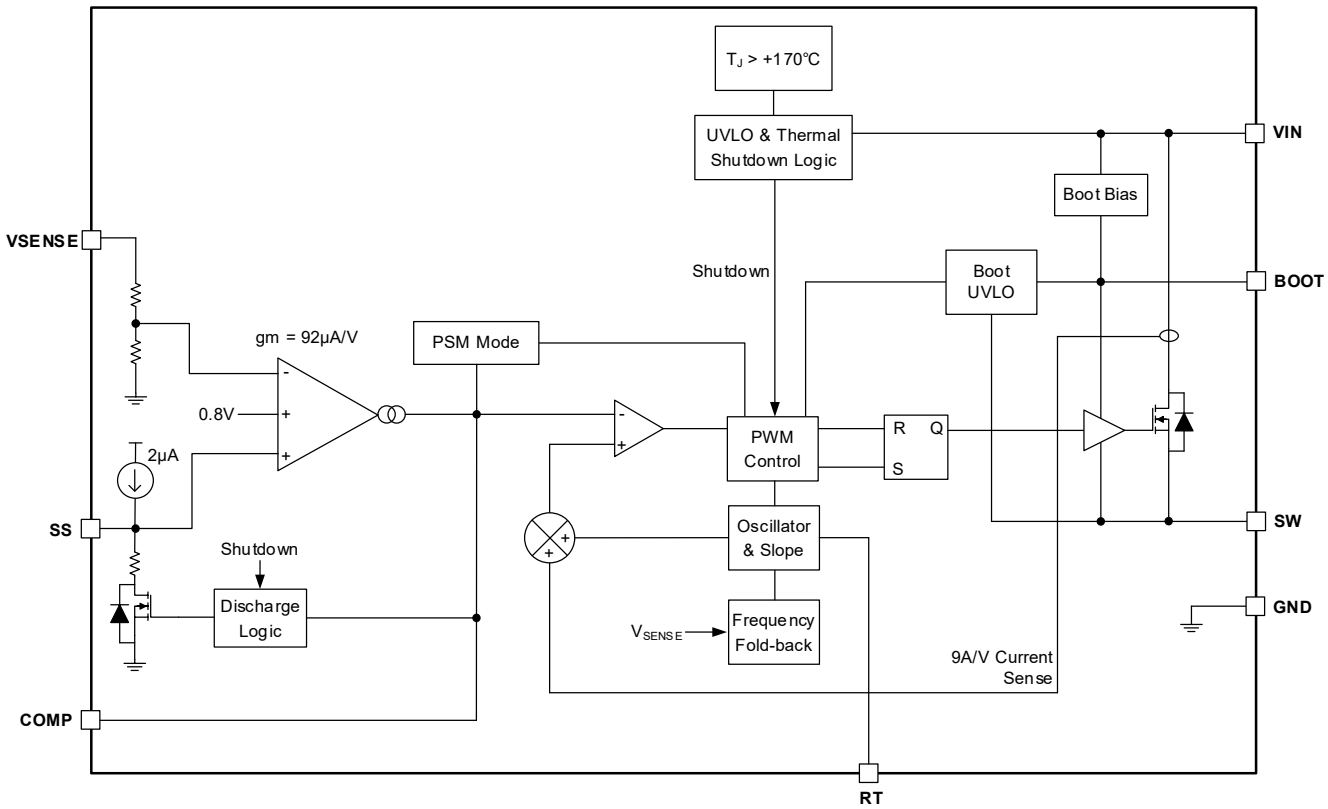


Figure 2. SGM61234 Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61234 is a fixed 5V output Buck converter with a wide input voltage range from 6.5V to 28V and 2A continuous output current capability. It is a non-synchronous regulator and requires an external high frequency power diode to complete the converter. The integrated high-side switch (HS) is a 125mΩ N-MOSFET. This device operates at fixed frequency (with spread spectrum jittering) and uses current mode control for better line and load transient responses. These features allow reduced output capacitance and simple compensation network.

An external resistor connected between the RT pin and GND sets the switching frequency. If the R_T is open, the default switching frequency is 120kHz.

Switching can start when V_{IN} exceeds 3.4V. The no switching quiescent current is 105μA.

The diode for recharging the external bootstrap capacitor (C_{BOOT}) is integrated. The bootstrap circuit provides the supply voltage for driving the N-MOSFET that needs to be higher than V_{IN}.

The soft-start time can be set by an external capacitor (C_{SS}) placed between SS and GND pins. Adjustable soft-start time provides more flexibility in selection of the output filter.

Light load losses are reduced when the inductor peak current falls below 200mA (TYP) and the device enters in its unique pulse skip mode (PSM).

The peak current control naturally limits the current in each cycle. However it may not be sufficient during startup or an over-current event. The frequency foldback feature reduces the switching frequency to give enough time to the controller for limiting the inductor current, especially in short-circuit conditions.

Thermal shutdown is an additional protection for the device against overheating caused by the faults.

Switching Frequency

The external resistor between the RT and GND sets the switching frequency (Equation 1) as shown in Figure 3. If R_T is shorted, f_{SW} = 70kHz, and if it is open, f_{SW} = 120kHz. For f_{SW} = 340kHz, set R_T = 85.5kΩ.

$$R_T\left(k\Omega\right) = 25.5 \times f_{SW}\left(MHz\right)^{-1.12} \quad (1)$$

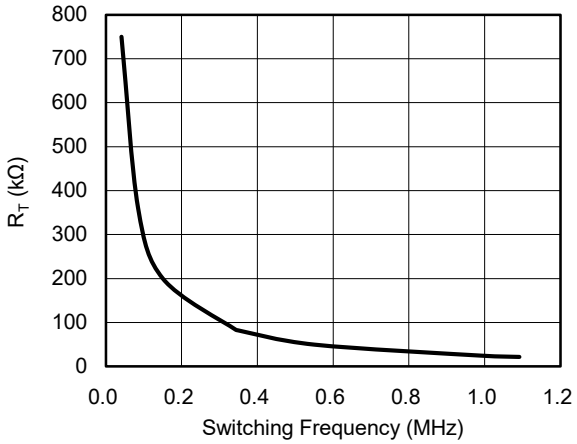


Figure 3. R_T and Switching Frequency Relationship

Bootstrap Voltage (BOOT)

To power the upper switch gate driver, a voltage higher than V_{IN} is needed. Bootstrap technique is used to provide this voltage from the switching node by using a 0.1μF bootstrap capacitor between SW and BOOT pins along with an internal bootstrap diode.

SS Pin and Soft-Start Adjustment

It is recommended to add a soft-start capacitor (C_{SS}) between SS pin and GND to set the soft-start time between 1ms to 10ms for a proper startup. The lower of the SS voltage (V_{SS}) and V_{REF} is applied to the error amplifier to regulate the output. The internal I_{SS} = 2μA current charges the C_{SS} and provides a linear voltage ramp on the SS pin. Use Equation 2 to calculate the soft-start time (10% to 90% rise). It is recommended that C_{SS} be less than 27nF. (V_{REF} = 0.8V).

$$t_{ss}\ (ms) = \frac{C_{SS}\ (nF) \times V_{REF}\ (V)}{I_{SS}\ (\mu A)} \quad (2)$$

Error Amplifier (EA)

This device uses a transconductance error amplifier (EA) to compare the sensed output voltage (V_{SENSE}) and the internal reference. The gain of EA amplifier in normal operation is 92μA/V. The output current is injected into the frequency compensation network (between COMP and GND pins) to produce the control signal (V_{COMP}) for the PWM comparator.

Slope Compensation

Without slope compensation, when the duty cycle is above 50%, the PWM pulse-widths will be unstable with subharmonic oscillation. To avoid such oscillations in the SGM61234, a compensation ramp is added to the measured switch current before it is compared with the control signal by the PWM comparator.

DETAILED DESCRIPTION (continued)

Pulse Skip Mode (PSM)

To improve light load efficiency, the pulse skip mode (PSM) feature is included in the SGM61234. The device enters in PSM if V_{COMP} < 0.65V (TYP) at light load (the peak inductor current falls below 200mA at V_{IN} = 12V). In PSM, the COMP voltage is internally clamped at 0.65V to inhibit MOSFET from switching. The device can exit PSM if V_{COMP} rises above the clamp level. Since the peak inductor current is the sensed parameter for entering the PSM, the actual load current (DC) threshold for PSM will depend on the output filter.

Over-Current and Frequency Foldback

Over-current protection (OCP) is naturally provided by current mode control. In each cycle, the control voltage (V_{COMP}) is compared with the sensed switch current (that is equivalent to the inductor current during on-time) and when the peak inductor current reaches to the control signal level, the switch is turned off. This technique reduces the duty cycle and hence the output voltage in the over-current conditions. Normally, if the output voltage drops, the EA will increase V_{COMP} to expand the duty cycle and increase the output current to bring the output back to regulation. However, the COMP pin has an internal maximum clamp and cannot request more than a certain level of current for the output. In other words, the OCP current limit is determined by the COMP pin clamp voltage.

The natural OCP in the peak current mode control may not be able to provide a complete protection when an output short-circuit occurs, so an extra protection for short-circuit is needed. During an output short, inductor current may runaway above over-current limits. Current runaway can saturate the inductor and the current may increase until the device is damaged. It occurs since the inductor current cannot reset (volt-second balance) during the off-times. During an output-short, only the small negative diode forward voltage appears across the inductor in the off-time. Note that the minimum on-time is limited, and in each cycle, all input voltage appears on the inductor during the minimum on-time. The circuit delays and reaction times make these conditions even worse, and in each cycle the current is increased to a higher level. In the SGM61234 this problem is effectively solved by increasing the off-time by reducing the switching frequency which is called frequency foldback. As the V_{SENSE} voltage falls from 5V to 0V, the frequency will be divided by 1, 2, 4, and 8 depending on the drop as shown in Table 1.

Table 1. Frequency Foldback with V_{OUT} Drop

Switching Frequency	VSENSE Pin Voltage
f_{SW}	V_{SENSE} ≥ 3.75V
$f_{SW}/2$	3.75V > V_{SENSE} ≥ 2.5V
$f_{SW}/4$	2.5V > V_{SENSE} ≥ 1.25V
$f_{SW}/8$	1.25V > V_{SENSE}

Spread Spectrum Switching

Spread spectrum technique is used in the SGM61234 to flatten the generated EMI spectrum and reduce the large EMI peaks. The switching frequency is periodically varied between -6% and +6% of the nominal value at the jittering frequency of $f_{SW}/512$.

Anti-Ringing at the Switching Node

A high-Q LC resonant circuit is formed by the filter inductor and the parasitic capacitances (such as diode) at the switching node. In DCM, the parasitic energy stored in the parasitic elements causes high frequency oscillations (ringing) on the SW pin after the diode is turned off. This ringing is not quickly damped due to the high-Q (low loss) resonance. The high frequency ringing may radiate EMI at levels that is not acceptable in some systems. To stop such oscillations, an anti-ringing circuit that includes an auxiliary MOSFET between SW and VSENSE pins is integrated in the device. This switch is turned on when the inductor current crosses zero and the SW voltage starts to rise above V_{SENSE}. This will kill the ringing by shorting those two pins that increases the damping (reduces Q).

Over-Voltage Transient Protection (OVTP)

When an overload or an output fault condition is cleared, large overshoot voltages may appear on the output. The SGM61234 includes a protection circuit to reduce such over-voltage transients. If the VSENSE voltage exceeds 108% of the V_{REF} threshold, the HS MOSFET is turned off and when it returns below 105% of the V_{REF}, the HS MOSFET is released for turn-on.

Thermal Shutdown

If the device junction temperature exceeds +170℃, the thermal shutdown protection trips the device, and the switching will stop. When the temperature falls below +135℃, the device will automatically recover with a power-up and soft-start sequence.

APPLICATION INFORMATION

Input Capacitor Design

It is recommended to use at least a 10μF X5R or better ceramic capacitor between VIN and GND pins, placed as close as possible to the device. The converter AC (RMS) input current that is given in Equation 3, is provided by this capacitor.

In this example V_{IN_MIN} = 6.5V, that results in I_{IN_RMS} ≈ 1A. The input capacitor RMS rating should be above 1A.

$$I_{IN_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN_MIN}} \times \frac{\left(V_{IN_MIN} - V_{OUT}\right)}{V_{IN_MIN}}} \quad (3)$$

The main requirement that determines the input capacitance is the converter input voltage ripple given in Equation 4. In this design, the choosing C_{IN} = 10μF results in 147mV input voltage ripple.

$$\Delta V_{IN} = \frac{I_{OUT_MAX} \times 0.25}{C_{IN} \times f_{SW}} \quad (4)$$

The input capacitor also provides the high frequency switching transient currents. So, choosing a low-ESR and small size capacitor with high self-resonance frequency and sufficient RMS rating is necessary.

Inductor Selection

Higher operating frequency allows the designer to choose smaller inductor and capacitor values, however, the switching and gate losses are increased. On the other hand, at lower frequencies the current ripple (ΔI_L) is higher, which results in higher light load losses.

Use Equation 5 to calculate the required inductance. K is the ratio of the inductor peak-to-peak ripple (ΔI_L) to the DC current (I_{OUT}). The recommended selection range for K is between 0.2 ~ 0.4. Choosing a higher K value reduces the selected inductance, but a too high K factor may result in insufficient slope compensation. Equation 6 shows that ΔI_L is inversely proportional to f_{SW} × L and is increased at higher input voltages (V_{IN}). Therefore by accepting larger ΔI_L values, smaller inductances can be chosen but the cost is higher output voltage ripple and increased core losses.

If the peak current exceeds the saturation current, the current ripple increases abruptly (and hence the output voltage ripple). So, it is important to make sure that inductor does not saturate even in the worst conditions. To select the inductor, the RMS current ratings, DCR and temperature rise must also be considered. Use Equation 6, Equation 7 and Equation 8 to calculate the inductor peak-to-peak, RMS and peak currents respectively.

$$L = \frac{V_{IN} - V_{OUT}}{I_{OUT} \times K} \times \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (5)$$

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (6)$$

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^{\ 2}}{12}} \quad (7)$$

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (8)$$

For a design with I_{OUT_MAX} = 2A, V_{OUT} = 5V, f_{SW} = 340kHz and V_{IN} = 12V parameters, and by choosing K = 0.3, the calculated inductance will be 14.3μH. A 15μH standard inductor can be selected that results in about 29% peak-to-peak current ripple.

External Diode

An external power diode between the SW and GND pins is needed for the SGM61234 to complete the converter. This diode must tolerate the application's absolute maximum ratings. The reverse blocking voltage must be higher than V_{IN_MAX} and its peak current must be above the maximum inductor current. Choose a diode with small forward voltage drop for higher efficiency. Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 30V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the SGM61234.

Output Capacitor Design

The main two factors for designing the output capacitance are output voltage ripple and the transient response (peak or valley) to load steps (up or down).

The minimum required capacitance to keep the output transient overshoot below ΔV_{OUT} in response to a load step (drop) with the magnitude of ΔI_{OUT}, is given in Equation 9. In this example (L = 15μH), if ΔI_{OUT} = 1A - 0A = 1A, the required peak voltage deviation (overshoot) is ΔV_{OUT} = 500mV (10% of the V_{OUT} = 5V), which results in 3μF minimum calculated output capacitance.

$$C_{OUT} > \frac{\Delta I_{OUT}^2 \times L}{2 \times V_{OUT} \times \Delta V_{OUT}} \quad (9)$$

APPLICATION INFORMATION (continued)

The other factor is the required maximum output voltage ripple. This requirement limits both C_{OUT} and its ESR, as each parameter individually contribute to the output voltage ripple. Capacitor charge and discharge during switching cycles and the ESR × ΔI_L voltage ripple are two main components of this ripple. Use Equation 10 to calculate the minimum output capacitance required to keep the output voltage ripple below ΔV_{OUT}. In this example, the ΔI_L is 0.57A from Equation 6. If the maximum acceptable ripple is 50mV (1% of the V_{OUT} = 5V), and ESR = 3mΩ, the minimum output capacitance to satisfy the output ripple requirement is 4.4μF.

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{\Delta V_{OUT}}{\Delta I_L} - ESR} \quad (10)$$

Considering both conditions and the required derating and tolerances, a 10μF/6.3V/X7R capacitor with ESR ≤ 3mΩ can be chosen.

Bootstrap Capacitor Selection

Use a 0.1μF high-quality ceramic capacitor (X7R or X5R) with 10V or higher voltage rating for the bootstrap capacitor (C_4). It is recommended to add a resistor R_4 in series with C_4 to slow down switch-on speed of the HS switch and improve radiated EMI problems. The R_4 value depends on the size of the HS switch. For most applications, it's approximately 5Ω ~ 10Ω. Too high values for R_4 may cause insufficient C_4 charging in high duty-cycle applications. Slower switch-on will also increase switch losses and reduce efficiency.

Soft-Start Capacitor Selection

The soft-start capacitor programs the ramp-up time of the output voltage during power-up. Due to the limited voltage slew rate required by the load or limited available input current, a ramp is needed in many applications to avoid input voltage sag during startup (UVLO) or to avoid over-current protection that can occur during output capacitor charging. Soft-start will solve all these issues by limiting the output voltage slew rate.

Equation 2 (with I_{SS} = 2μA and V_{REF} = 0.8V) can be used to calculate the soft-start capacitor for a required soft-start time (t_{SS}). It is recommended that C_{SS} be less than 27nF.

Typical Application

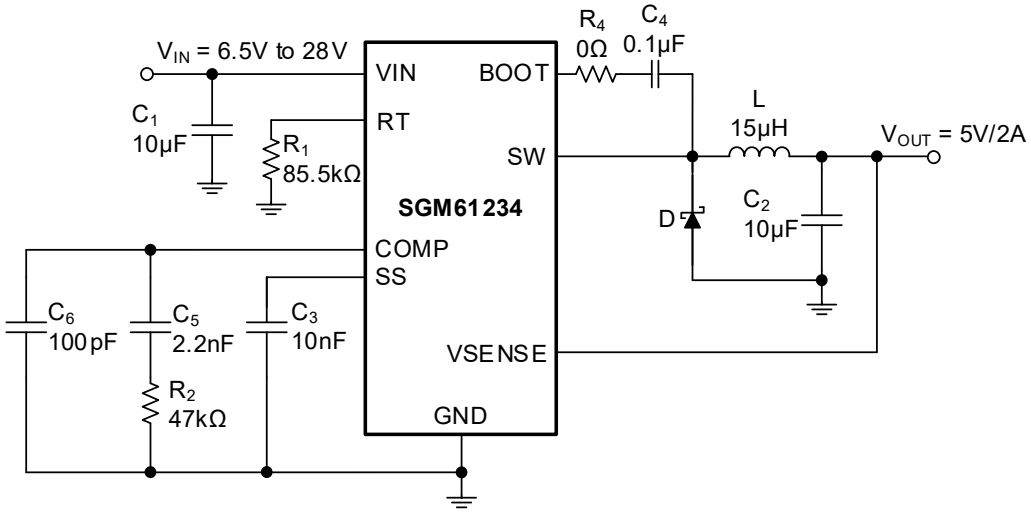


Figure 4. SGM61234 Typical Application Circuit

APPLICATION INFORMATION (continued)

Layout Considerations

A PCB layout example for SOIC-8 (Exposed Pad) is provided in Figure 5. This layout has been proved to bring good results although other layout designs may also obtain good performance.

• Bypass the VIN pin to GND pin (where it connects to the anode pin of the power diode) with low-ESR ceramic capacitors and place them as close as possible to the device.

• Connect the diode as close as possible to SW and GND pins.

• Minimize VSENSE trace length. Connect the VSENSE trace from the point where VOUT accuracy is important and keep it away from the noisy nodes (SW), preferably through another layer that is on the other side of a shield layer.

• Share the same GND connection point with the input and output capacitors.

• Minimize the length and the area of the connection route from SW pin to the cathode of the diode and the inductor to reduce the noise coupling from this area.

• Consider sufficient ground plane area on the top side for proper heat dissipation. Connect the large internal or back-side ground planes to the top-side ground near the device with thermal vias for better heat dissipation.

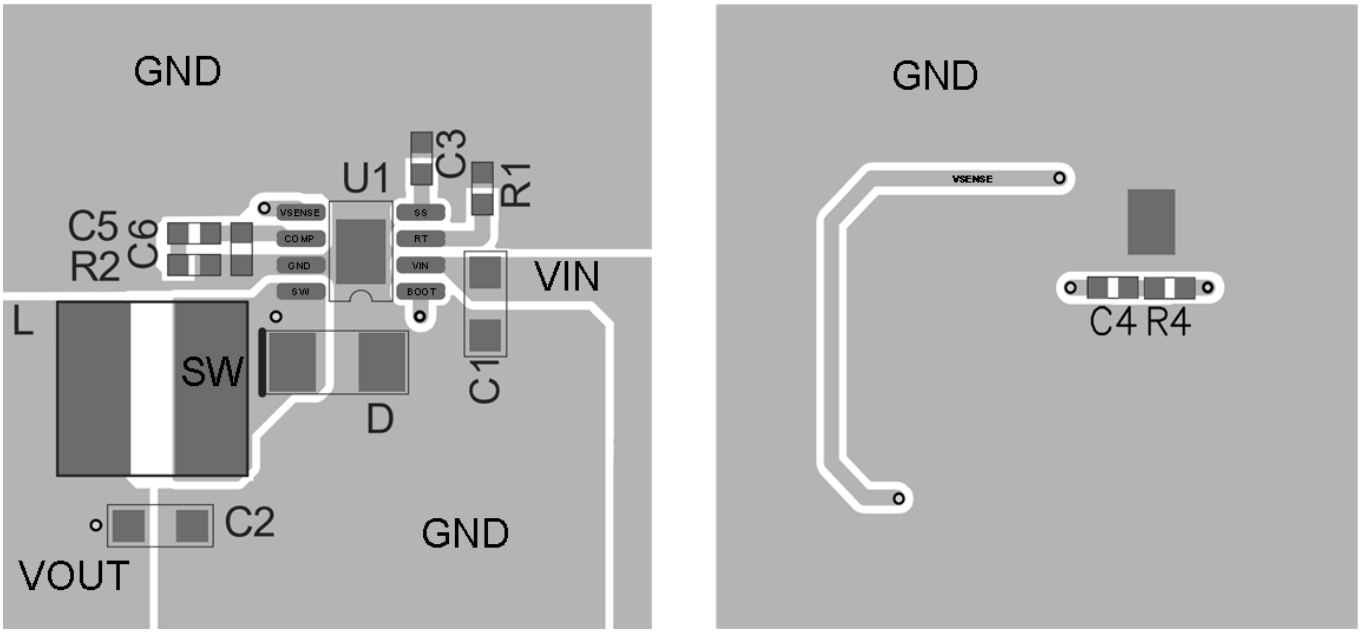


Figure 5. Top and Bottom Layers for SOIC-8 (Exposed Pad)

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

APRIL 2026 – REV.A.2 to REV.A.3	Page
Updated recommended operating conditions section	2
Updated pin description section	3
Updated electrical characteristics section	4
Updated typical performance characteristics section	5, 6, 7, 8, 9
Updated functional block diagram	9
Updated detailed description	10
Updated application information	13

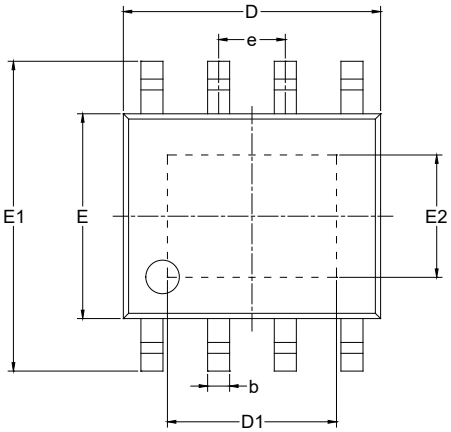
MAY 2025 – REV.A.1 to REV.A.2	Page
Updated absolute maximum ratings section	2

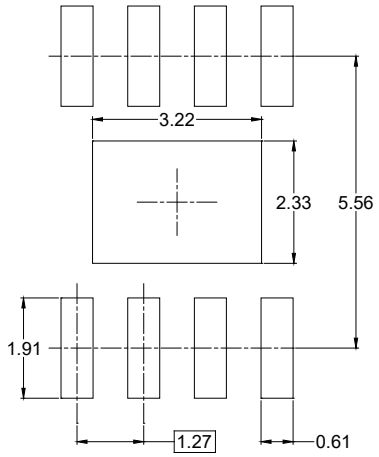
JANUARY 2022 – REV.A to REV.A.1	Page
Added SOIC-8 Package	1, 2, 3

Changes from Original (JANUARY 2022) to REV.A	Page
Changed from product preview to production data	All

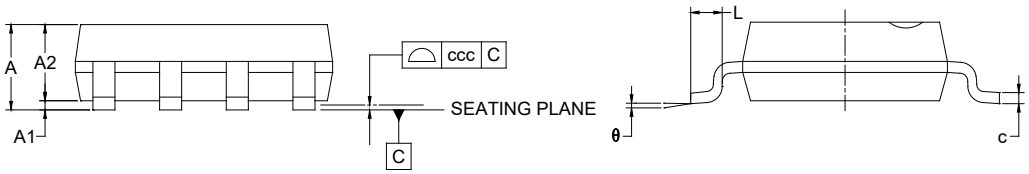
PACKAGE OUTLINE DIMENSIONS

SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)

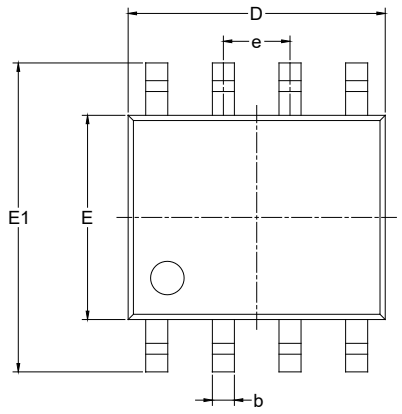


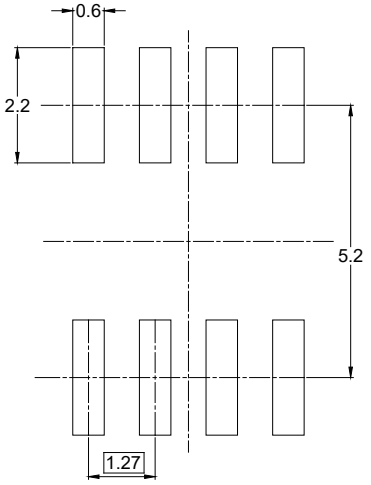
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

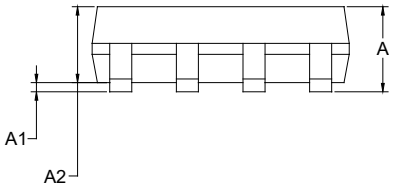
PACKAGE OUTLINE DIMENSIONS

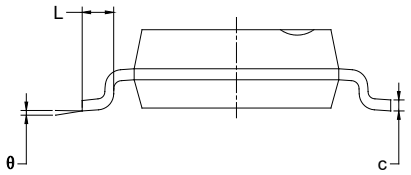
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)



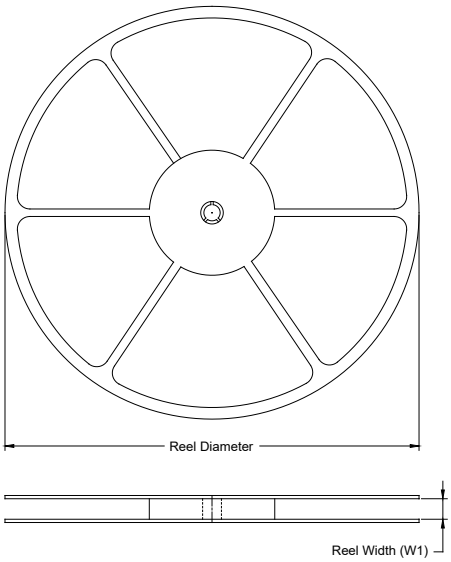


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

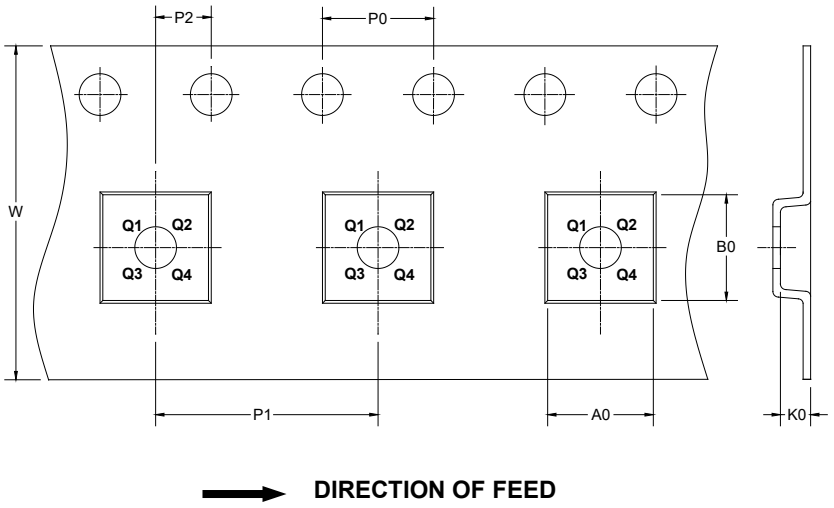
NOTES:
1. Body dimensions do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



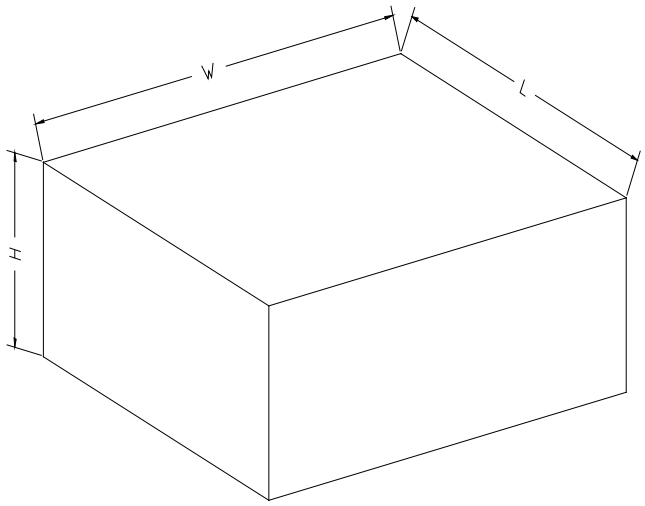
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
SOIC-8	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002