SGM61103
3V to 17V, 300mA Buck Converter with Adjustable Enable Threshold and Hysteresis

GENERAL DESCRIPTION

The SGM61103 is an easy-to-use synchronous Buck DC/DC converter optimized for low-power applications. A high switching frequency of 1MHz (TYP) allows the use of small inductors and provides fast transient response as well as high output voltage accuracy by using AHP-COT control topology.

With its wide operating input voltage range of 3V to 17V and low quiescent current, SGM61103 is ideally suited for battery-powered systems. The SGM61103 works in power-save mode to ensure the highest efficiency at light load conditions.

The SGM61103 supports up to 300mA continuous output current at wide output voltages between 1.2V and 10V. Lower-power EN comparator with precise threshold and hysteresis can be used as the input supply voltage supervisor (SVS). More hysteresis is possible by combining with EN_HYS pin. PG pin is also provided as output voltage indicator.

The SGM61103 is available in a Green TDFN-2×2-8AL package.

FEATURES

- **AHP-COT Control Topology**
- **Input Voltage Range: 3V to 17V**
- **Output Voltage Range: 1.2V to 10V**
- **Quiescent Current: 28μA (TYP)**
- **Shutdown Current: 450nA (TYP)**
- **Switching Frequency: Up to 1MHz**
- **EN Pin with Precise Threshold**
- **EN_HYS Pin for Additional Hysteresis Programming**
- **100% Duty Cycle Mode**
- **Power Good Indicator**
- **Output Discharge**
- **Available in a Green TDFN-2×2-8AL Package**

APPLICATIONS

Embedded Processing
Battery-Powered Systems
9V to 15V Standby Power Supply
Energy Harvesting
Inverter (Negative V_{OUT})

TYPICAL APPLICATION

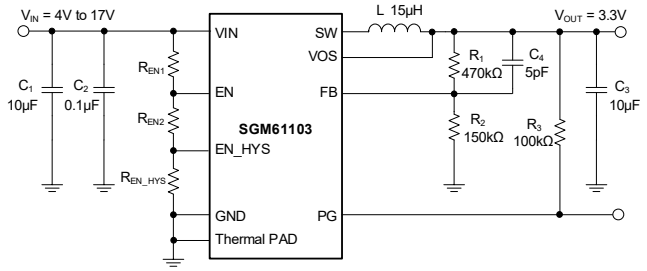
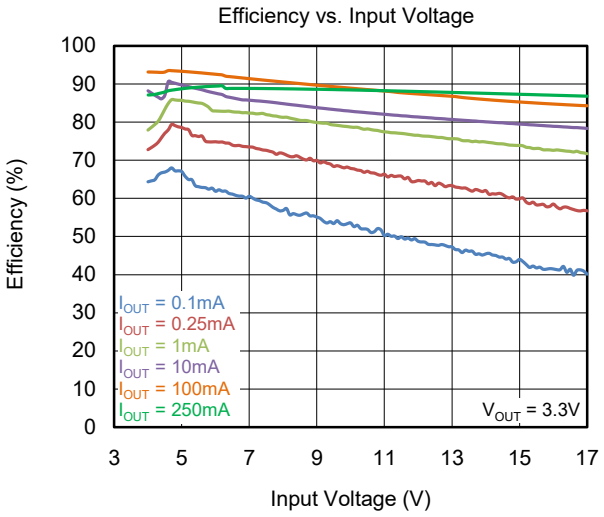


Figure 1. Typical Application Circuit

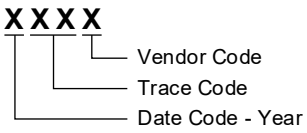


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61103	TDFN-2×2-8AL	-40℃ to +125℃	SGM61103XTDE8G/TR	0EH XXXX	Tape and Reel, 3000
	TDFN-2×2-8AL	-40℃ to +125℃	SGM61103XTDE8DG/TR	0EH XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range
- VIN ..... -0.3V to 20V
- SW (DC) ..... -0.3V to V_{IN} + 0.3V
- SW (AC, Less than 10ns) ..... -3V to 23.5V
- EN ..... -0.3V to V_{IN} + 0.3V
- FB ..... -0.3V to 3.6V
- VOS, PG ..... -0.3V to 12V
- EN_HYS ..... -0.3V to 7V

Power Good Sink Current, I_{PG} 10mA
EN_HYS Sink Current, I_{EN_HYS} 3mA
Package Thermal Resistance
- TDFN-2×2-8AL, θ_{JA} ..... 66℃/W
- TDFN-2×2-8AL, θ_{JB} ..... 31.2℃/W
- TDFN-2×2-8AL, $\theta_{JC\ (TOP)}$ ..... 83.6℃/W
- TDFN-2×2-8AL, $\theta_{JC\ (BOT)}$ ..... 12.3℃/W

Junction Temperature ..... +125℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{IN} ..... 3V to 17V
Output Current, I_{OUT}
- 3V ≤ V_{IN} < 6V 200mA
- 6V ≤ V_{IN} ≤ 17V 300mA

Operating Junction Temperature, T_J ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

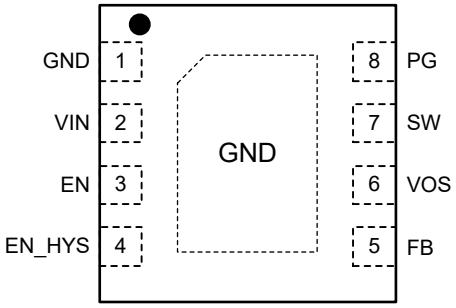
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TDFN-2×2-8AL

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	GND	G	Ground Pin.
2	VIN	P	Input Voltage Pin.
3	EN	I	Active High Enable Input. Pull up to 1.22V to enable the device or pull down to 1.15V to disable it. Connect an external resistor to EN_HYS pin to increase the hysteresis if needed. Do not leave this pin unconnected.
4	EN_HYS	O	Enable Hysteresis Open-Drain Output. This pin is pulled to GND when the rising voltage on the EN pin is below 1.22V or the falling voltage on the EN pin is above 1.15V. The pin is high-impedance once the EN voltage rises above 1.22V or falls below 1.15V. Connect EN_HYS pin to GND or leave it floating if it is not used.
5	FB	I	Feedback Pin. Connect a resistor divider between the output voltage sense point and ground, and tap it to the FB pin to set the output voltage.
6	VOS	I	Output Voltage Sense Pin. Connect this pin to the output voltage of the DC/DC converter.
7	SW	O	Switch Node of the Power Converter. Connect it to the output inductor.
8	PG	O	Power Good Indicator. This pin is open-drain output. It is released to go high if the device is in power good status. Pull up this pin to a 10V or less voltage rail. It can be left open if not used.
-	Exposed Pad	G	Exposed Thermal Pad. Connect it to GND.

NOTE: I = input, O = output, P = power, G = ground.

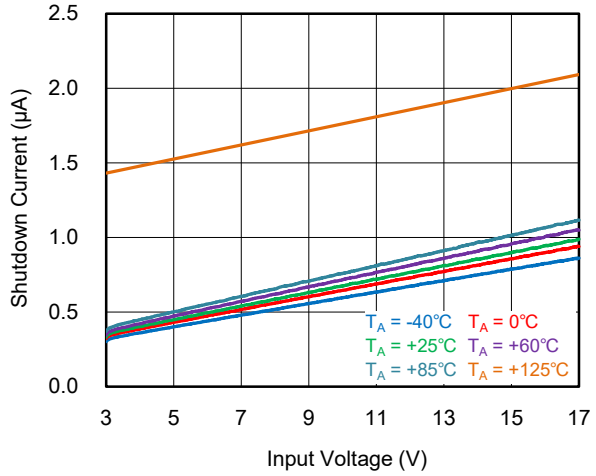
ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 12V, typical values are at T_J = +25℃, unless otherwise noted.)

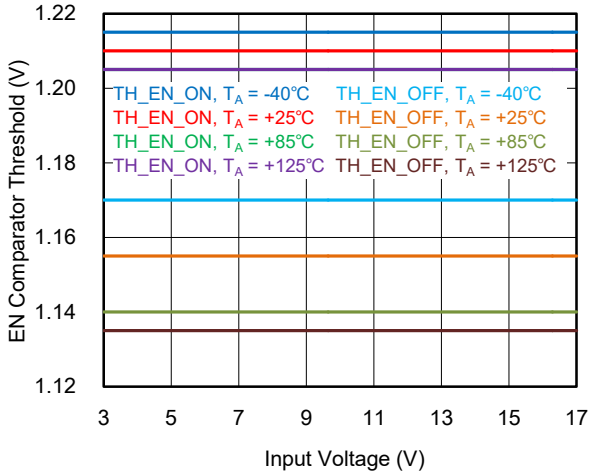
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage						
Input Voltage Range	V_{IN}		3		17	V
Output Voltage Range	V_{OUT}		1.2		10	V
Quiescent Current	I_Q	I_{OUT} = 0mA, not switching, V_{EN} = V_{IN}, regulator in sleep		28	42	μA
		I_{OUT} = 0mA, switching, V_{IN} = 7.2V, V_{OUT} = 1.2V, L = 22μH		30		μA
		Enable comparator on, V_{IN} = 5V, V_{EN} = 1.1V, DC/DC converter off		1.7	6	μA
Active Mode Current Consumption	I_{ACTIVE}	V_{IN} = V_{OUT} = 5V, T_A = +25℃, high-side MOSFET switch fully turned on (100% mode)		290	550	μA
Shutdown Current	I_{SD}	Enable comparator off, V_{IN} = 5V, V_{EN} < 0.4V, V_{OUT} = V_{SW} = 0V		0.45	4	μA
Under-Voltage Lockout Threshold	V_{UVLO_F}	V_{IN} falling	2.65	2.77		V
	V_{UVLO_R}	V_{IN} rising		2.87	2.95	V
Enable Threshold and Hysteresis (EN, EN_HYS)						
EN Pin Threshold	$V_{TH_EN_ON}$	V_{IN} = 3V to 17V, V_{EN} rising		1.22	1.35	V
	$V_{TH_EN_OFF}$	V_{IN} = 3V to 17V, V_{EN} falling	1.02	1.15		V
EN Pin Hysteresis	$V_{TH_EN_HYS}$	V_{IN} = 3V to 17V, Hysteresis		70		mV
Input Bias Current into EN Pin	I_{IN_EN}	V_{EN} = 1.3V		5	50	nA
EN_HYS Pin Output Low	V_{EN_HYS}	I_{EN_HYS} = 1mA, V_{EN} = 1.1V			0.4	V
Input Bias Current into EN_HYS Pin	$I_{IN_EN_HYS}$	V_{EN_HYS} = 1.3V		10	50	nA
Power Switch						
High-side MOSFET On-Resistance	R_{DSON}	V_{IN} = 3V, I_{OUT} = 100mA		1.95	3.2	Ω
		V_{IN} = 12V, I_{OUT} = 100mA		1.45	2.4	Ω
Low-side MOSFET On-Resistance		V_{IN} = 3V, I_{OUT} = 100mA		0.7	1.2	Ω
		V_{IN} = 12V, I_{OUT} = 100mA		0.55	0.9	Ω
Switch Current Limit High-side MOSFET	I_{LIMF}	V_{IN} = 12V	600	750	1050	mA
Thermal Shutdown	T_{SD}	Increasing junction temperature		150		℃
Thermal Shutdown Hysteresis	T_{HYS}	Decreasing junction temperature		20		℃
Output						
Switching Frequency	f_{SW}	V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 300mA		1		MHz
Internal Reference Voltage of Error Amplifier	V_{REF_FB}			0.808		V
Feedback Voltage Accuracy	V_{FB}	Referred to V_{REF_FB}	-2.2		2.2	%
Feedback Voltage Line Regulation		V_{OUT} = 3.3V, I_{OUT} = 100mA, V_{IN} = 5V to 17V, L = 15μH, C_{OUT} = 10μF		-0.01		%/V
Feedback Voltage Load Regulation		V_{OUT} = 3.3V, I_{OUT} = 1mA to 300mA, V_{IN} = 12V, L = 15μH, C_{OUT} = 10μF		-0.002		%/mA
Input Bias Current into FB Pin	I_{IN_FB}	V_{FB} = 0.8V		0.1	10	nA
Regulator Startup Time	t_{START}	V_{IN} = 5V, EN high to start switching		230		μs
Output Voltage Ramp Time	t_{RAMP}	First pulse to 95% V_{OUT} (TYP), I_{OUT} = 0.3A		460		μs
Leakage Current into SW Pin	I_{LK_SW}	V_{OS} = V_{IN} = V_{SW} = 1.8V, V_{EN} = GND		0.002	0.1	μA
Bias Current into VOS Pin	I_{IN_VOS}	V_{OS} = V_{IN} = V_{SW} = 1.8V, V_{EN} = GND		3	50	nA
Power Good Output (PG)						
Power Good Threshold Voltage	V_{TH_PG}	Rising V_{FB} feedback voltage	92	95	98	%
		Falling V_{FB} feedback voltage	86	90	92	%
PG Pin Low-Level Output Voltage	V_{OL}	Current into PG pin, I_{PG} = 0.4mA			0.2	V
PG Pin High-Level Output Voltage	V_{OH}	Open-drain output, external pull-up resistor			10	V
Bias Current into PG Pin	I_{IN_PG}	V_{PG} = 3V, V_{EN} = 1.3V, V_{FB} = 0.85V		10	50	nA

TYPICAL PERFORMANCE CHARACTERISTICS

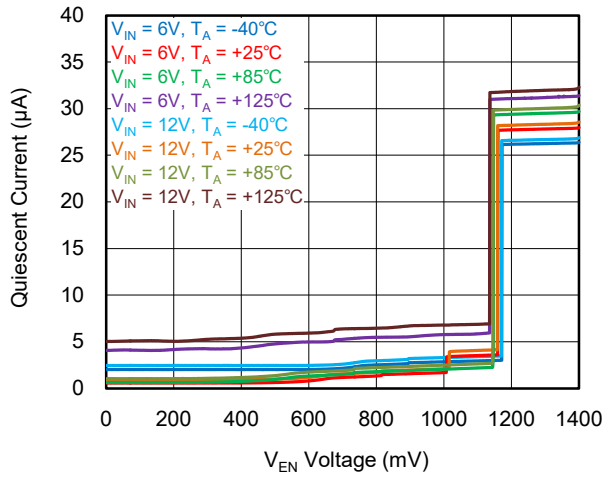
Shutdown Current vs. Input Voltage



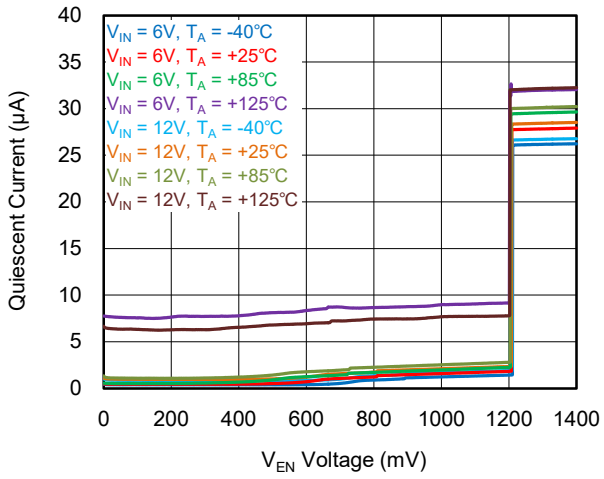
EN Comparator Threshold vs. Input Voltage



Quiescent Current vs. V_{EN} Voltage, V_{EN} Falling

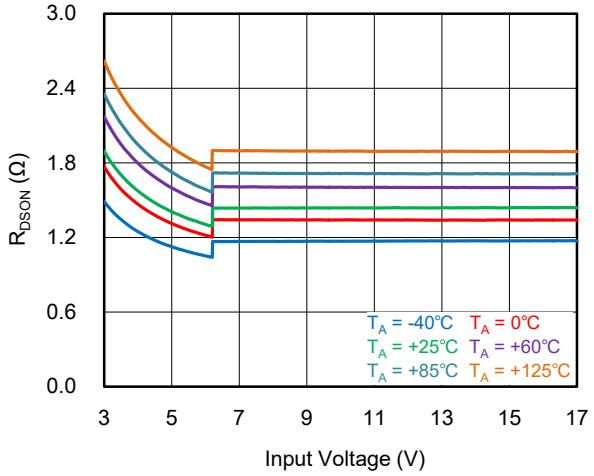


Quiescent Current vs. V_{EN} Voltage, V_{EN} Rising

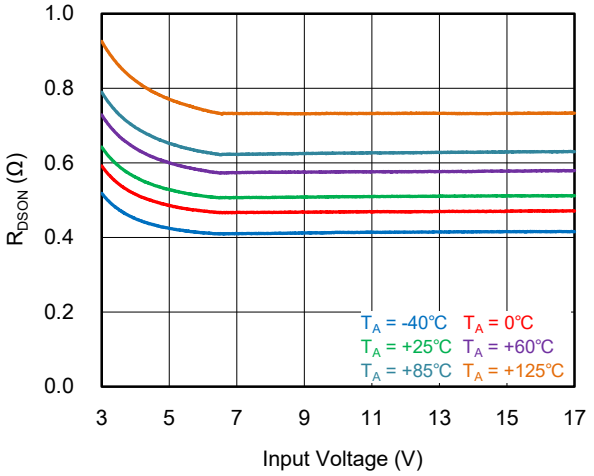


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

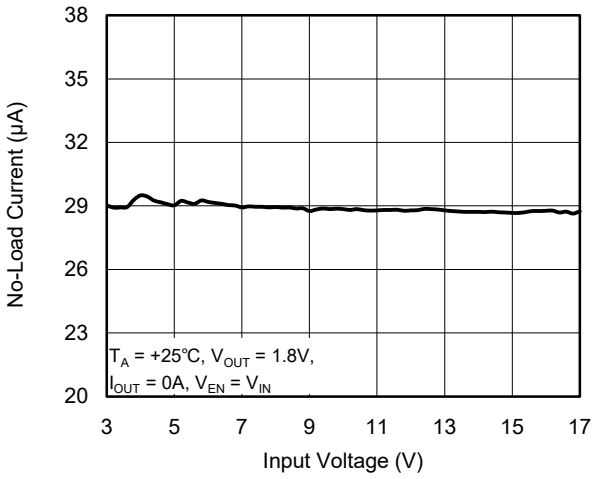
R_{DSON} High-side Switch vs. Input Voltage



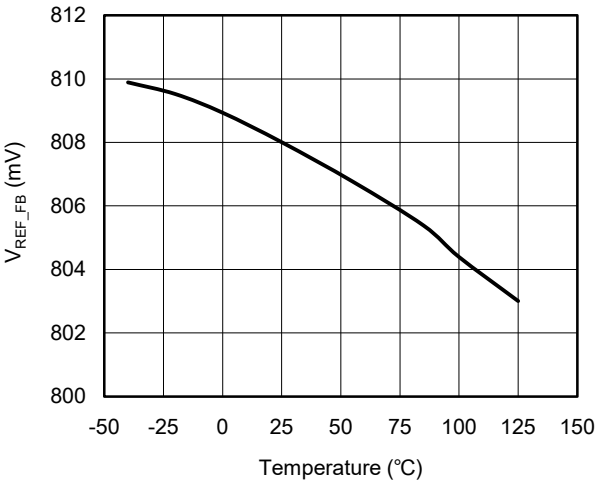
R_{DSON} Low-side Switch vs. Input Voltage



No-Load Current vs. Input Voltage



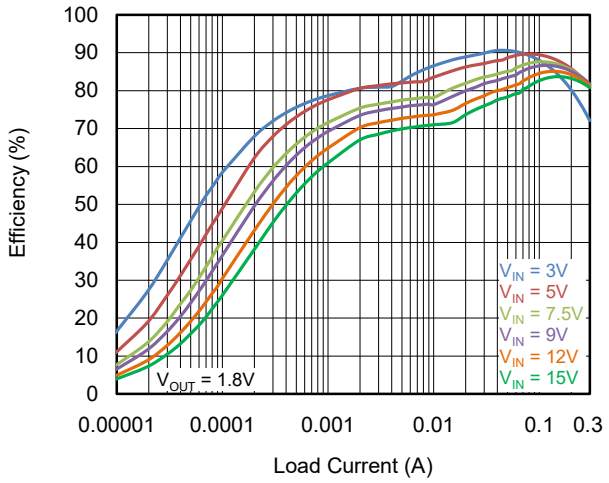
V_{REF_FB} vs. Temperature



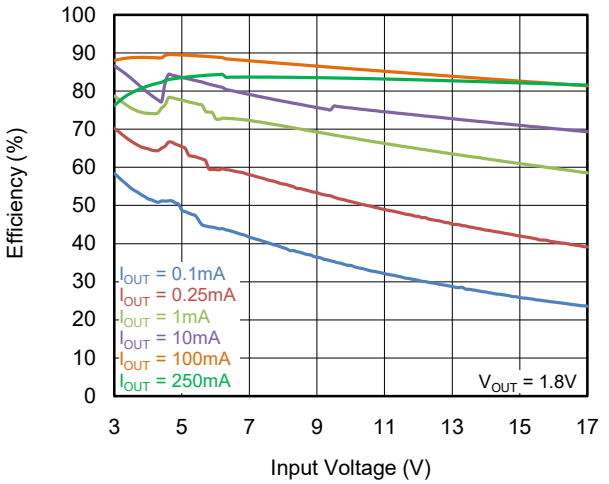
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L = 15μH, DCR = 210mΩ, and C_{OUT} = 10μF, unless otherwise noted.

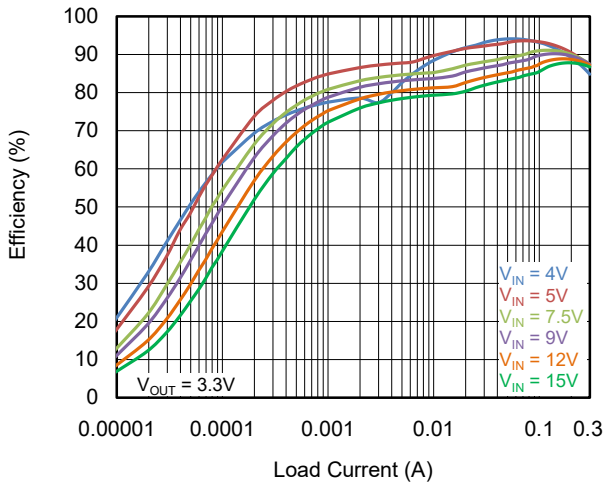
Efficiency vs. Load Current



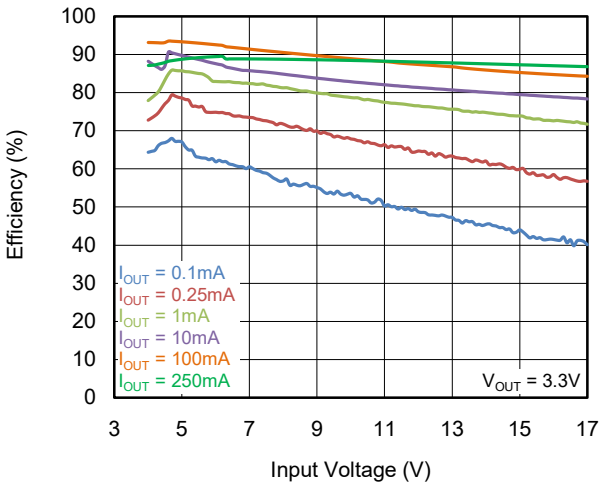
Efficiency vs. Input Voltage



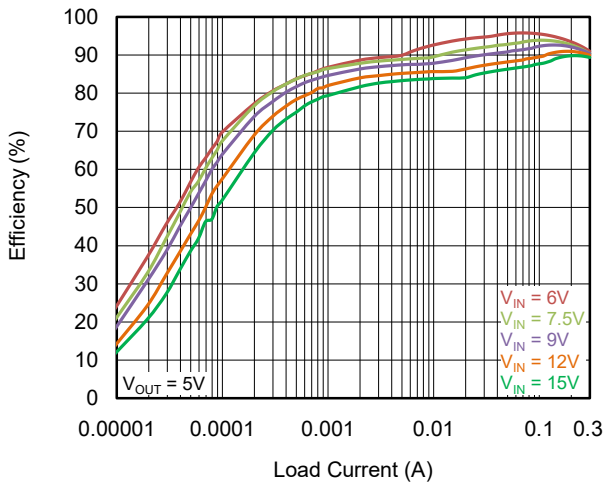
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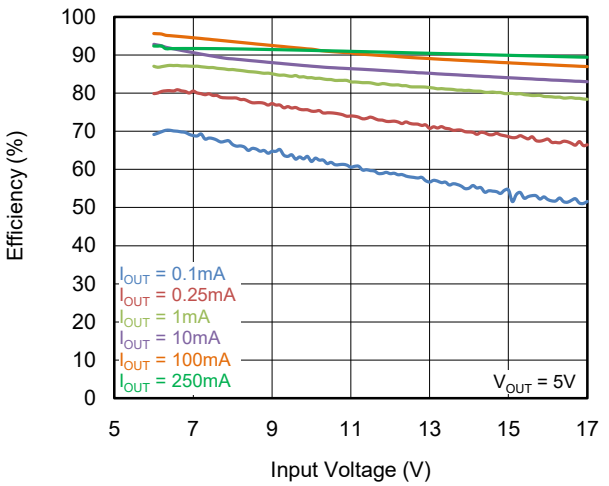
Efficiency vs. Input Voltage



Efficiency vs. Load Current



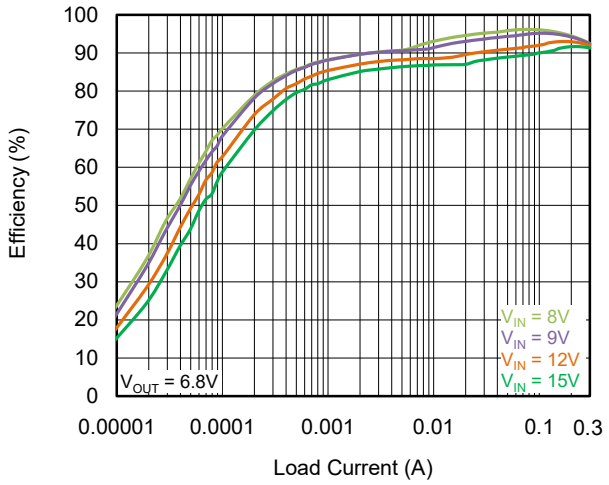
Efficiency vs. Input Voltage



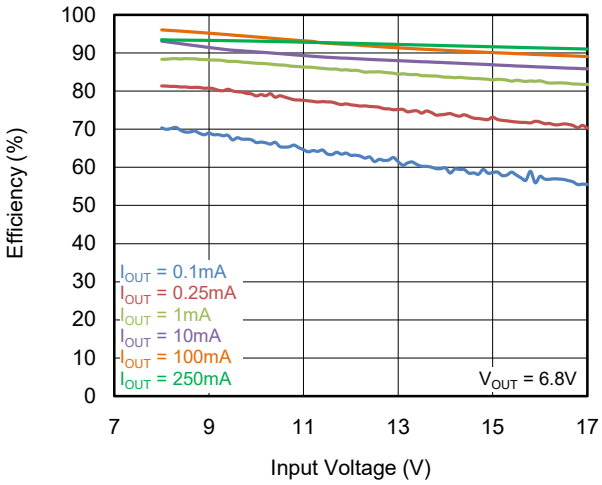
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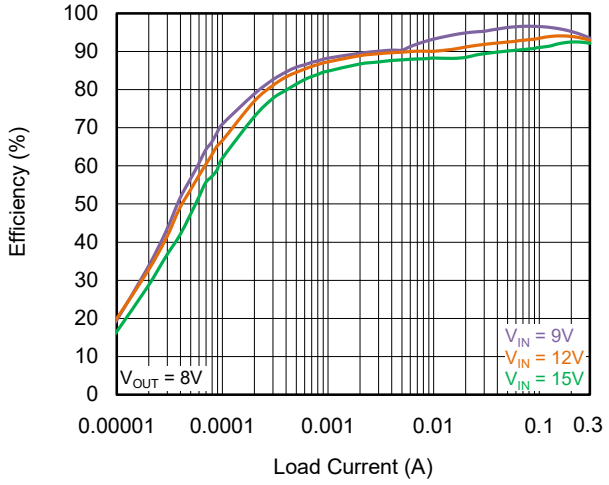
Efficiency vs. Load Current



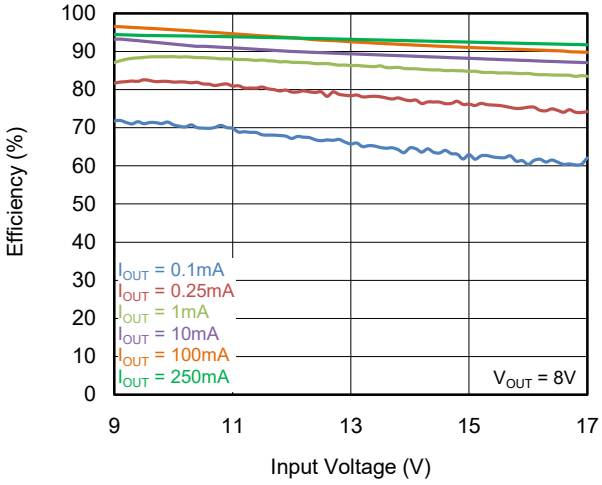
Efficiency vs. Input Voltage



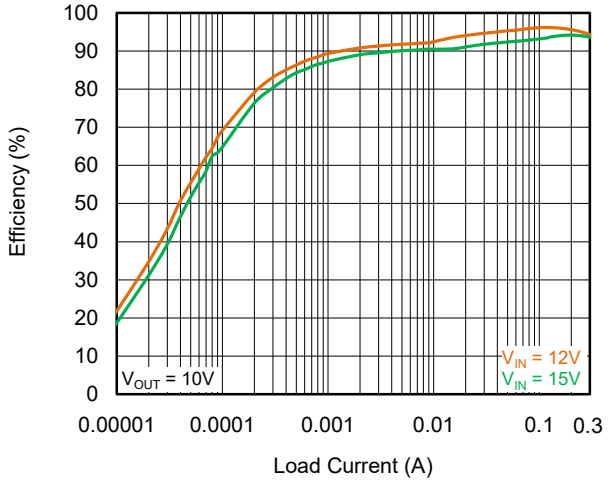
Efficiency vs. Load Current



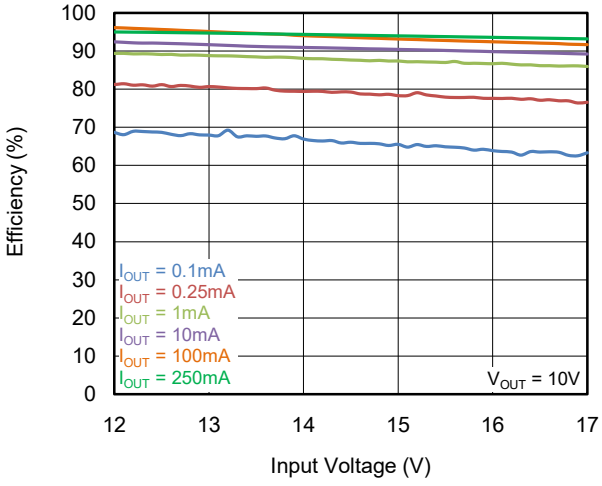
Efficiency vs. Input Voltage



Efficiency vs. Load Current



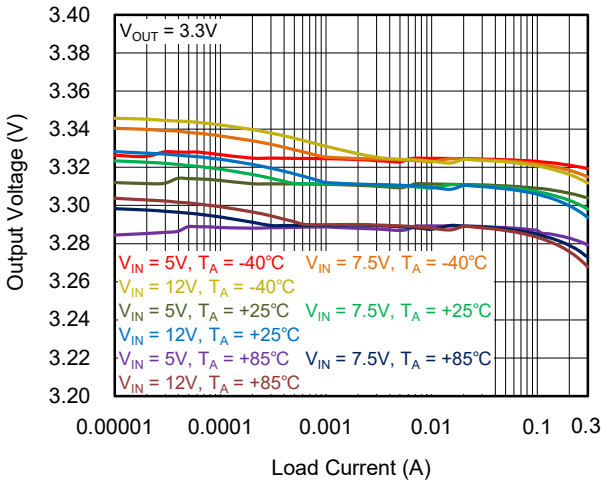
Efficiency vs. Input Voltage



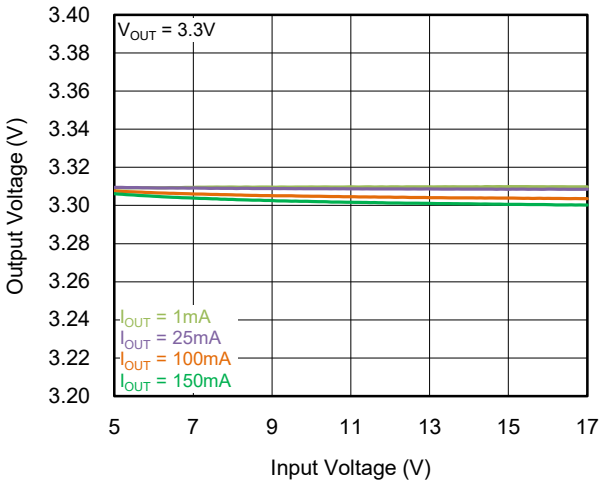
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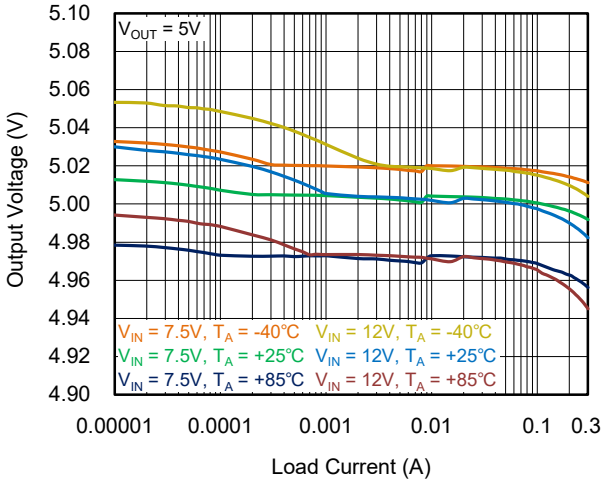
Load Regulation



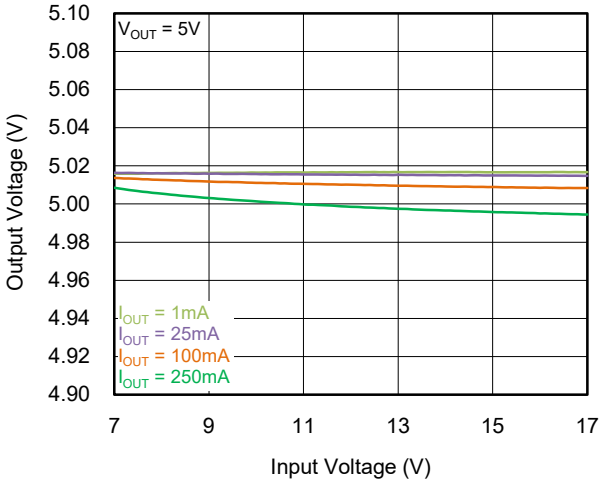
Line Regulation



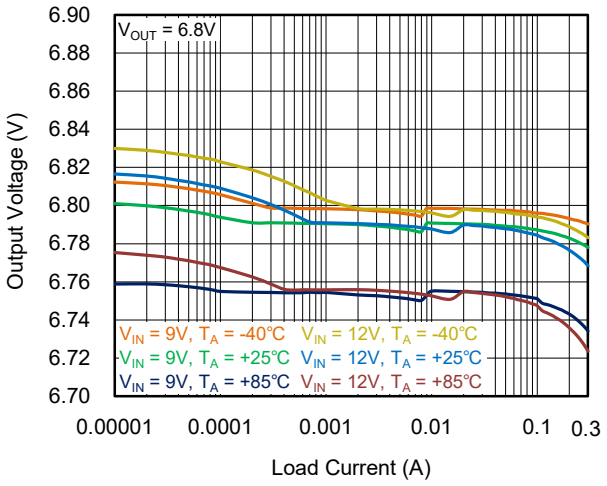
Load Regulation



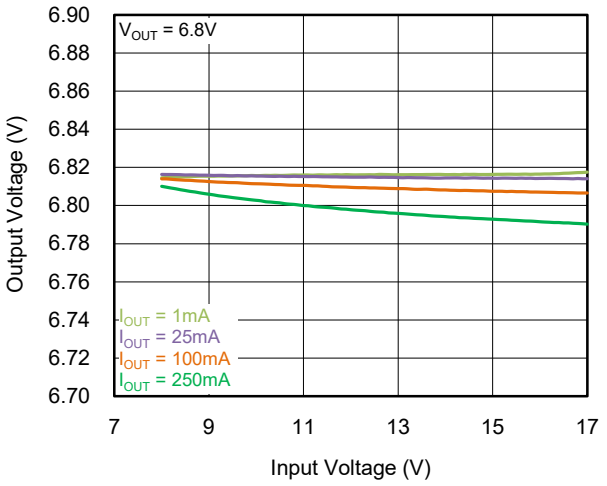
Line Regulation



Load Regulation



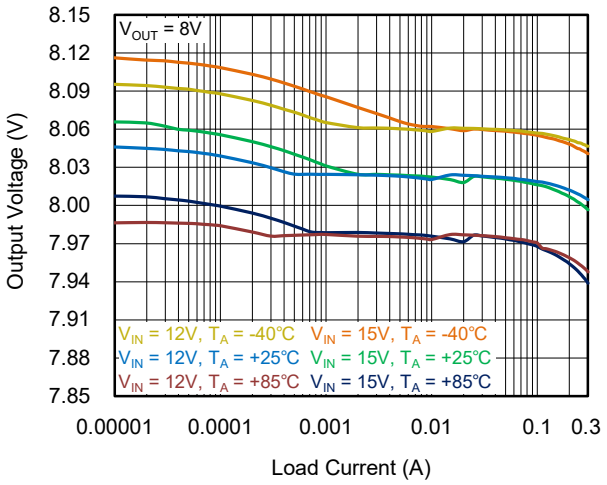
Line Regulation



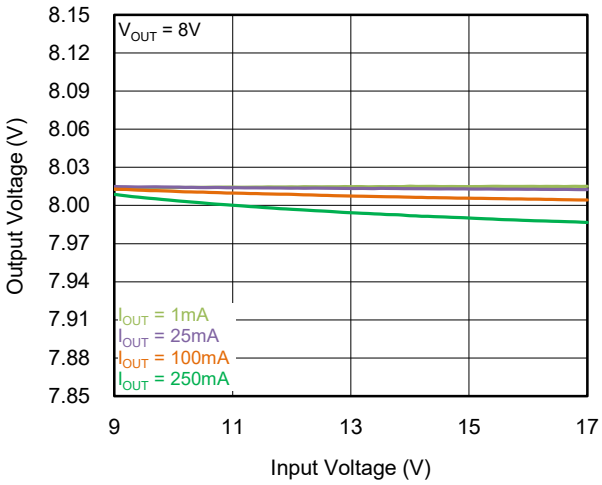
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L = 15μH, and C_{OUT} = 10μF, unless otherwise noted.

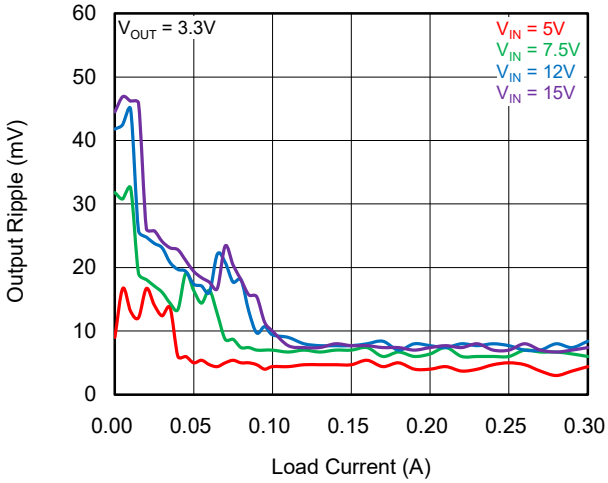
Load Regulation



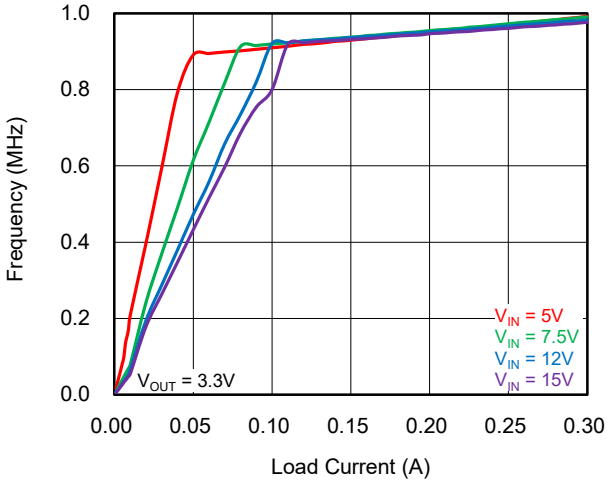
Line Regulation



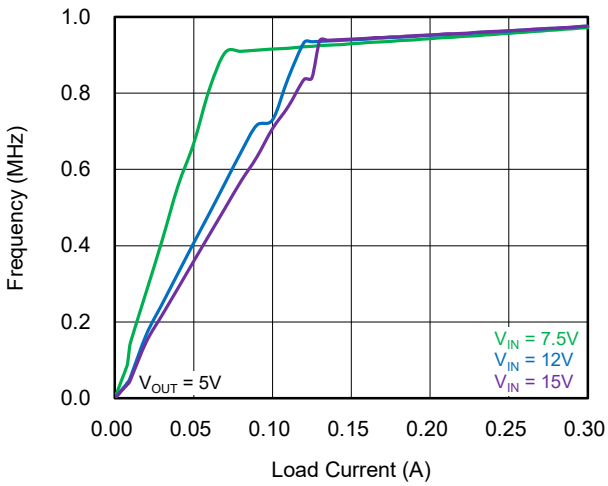
Output Ripple vs. Load Current



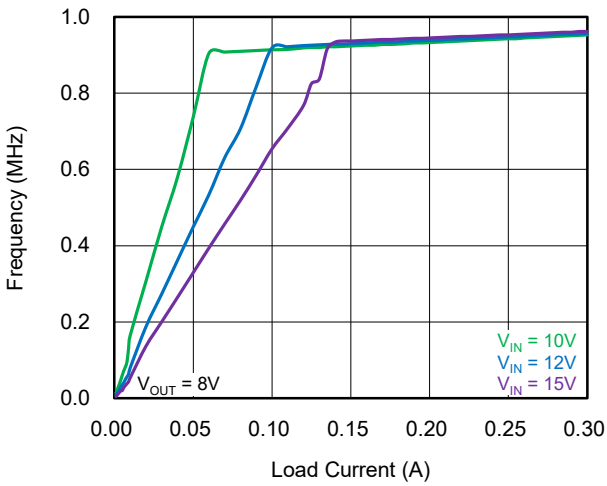
Frequency vs. Load Current



Frequency vs. Load Current



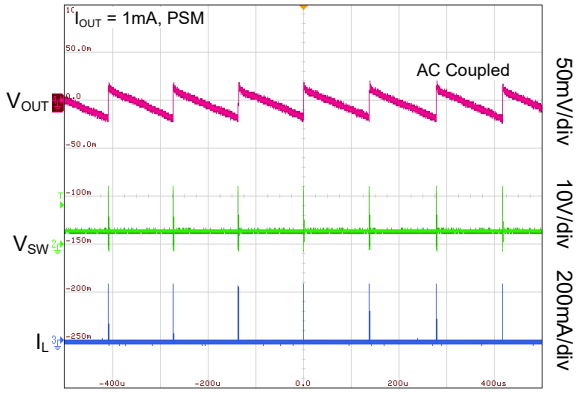
Frequency vs. Load Current



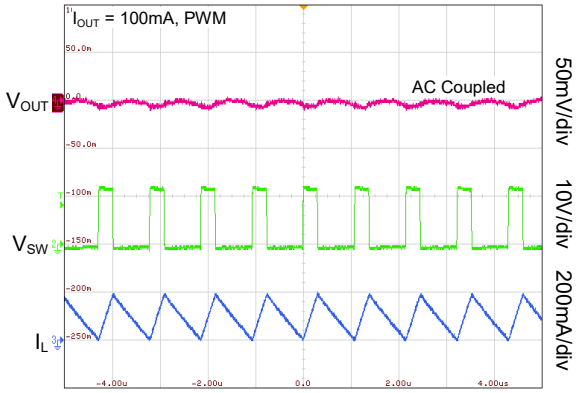
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L = 15μH, and C_{OUT} = 10μF, unless otherwise noted.

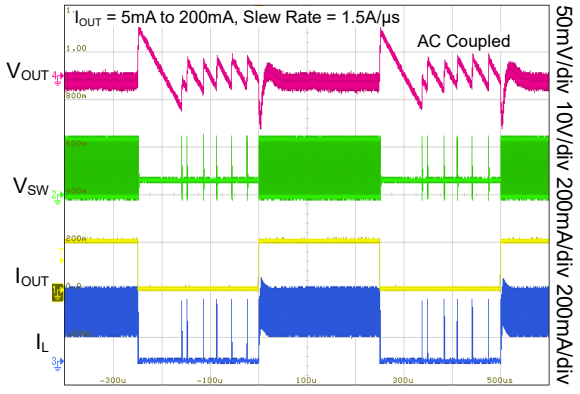
Output Ripple



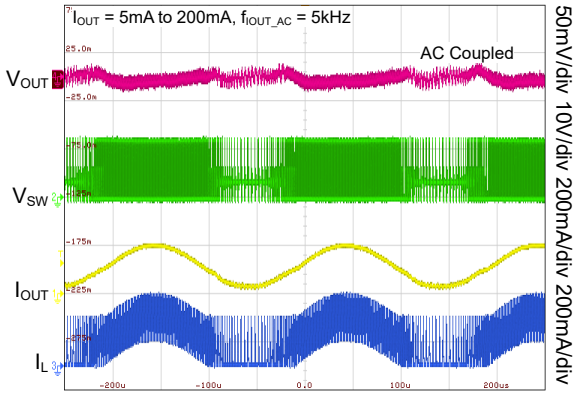
Output Ripple



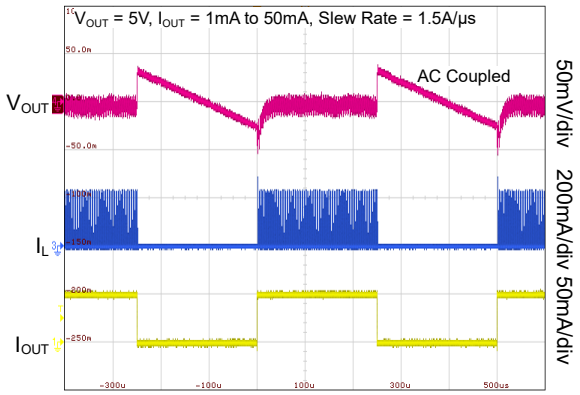
Load Transient



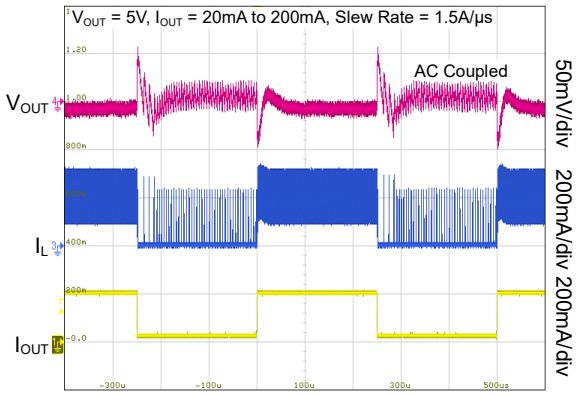
AC Load Regulation



Load Transient



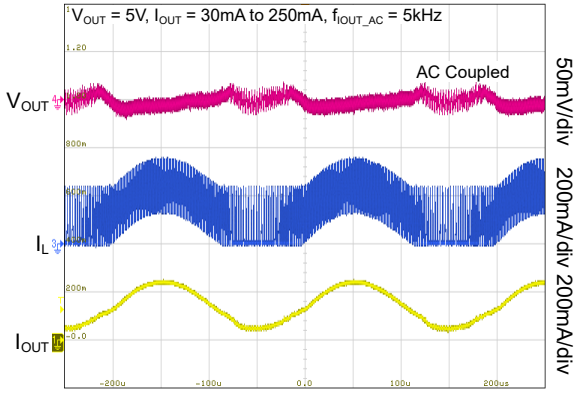
Load Transient



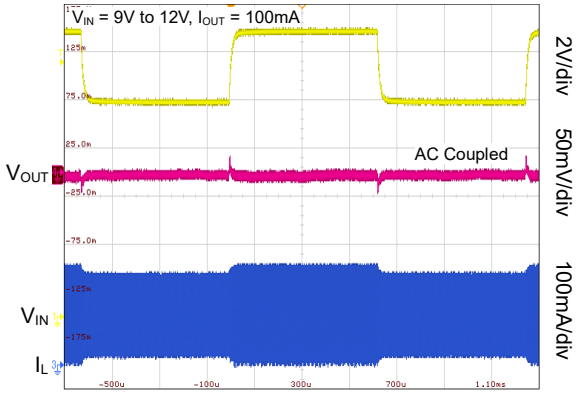
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L = 15μH, and C_{OUT} = 10μF, unless otherwise noted.

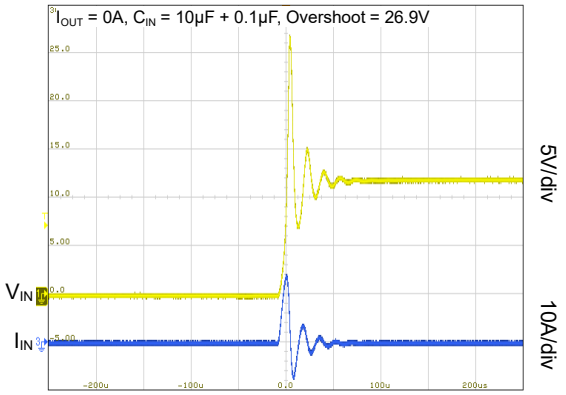
AC Load Regulation



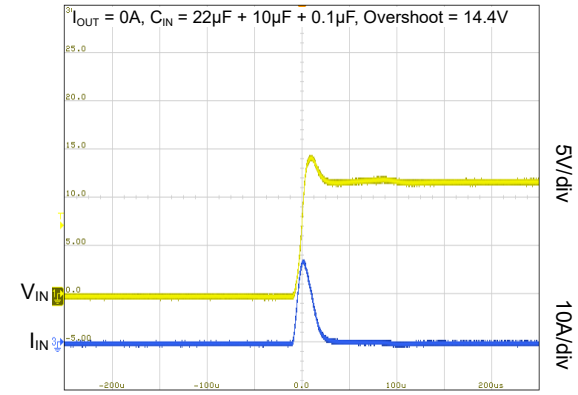
Line Transient



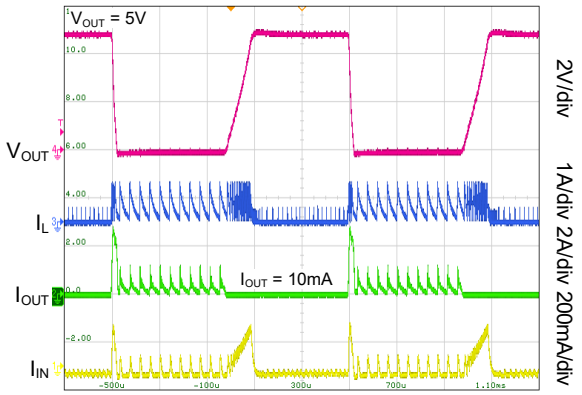
Hot Plug Overshoot



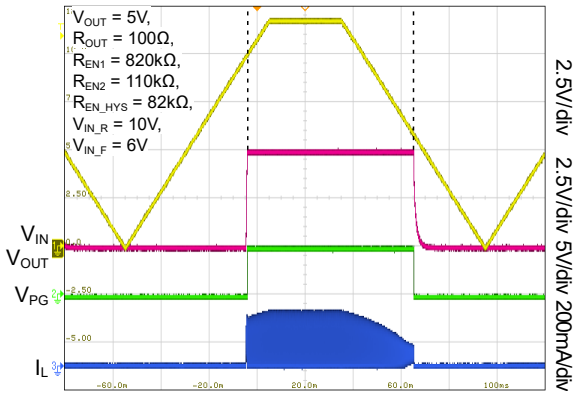
Hot Plug Overshoot Reduction



Short-Circuit Protection and Recovery



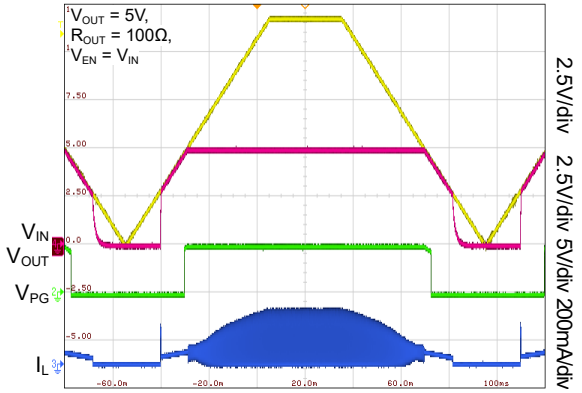
Input Supply Voltage Supervisor (SVS)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

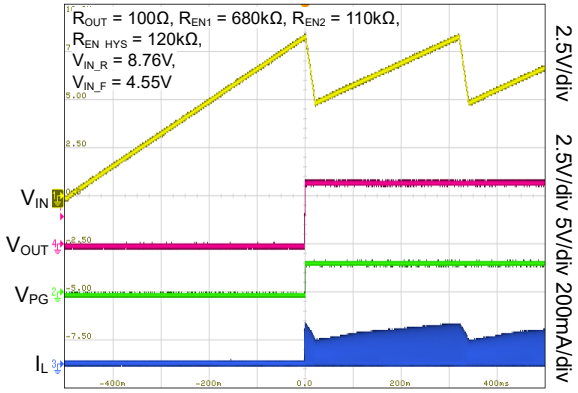
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L = 15μH, and C_{OUT} = 10μF, unless otherwise noted.

Operation with V_{EN} = V_{IN}, V_{IN} Tracks V_{OUT}



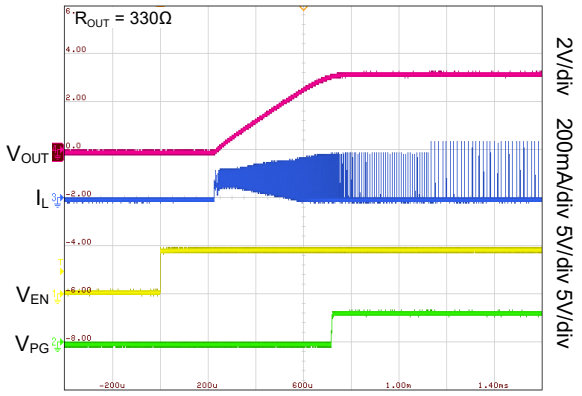
Time (20ms/div)

Simulated High-Impedance Source



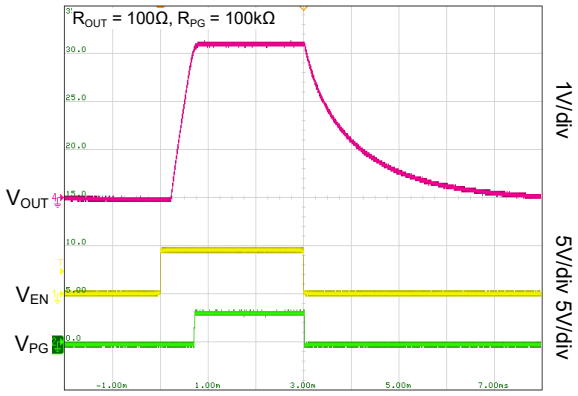
Time (100ms/div)

Startup



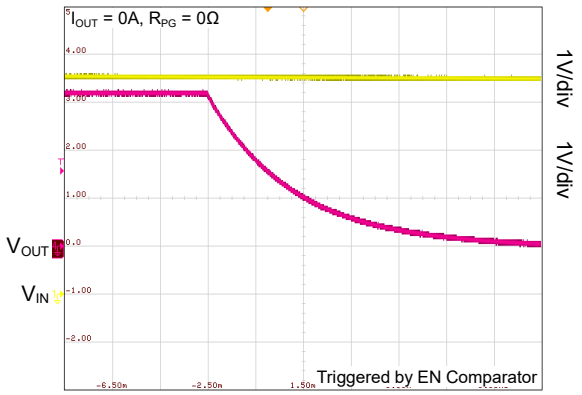
Time (200μs/div)

V_{OUT} Ramp-Up/Down with V_{EN} On/Off



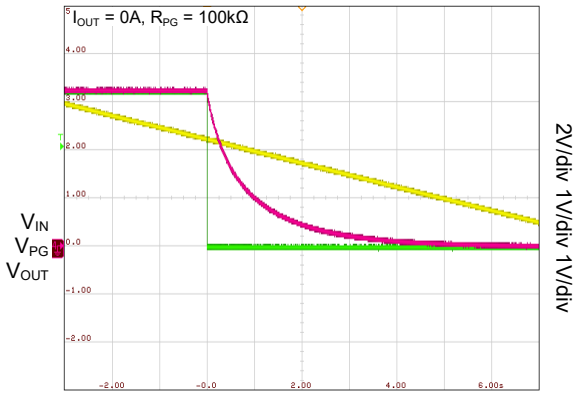
Time (1ms/div)

Output Discharge Using PG Pin



Time (2ms/div)

V_{OUT} Ramp-Down with Falling V_{IN}



Time (1s/div)

FUNCTIONAL BLOCK DIAGRAM

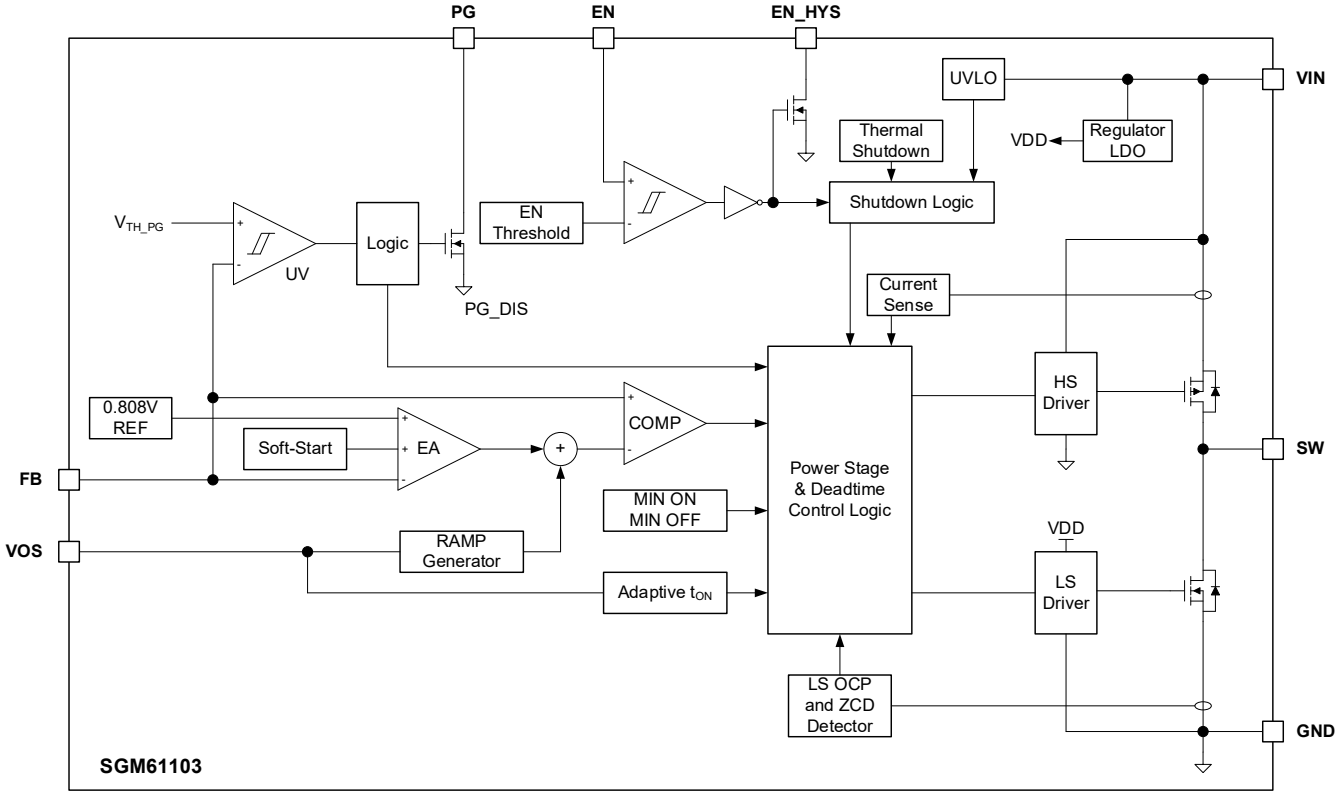


Figure 2. SGM61103 Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61103 is a high efficiency Buck switching regulator with wide input voltage range of 3V to 17V. It operates at a quasi-fixed frequency of 1MHz and uses AHP-COT PWM control for the moderate to heavy load range. In order to achieve quasi-fixed frequency, it adjusts on-time adaptively according to input voltage and output voltage fed by the output voltage sense (VOS) pin. For low converter drop, it can operate at 100% duty cycle.

The SGM61103 transitions seamlessly from PWM mode to pulse frequency modulation (PFM) once the inductor current becomes discontinuous. At lighter load conditions, it shifts to the power-save mode (PSM) to minimize the losses. It also shuts down most of the internal circuits in power-save mode. In this mode, one or a few PWM pulses are sent to charge the output capacitor and then the switches are kept off. The output capacitor voltage gradually drops due to small load current and when it falls below the nominal voltage threshold, the PWM pulses resume. If the load is still low, the output will go slightly higher than normal value again and the switches will be turned off. In power-save mode, the output voltage is slightly higher than the nominal output voltage.

Under-Voltage Lockout Protection

Preventing from faulty logic in the internal circuit due to low input supply voltage, the device includes an under-voltage lockout (UVLO). The UVLO threshold is set to 2.87V for V_{IN} rising and 2.77V for V_{IN} falling. The device starts operation when the input voltage rises above the rising threshold and shuts down when the input voltage falls below the falling threshold. The hysteresis between rising and falling threshold ensures proper startup.

Enable Input (EN / EN_HYS)

In addition to the UVLO, the device includes an EN pin which can enable or disable the device. When the input voltage is above the UVLO threshold and the voltage at EN pin is above $V_{TH_EN_ON}$ (1.22V), the device enters soft-start and ramps up the output voltage after a delay of 230μs. When the voltage at EN pin is below $V_{TH_EN_OFF}$ (1.15V), the device will be shut down. The hysteresis between $V_{TH_EN_ON}$ and $V_{TH_EN_OFF}$ is 70mV. The EN pin cannot be floated. If there is no need to control the EN function separately, connecting it to the V_{IN}.

EN_HYS is an open-drain output driven by EN comparator. EN_HYS is pulled to ground if the input voltage is above V_{UVLO_R} and the voltage at EN pin is below $V_{TH_EN_ON}$. When the voltage at EN pin is above $V_{TH_EN_ON}$, EN_HYS becomes high-impedance state. The EN_HYS can be used as an adjustable input supply voltage supervisor (SVS) to start and stop the DC/DC converter depending on the input voltage level.

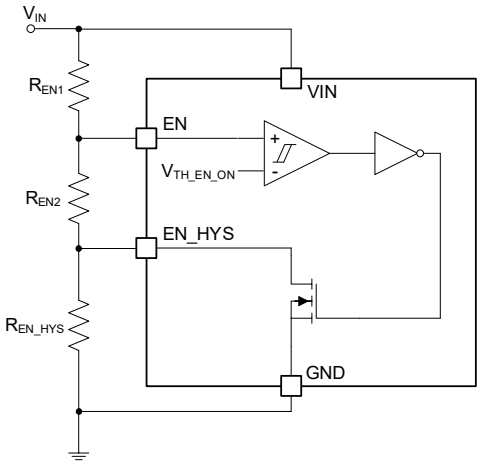


Figure 3. Using the Enable Comparator Threshold and Hysteresis

The input voltage level, $V_{IN_STARTUP}$, at which the device startup is set by the resistors R_{EN1} and R_{EN2} and can be calculated by:

$$V_{IN_STARTUP} = V_{TH_EN_ON} \times \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) = 1.22V \times \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) \quad (1)$$

After selecting R_{EN1}, R_{EN2} can be selected by:

$$R_{EN2} = R_{EN1} \times \frac{1.22V}{V_{IN_STARTUP} - 1.22V} \quad (2)$$

If R_{EN2} is selected first, R_{EN1} can be calculated by:

$$R_{EN1} = R_{EN2} \times \left(\frac{V_{IN_STARTUP}}{1.22V} - 1\right) \quad (3)$$

DETAILED DESCRIPTION (continued)

The input voltage level V_{IN_STOP} at which the device will stop operation is set by R_{EN1}, R_{EN2} and R_{EN_HYS} and can be calculated by:

$$V_{IN_STOP} = V_{TH_EN_OFF} \times \left(1 + \frac{R_{EN1}}{R_{EN2} + R_{EN_HYS}}\right) = 1.15V \times \left(1 + \frac{R_{EN1}}{R_{EN2} + R_{EN_HYS}}\right) \quad (4)$$

The resistor value R_{EN_HYS} can be calculated according to:

$$R_{EN_HYS} = R_{EN1} \times \frac{1.15}{V_{IN_STOP} - 1.15} - R_{EN2} \quad (5)$$

The current through the resistors R_{EN1}, R_{EN2}, and R_{EN_HYS} should be higher than 1μA. In applications operating over the full temperature range and in noisy environments, the resistor values can be reduced to smaller values.

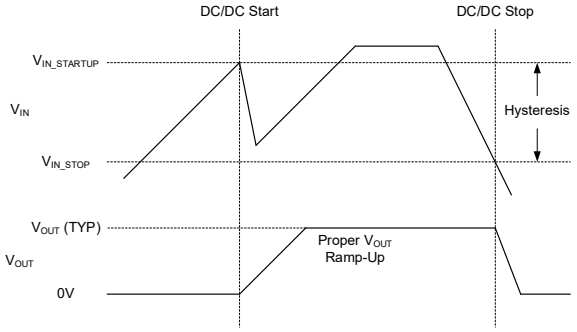


Figure 4. Using the EN Comparator as Input SVS for Proper V_{OUT} Ramp-Up

Soft Startup

A 460μs internal soft-start circuit is included to prevent input inrush current and voltage drops during startup. This circuit slowly ramps up the error amplifier reference voltage after exiting the shutdown state or under-voltage lockout (UVLO). Slow increase of the output voltage prevents the excessive inrush current for charging the output capacitors and creates a smooth output voltage rise. The other advantage of a soft-start is avoiding supply voltage drops especially on the high internal impedance sources such as the primary cells and rechargeable batteries.

The SGM61103 is also capable of starting with a pre-biased output capacitor when it is powered up or enabled. When the device is turned on, a bias on the output may exist due to the other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output may not drop during the off period and the device must restart under pre-biased output condition. The output ramp is automatically initiated with the bias voltage and ramps up to the nominal output value. Without the pre-biased capability, the device may not be able to start up properly.

Large output capacitors and high load currents may exceed the current capability of the device during startup. The high-side MOSFET switch current limit may be triggered during startup, and the maximum output current provided by device is half of the current limit I_{LIM}. In this case, the startup ramp of the output voltage will be slower.

Power Good Output

The PG pin is an open-drain output. PG requires a pull-up resistor. PG pin is pulled to GND before the output voltage is above 95% of the nominal voltage. After FB voltage reaches 95% of V_{REF}, the PG pin is pulled high immediately. When the FB voltage drops below 90% of V_{REF}, the PG pin will be pulled to GND. Leave the PG pin unconnected when not used. Table 1 shows how the PG state is changed in different conditions.

Table 1. PG Output Logic

Device Conditions		Logic Status	
		Hi-Z	Low
Enable	V_{EN} = High, $V_{FB} \geq V_{PG}$	√	
	V_{EN} = High, $V_{FB} \leq V_{PG}$		√
Shutdown	V_{EN} = Low		√
Thermal Shutdown	$T_A > T_{SD}$		√
UVLO (1)	$1.5V < V_{IN} < V_{UVLO}$		√
Power Supply Removal (1)	$V_{IN} \leq 1.5V$	Uncertainty	

NOTE: 1. PG is connected to VIN with 100kΩ.

The voltage connected to the pull-up resistor cannot exceed 10V. The PG output can sink current up to 0.4mA if the PG voltage is less than 0.3V. The lowest value for the pull-up resistor can be calculated by:

$$R_{PULL_UP_MIN} = \frac{V_{PG} - 0.3V}{0.0004A} \quad (6)$$

DETAILED DESCRIPTION (continued)

The PG pin can be used to discharge the output capacitor. The maximum sink current into the PG pin is 6mA. With the internal resistance R_{PG} of minimum 400Ω, the minimum pull-up resistor can be calculated by:

$$R_{PULL_UP_MIN} = \frac{V_{PG}}{I_{PG_MAX}} - R_{PG_MIN} = \frac{V_{PG}}{0.01A} - 400\Omega \quad (7)$$

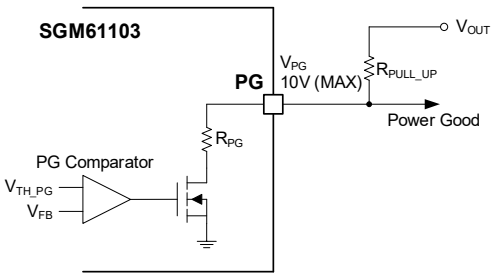


Figure 5. PG Open Collector Output

Pulse Width Modulation (PWM)

At moderate and heavy load condition, the SGM61103 operates in PWM mode with a switching frequency of about 1MHz. The switching frequency is slightly affected by V_{IN}, V_{OUT} and load condition. As the load current decreases, it automatically exits PWM mode when the inductor current is discontinuous.

Typically, the on-time in PWM can be calculated by:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{sw}} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{1MHz} \quad (8)$$

Then the peak current of inductor is:

$$I_{LP} = \frac{V_{IN} - V_{OUT}}{L} \times t_{ON} \quad (9)$$

where:
t_{ON}: On-time of High-side switch (μs)
V_{IN}: Input voltage (V)
V_{OUT}: Output voltage (V)
f_{SW}: Switching frequency in PWM (MHz)
L: Inductance (μH)
I_{LP}: Peak current of inductor (A)

Power-Save Mode (PSM)

At light load condition, the SGM61103 shifts to the PFM mode once the inductor current is discontinuous. If the load current further decreases, the SGM61103 enters into PSM mode when off time is longer than 8μs. The switching frequency is reduced automatically in both PFM and PSM mode.

In PSM mode, some internal control blocks are shut down to minimize the losses. One or a few PWM pulses are sent to charge the output capacitor and then the switches are kept off. The output capacitor voltage gradually drops due to small load current and when it falls below the nominal voltage threshold, the PWM pulses resume. If the load is still low, the output will go slightly higher than normal again and the switches will be turned off. In PSM mode, the switching frequency varies with the load current. Because of the decrease of frequency, the output voltage ripple is slightly higher than that in PWM. This effect can be mitigated by a larger output capacitor.

Low Dropout Operation (100% Duty Cycle)

When the input voltage reduces, the duty cycle increases to keep the output voltage constant. When the input voltage is lower than the regulation output voltage, the output voltage drops, and the SGM61103 goes into 100% duty cycle mode. The high-side switch is always on, and the output voltage is determined by the load current times the R_{DSON} composed by the high-side switch and inductor.

Current Limit Protection

Limiting the switch current protects the switch itself and also prevents over-current in the source and the inductor. If the high-side (HS) switch current exceeds the I_{LIM} threshold, HS switch is turned off and the low-side (LS) switch will be turned on to reduce the inductor current and limit the peak value. The HS switch is turned on again once the inductor current drops to zero. At this time, the maximum output current that the device can provide is about half of the I_{LIM}.

Note that the measured peak current limit in the closed-loop and open-loop test conditions is slightly different, mainly due to the current comparator propagation delay.

Thermal Shutdown Protection

A thermal shutdown function is implemented to prevent damage caused by excessive heat and power dissipation. Once the junction temperature exceeds +150℃, the device is shut down. The device is released from shutdown automatically when the junction temperature decreases by 20℃.

APPLICATION INFORMATION

In this section, power supply design with the SGM61103 synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.

Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 6. The selected components are given in Table 3.

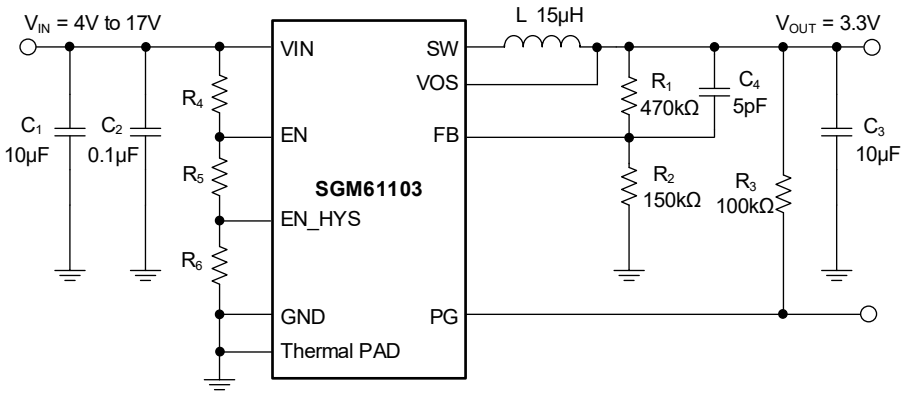


Figure 6. SGM61103 Application Example with 3.3V/300mA Output

Table 2. Design Parameters for the Application Example

Design Parameter	Example Value
Input Voltage	4V to 17V
Output Voltage	3.3V
Output Current	≤ 300mA
Output Ripple Voltage	< 30mV

Table 3. Selected Components for the Design Example

Ref	Description
C_1	10μF, 25V, X5R, 0805, Ceramic
C_2	0.1μF, 25V, X5R, 0603, Ceramic
C_3	10μF, 16V, X5R, 0805, Ceramic
C_4	5pF, 50V, C0G, 0603, Ceramic
L	15μH, DCR_{TYP} = 210mΩ, $I_{SAT(30\%)}$ = 1.1A, $I_{RMS(40℃)}$ = 0.85A
R_1	470kΩ, 1%, 0603, 1/16W Chip Resistor
R_2	150kΩ, 1%, 0603, 1/16W Chip Resistor
R_3	100kΩ, 5%, 0603, 1/16W Chip Resistor

Input Capacitor Selection (C_{IN})

High frequency decoupling input capacitors with low ESR are needed to circulate and absorb the high frequency switching currents of the converter. Place this capacitor right beside the VIN and GND pins. A 10μF ceramic capacitor with X5R or better dielectric and 0805 or smaller size is sufficient in most cases. A larger value can be selected to reduce the input current ripple.

Inductor Selection (L)

The important factors for inductor selection are inductance (L), saturation current (I_{SAT}), RMS rating (I_{RMS}), DC resistance (DCR) and dimensions. Use Equation 10 and 11 to find the inductor peak current (I_{L_MAX}) and peak-to-peak ripple current (ΔI_L) in static conditions:

$$I_{L_MAX} = I_{O_MAX} + \frac{\Delta I_L}{2} \quad (10)$$

$$\Delta I_L = V_{OUT} \times \frac{1-D}{L \times f_{SW}} \quad (11)$$

where:

I_{O_MAX}: Maximum load current

D: Duty cycle

f_{SW}: Switching frequency in PWM

I_{SAT} should be higher than I_{L_MAX}, and sufficient margin should be reserved. More generally, the saturation current above high-side current limit is enough. Increasing the inductance can lower the ripple current and RMS current. However, for inductors of the same series and package, the larger the inductance, the smaller the saturation current and the larger the DCR. A larger inductance also reduces dynamic response.

APPLICATION INFORMATION (continued)

In applications that focus on high efficiency, it is also necessary to consider the impact of AC resistance on power supply efficiency. Usually, an inductor with quality factor > 25 at the switching frequency is selected, which can be used to characterize the AC resistance characteristic of inductor.

Output Voltage Setting

An external resistor divider connected to FB pin is used for setting the output voltage. Through adjusting R_1 and R_2, the output voltage can be programmed to the desired value. It is recommended to use 1% resistor to achieve good output accuracy. Calculate R_1 and R_2 with Equation 12.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.8 \times \left(1 + \frac{R_1}{R_2}\right) \quad (12)$$

The current flowing through R_2 should be higher than the current 1μA. A lower value of R_2 increases the robustness against noise injection, and higher values reduce the current consumption, which can impact the light load efficiency.

A feed-forward capacitor is recommended to improve the performance of smooth transition into power-save mode and reduce undershoot during load transient. 5pF is enough for typical applications.

Output Capacitor Selection (C_{OUT})

This device is capable of operating with low ESR ceramic capacitors to get low voltage ripple and fast response. 10μF to 22μF capacitors with X7R or X5R dielectric type are recommended. Minimum capacitance of output ripple criteria can be calculated from Equation 13.

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT_RIPPLE}} \quad (13)$$

For output capacitor selection, transient response and loop stability should also be considered. Bias voltage may cause significant capacitance drops in the ceramic capacitors. The effective deviation of a ceramic capacitor can be as high as -50% to +20% of the nominal value.

Additional Typical Application Circuit

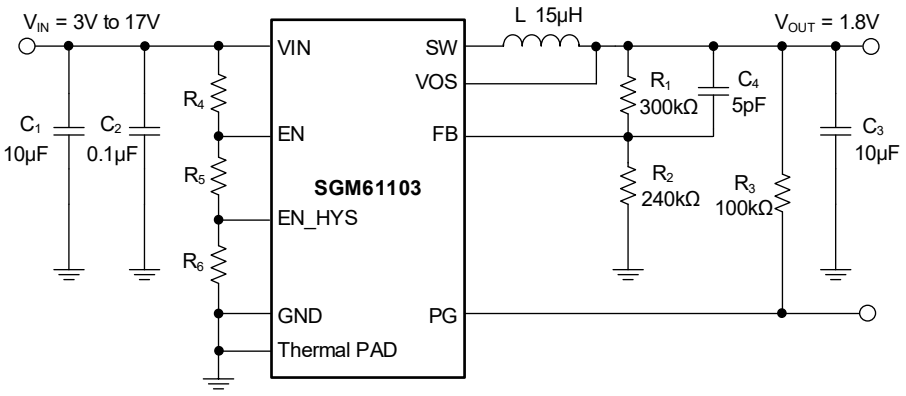


Figure 7. Additional Typical Application Circuit with 1.8V Output

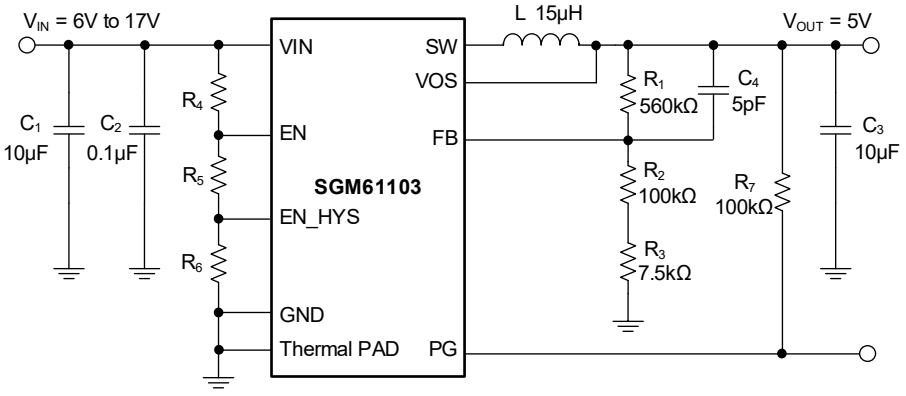


Figure 8. Additional Typical Application Circuit with 5V Output

APPLICATION INFORMATION (continued)

Layout Guidelines

A good printed-circuit-board (PCB) layout is a critical element of any high performance design. Follow the guidelines below for designing a good layout for the SGM61103.

- Place the input capacitor close to the device with the shortest possible connection traces to minimize the AC current loop.
- Share the same GND return point for the input and output capacitors and locate it as close as possible to the device GND pin to minimize the AC current loops. Place the inductor close to the switching node and connect it with a short trace to minimize the parasitic capacitances coupled to the SW node.
- Keep the signal traces like the FB sense line away from SW or other noisy sources.
- The VOS line should be connected as short as possible to the output, ideally to the VOUT pin terminal of the inductor.
- The exposed thermal pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation.

Refer to Figure 9 for a recommended PCB layout.

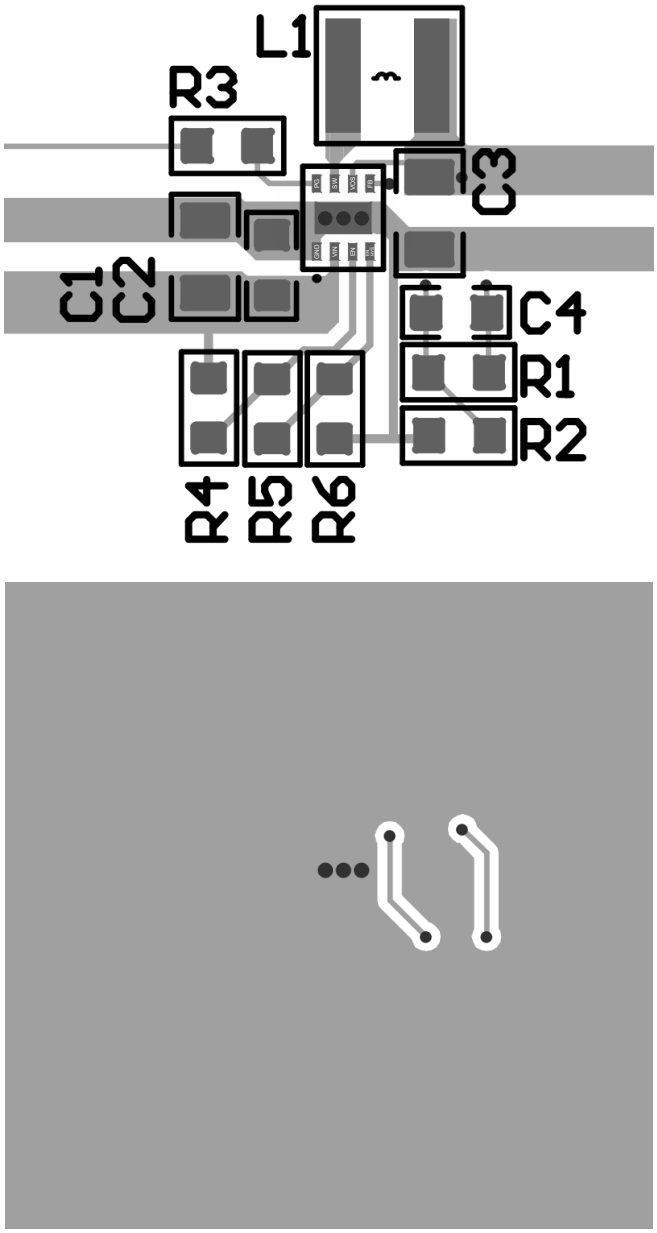


Figure 9. Layout

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

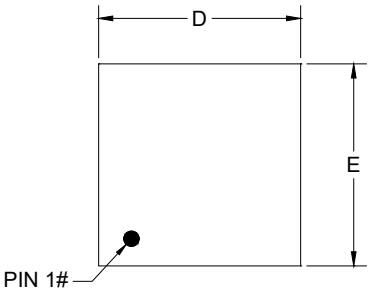
JUNE 2026 – REV.A.1 to REV.A.2	Page
Updated PACKAGE/ORDERING INFORMATION and TAPE AND REEL INFORMATION (Q2)	2, 23

AUGUST 2024 – REV.A to REV.A.1	Page
Added Package Thermal Resistance section	2
Updated Package Outline Dimensions	21

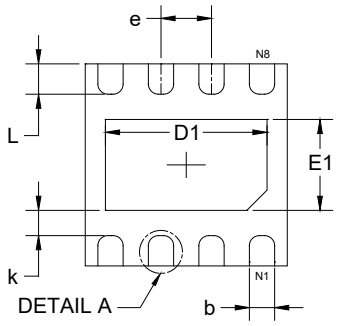
Changes from Original to REV.A (DECEMBER 2023)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

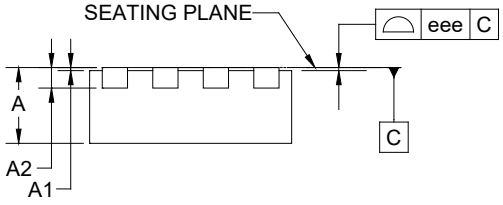
TDFN-2×2-8AL



TOP VIEW



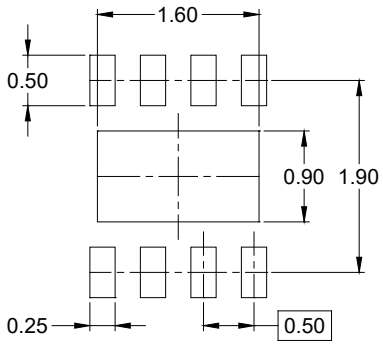
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



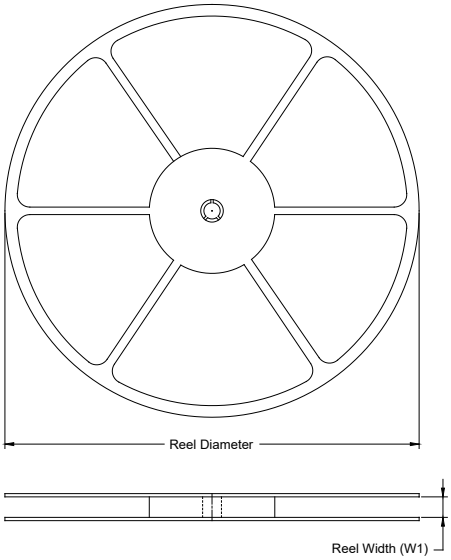
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	1.900	-	2.100
D1	1.450	-	1.700
E	1.900	-	2.100
E1	0.750	-	1.000
k	0.200	-	-
e	0.500 BSC		
L	0.200	-	0.400
eee	0.080		

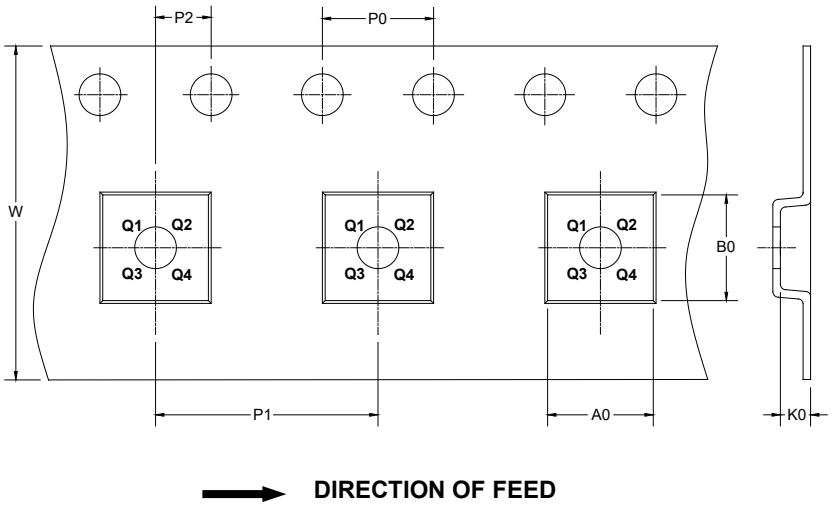
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



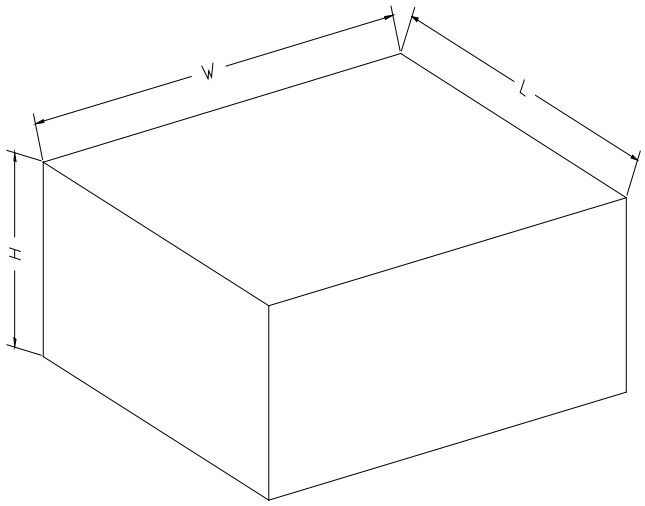
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-8AL (SGM61103XTDE8G)	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1
TDFN-2×2-8AL (SGM61103XTDE8DG)	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002