# SGM6037
# 2.4V to 5.5V Input, 4A/6A Synchronous Buck Converter with I²C Interface

## GENERAL DESCRIPTION

The SGM6037 is a family of high power density synchronous Buck converters which are capable of delivering up to 4A/6A continuous output current from 2.4V to 5.5V input voltage range. The device only consumes 5μA (TYP) quiescent current.

The SGM6037 implements an I²C interface to further enhance the device's flexibility and ease of use to adapt for various application needs. The device implements auto PFM mode operation to maximize the efficiency at light load condition. At moderate to heavy loads, the device automatically switches to CCM operation with a 2.3MHz (TYP) switching frequency. FPWM operation is also available via I²C programming for low output voltage ripple requirement.

The SGM6037 implements the constant on-time (COT) architecture that incorporates the benefits of fast load and line transient responses and low output voltage ripple, which is beneficial for RF and noise sensitive applications.

The SGM6037 family of devices offers VID option for dynamic voltage scaling (DVS) via the I²C interface, which can adjust the output voltage rapidly to adapt for any changes on the load side. Another variant of the device offers an active-low power good (PG) function.

The SGM6037 is available in a Green WLCSP-1.05×1.78-15B package.

## APPLICATIONS

Core Supply for FPGAs, CPUs, ASICs or GPUs
DDR Memory
Optical Modules
Solid-State Drives

## FEATURES

- **2.4V to 5.5V Input Voltage Range**
- **5μA (TYP) Quiescent Current**
- **2.3MHz (TYP) Switching Frequency**
- **2% Output Voltage Accuracy**
- **15mΩ and 9.8mΩ Internal Power MOSFETs**
- **90% Efficiency at 0.9V Output**
- **COT-Control Architecture for Fast Transient Response**
- **Output Current:**
  - **SGM6037A: 4A (VSET/VID Pin)**
  - **SGM6037B: 4A (VSET/nPG Pin)**
  - **SGM6037C: 6A (VSET/VID Pin)**
  - **SGM6037D: 6A (VSET/nPG Pin)**
- **Selection by External Resistor**
  - **I²C Slave Address**
  - **Start-up Output Voltage**
- **Selection by I²C Interface**
  - **Output Discharge**
  - **Output Voltage Ramp Speed**
  - **Power-Save Mode or Forced PWM Mode**
  - **Hiccup or Latching Short-Circuit Protection**
- **VID Option for Dynamic Voltage Scaling (DVS)**
- **Thermal Warning and Shutdown**
- **Power Good Indicator Pin Option**
- **Up to 3.4Mbps I²C Compatible Interface**
- **Available in a Green WLCSP-1.05×1.78-15B Package**

## SIMPLIFIED SCHEMATIC

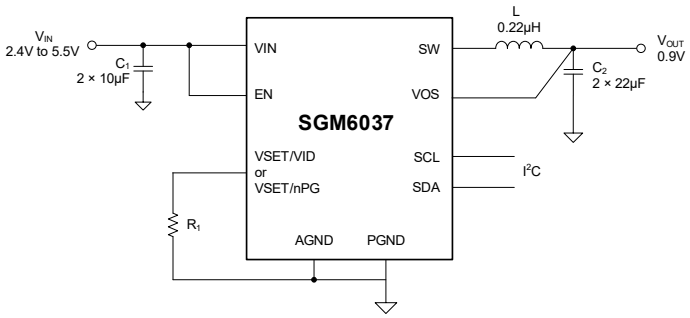


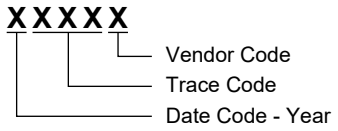

**Figure 1. Simplified Schematic**

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM6037A | WLCSP-1.05×1.78-15B | -40℃ to +125℃ | SGM6037AXG/TR | XXXXX<br>6037A | Tape and Reel, 3500 |
| SGM6037B | WLCSP-1.05×1.78-15B | -40℃ to +125℃ | SGM6037BXG/TR | XXXXX<br>6037B | Tape and Reel, 3500 |
| SGM6037C | WLCSP-1.05×1.78-15B | -40℃ to +125℃ | SGM6037CXG/TR | XXXXX<br>6037C | Tape and Reel, 3500 |
| SGM6037D | WLCSP-1.05×1.78-15B | -40℃ to +125℃ | SGM6037DXG/TR | XXXXX<br>6037D | Tape and Reel, 3500 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

# DEVICE DESCRIPTION

| Part Number | Start-up Output Voltage | Output Current | VSET/VID or VSET/nPG Pin |
|---|---|---|---|
| SGM6037A | 0.4V to 1.15V, Selectable | 4A | VSET/VID |
| SGM6037B | | | VSET/nPG |
| SGM6037C | | 6A | VSET/VID |
| SGM6037D | | | VSET/nPG |

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{IN}$ ..... -0.3V to 6V
EN, SDA, SCL, VOS Voltages ..... -0.3V to 6V
VSET/VID, VSET/nPG Voltages ..... -0.3V to 6V
SW, DC Voltages ..... -0.3V to $V_{IN}$ + 0.3V
SW, AC (10ns Transient), while Switching ..... -2.5V to 10V
Source Current at VSET/nPG, $I_{SOURCE_VSET/nPG}$ ..... 1mA
Sink Current at SDA, SCL, $I_{SINK_SDA/SCL}$ ..... 2mA
Package Thermal Resistance
WLCSP-1.05×1.78-15B, $\theta_{JA}$ ..... 63.2℃/W
WLCSP-1.05×1.78-15B, $\theta_{JB}$ ..... 16.5℃/W
WLCSP-1.05×1.78-15B, $\theta_{JC}$ ..... 32.5℃/W
Operating Junction Temperature ..... -40℃ to +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

## RECOMMENDED OPERATING CONDITIONS

Supply Voltage, $V_{IN}$ ..... 2.4V to 5.5V
Falling Transition Time at VIN Pin, $t_{VIN_F}$ (1) ..... 10mV/μs
SGM6037A/B: Output Current, $I_{OUT}$ (2) ..... 0A to 4A
SGM6037C/D: Output Current, $I_{OUT}$ (3) ..... 0A to 6A
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTES:
1. The falling slew rate of $V_{IN}$ should be limited if $V_{IN}$ goes below $V_{UVLO}$.
2. Lifetime is reduced when operating continuously at 4A output current and the junction temperature is higher than +105℃.
3. Lifetime is reduced when operating continuously at 6A output current and the junction temperature is higher than +85℃.

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

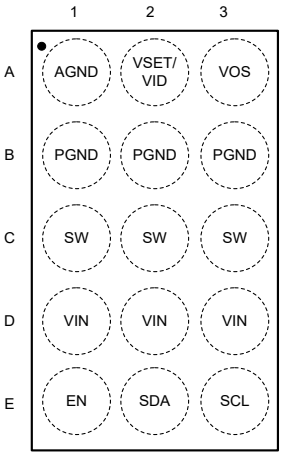
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

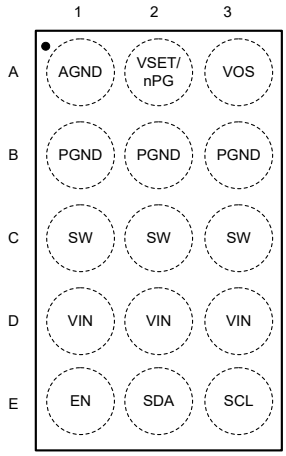
## PIN CONFIGURATIONS

**SGM6037A/C (TOP VIEW)**




**WLCSP-1.05×1.78-15B**

**SGM6037B/D (TOP VIEW)**




**WLCSP-1.05×1.78-15B**

## PIN DESCRIPTION

| PIN | NAME | TYPE | FUNCTION |
|---|---|---|---|
| A1 | AGND | G | Analog Ground Pin. |
| A2 | VSET/VID | I/O | I²C Address Selection and Start-up Voltage Selection Pin. An external resistor connected to this pin programs the start-up voltage. Logic low selects the VOUT register 1 (**REG0x01**), and logic high selects the VOUT register 2 (**REG0x02**). |
| | VSET/nPG | I/O | I²C Address Selection and Start-up Voltage Selection Pin. An external resistor connected to this pin programs the start-up voltage. After start-up, this pin is an active-low power good pin. When output voltage is within regulation, this pin is pulled low through the external resistor. |
| A3 | VOS | P | Output Voltage Sense Input. This pin is internally connected to the feedback loop and a MOSFET to discharge the output ($V_{OUT}$) when the device is disabled. Connect it with a short trace to the output capacitor. |
| B1, B2, B3 | PGND | G | Power Ground Pin. |
| C1, C2, C3 | SW | P | Switching Node Pin. This pin is connected to the internal MOSFET switches. Connect the inductor to this terminal. |
| D1, D2, D3 | VIN | P | Power Supply Input. Connect a ceramic capacitor ($C_{IN}$) close to this pin and PGND. |
| E1 | EN | I | Device Enable Pin. Logic high on this pin enables the device, and logic low on this pin disables the device. Do not leave it floating. |
| E2 | SDA | I/O | I²C Bus Data Signal. Do not leave it floating. Connect it to AGND if not used. |
| E3 | SCL | I | I²C Bus Clock Signal. Do not leave it floating. Connect it to AGND if not used. |

NOTE: I = input, O = output, I/O = input/output, P = power, G = ground.

## ELECTRICAL CHARACTERISTICS

($T_J$ = -40℃ to +125℃, $V_{IN}$ = 2.4V to 5.5V, all typical values are measured at $T_J$ = +25℃ and $V_{IN}$ = 3.7V, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| Quiescent Current | $I_Q$ | EN = High, no load, device not switching | | 5 | 15.5 | μA |
| Shutdown Current | $I_{SD}$ | $T_J$ = -40℃ to +85℃, EN = low | | 0.1 | 1.7 | μA |
| Under-Voltage Lockout Threshold | $V_{UVLO}$ | $V_{IN}$ rising | 2.0 | 2.2 | 2.4 | V |
| | | $V_{IN}$ falling | 1.9 | 2.1 | 2.3 | |
| Thermal Warning Threshold | $T_{JW}$ | $T_J$ rising | | 130 | | ℃ |
| Thermal Warning Hysteresis | | $T_J$ falling | | 20 | | |
| Thermal Shutdown Threshold | $T_{SD}$ | $T_J$ rising | | 150 | | ℃ |
| Thermal Shutdown Hysteresis | | $T_J$ falling | | 20 | | |
| **Logic Interface EN, SDA, SCL and VSET/VID** | | | | | | |
| High-Level Input Threshold Voltage at EN, SCL, SDA, VSET/VID | $V_{IH}$ | | 0.9 | | | V |
| Low-Level Input Threshold Voltage at EN, SCL, SDA, VSET/VID | $V_{IL}$ | | | | 0.3 | V |
| Input Leakage Current into SCL Pin | $I_{SCL_LKG}$ | | | 0.01 | 0.30 | μA |
| Input Leakage Current into SDA Pin | $I_{SDA_LKG}$ | | | 0.01 | 0.30 | μA |
| Input Leakage Current into EN Pin | $I_{EN_LKG}$ | | | 0.03 | 0.33 | μA |
| Parasitic Capacitance at SCL | $C_{SCL}$ | | | 1 | | pF |
| Parasitic Capacitance at SDA | $C_{SDA}$ | | | 2 | | pF |
| **Start-up, Power Good** | | | | | | |
| Enable Delay Time | $t_{DELAY}$ | Time from EN high to device starts switching, $R_1$ = 249kΩ | 340 | 640 | 950 | μs |
| Output Voltage Ramp Time | $t_{RAMP}$ | Time from device starts switching to power good | 0.48 | 1.5 | 2.7 | ms |
| Power Good Lower Threshold | $V_{PG}$ | $V_{VOS}$ referenced to $V_{OUT}$ nominal | 85 | 91 | 97 | % |
| Power Good Upper Threshold | | $V_{VOS}$ referenced to $V_{OUT}$ nominal | 105 | 111 | 118 | % |
| Power Good Deglitch Delay | $t_{PG_DLY}$ | Rising and falling edges | | 48 | | μs |
| **Output** | | | | | | |
| Output Voltage Accuracy | $V_{OUT}$ | $T_J$ = -40℃ to +125℃, $V_{OUT}$ ≥ 1.15V, FPWM, no Load | -2.0 | | 2.0 | % |
| | | $T_J$ = -40℃ to +125℃, 0.9V ≤ $V_{OUT}$ < 1.15V, FPWM, no Load | -2.3 | | 2.3 | |
| | | $T_J$ = -40℃ to +125℃, 0.59V ≤ $V_{OUT}$ < 0.9V, FPWM, no Load | -3.3 | | 3.3 | |
| | | $T_J$ = -40℃ to +125℃, $V_{OUT}$ < 0.59V, FPWM, no Load | -4.8 | | 4.8 | |
| Input Leakage Current into VOS Pin | $I_{VOS_LKG}$ | EN = high, $V_{VOS}$ = 1.8V | | 1 | | μA |
| | | EN = low, output discharge disabled, $V_{VOS}$ = 1.8V | | 0.1 | 0.5 | |
| Output Discharge Resistor at VOS Pin | $R_{DIS}$ | | | 17 | 25 | Ω |
| Load Regulation | | $V_{OUT}$ = 0.9V, FPWM | | 0.18 | | %/A |
| **Power Switch** | | | | | | |
| High-side FET On-Resistance | $R_{DSON}$ | | | 15 | | mΩ |
| Low-side FET On-Resistance | | | | 9.8 | | |
| High-side FET Forward Current Limit | $I_{LIM}$ | SGM6037A and SGM6037B | 5.5 | 7.4 | 8.8 | A |
| | | SGM6037C and SGM6037D | 6.9 | 10.2 | 12.1 | |
| Low-side FET Forward Current Limit | | SGM6037A and SGM6037B | | 5.8 | | A |
| | | SGM6037C and SGM6037D | | 7.3 | | |
| Low-side FET Negative Current Limit | | SGM6037A, SGM6037B, SGM6037C and SGM6037D | | -2.6 | | A |
| PWM Switching Frequency | $f_{SW}$ | $I_{OUT}$ = 1A, $V_{OUT}$ = 0.9V | | 2.3 | | MHz |

## I²C INTERFACE TIMING CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SCL Clock Frequency | $f_{SCL}$ | Standard mode | | | 100 | kHz |
| | | Fast mode | | | 400 | kHz |
| | | Fast mode plus | | | 1 | MHz |
| | | High-speed mode (write operation), $C_B$ - 100pF (MAX) (1) | | | 3.4 | MHz |
| | | High-speed mode (read operation), $C_B$ - 10pF (MAX) (1) | | | 3.4 | MHz |
| | | High-speed mode (write operation), $C_B$ - 400pF (MAX) (1) | | | 1.7 | MHz |
| | | High-speed mode (read operation), $C_B$ - 400pF (MAX) (1) | | | 1.7 | MHz |
| Bus Free Time between a Stop and Start Condition | $t_{BUF}$ | Standard mode | 4.7 | | | μs |
| | | Fast mode | 1.3 | | | μs |
| | | Fast mode plus | 0.5 | | | μs |
| Hold Time (Repeated) Start Condition | $t_{HD}$, $t_{STA}$ | Standard mode | 4 | | | μs |
| | | Fast mode | 600 | | | ns |
| | | Fast mode plus | 260 | | | ns |
| | | High-speed mode | 160 | | | ns |
| Low Period of the SCL Clock | $t_{LOW}$ | Standard mode | 4.7 | | | μs |
| | | Fast mode | 1.3 | | | μs |
| | | Fast mode plus | 0.5 | | | μs |
| | | High-speed mode, $C_B$ - 100pF (MAX) | 160 | | | ns |
| | | High-speed mode, $C_B$ - 400pF (MAX) | 320 | | | ns |
| High Period of the SCL Clock | $t_{HIGH}$ | Standard mode | 4 | | | μs |
| | | Fast mode | 600 | | | ns |
| | | Fast mode plus | 260 | | | ns |
| | | High-speed mode, $C_B$ - 100pF (MAX) (1) | 60 | | | ns |
| | | High-speed mode, $C_B$ - 400pF (MAX) (1) | 120 | | | ns |
| Setup Time for a Repeated Start Condition | $t_{SU}$, $t_{STA}$ | Standard mode | 4.7 | | | μs |
| | | Fast mode | 600 | | | ns |
| | | Fast mode plus | 260 | | | ns |
| | | High-speed mode | 160 | | | ns |
| Data Setup Time | $t_{SU}$, $t_{DAT}$ | Standard mode | 250 | | | ns |
| | | Fast mode | 100 | | | ns |
| | | Fast mode plus | 50 | | | ns |
| | | High-speed mode | 10 | | | ns |
| Data Hold Time | $t_{HD}$, $t_{DAT}$ | Standard mode | 0 | | 3.45 | μs |
| | | Fast mode | 0 | | 0.9 | μs |
| | | Fast mode plus | 0 | | | μs |
| | | High-speed mode, $C_B$ - 100pF (MAX) | 0 | | 70 | ns |
| | | High-speed mode, $C_B$ - 400pF (MAX) | 0 | | 150 | ns |

NOTE:

1. High-speed mode (3.4Mbps) is supported but not fully compliant with I²C standard.

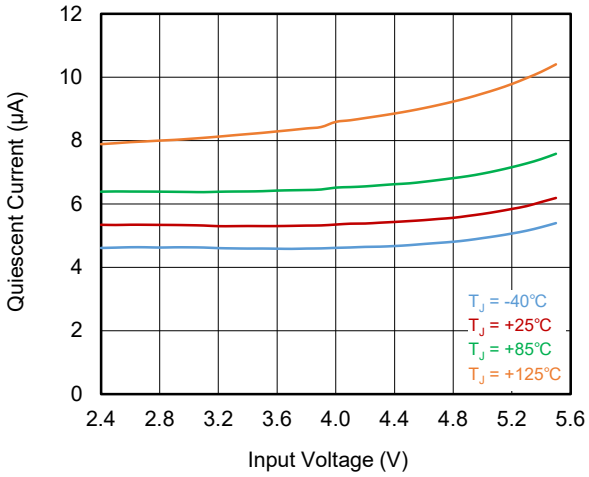
## I²C INTERFACE TIMING CHARACTERISTICS (continued)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Rise Time of SCL Signal | $t_{RCL}$ | Standard mode | | | 1000 | ns |
| | | Fast mode | 20 + 0.1 $C_B$ | | 300 | ns |
| | | Fast mode plus | | | 120 | ns |
| | | High-speed mode, $C_B$ - 100pF (MAX) | 10 | | 40 | ns |
| | | High-speed mode, $C_B$ - 400pF (MAX) | 20 | | 80 | ns |
| Rise Time of SCL Signal after a Repeated Start Condition and after an Acknowledge BIT | $t_{RCL1}$ | Standard mode | 20 + 0.1 $C_B$ | | 1000 | ns |
| | | Fast mode | 20 + 0.1 $C_B$ | | 300 | ns |
| | | Fast mode plus | | | 120 | ns |
| | | High-speed mode, $C_B$ - 100pF (MAX) | 10 | | 80 | ns |
| | | High-speed mode, $C_B$ - 400pF (MAX) | 20 | | 160 | ns |
| Fall Time of SCL Signal | $t_{FCL}$ | Standard mode | 20 + 0.1 $C_B$ | | 300 | ns |
| | | Fast mode | | | 300 | ns |
| | | Fast mode plus | | | 120 | ns |
| | | High-speed mode, $C_B$ - 100pF (MAX) | 10 | | 40 | ns |
| | | High-speed mode, $C_B$ - 400pF (MAX) | 20 | | 80 | ns |
| Rise Time of SDA Signal | $t_{RDA}$ | Standard mode | | | 1000 | ns |
| | | Fast mode | 20 + 0.1 $C_B$ | | 300 | ns |
| | | Fast mode plus | | | 120 | ns |
| | | High-speed mode, $C_B$ - 100pF (MAX) | 10 | | 80 | ns |
| | | High-speed mode, $C_B$ - 400pF (MAX) | 20 | | 160 | ns |
| Fall Time of SDA Signal | $t_{FDA}$ | Standard mode | | | 300 | ns |
| | | Fast mode | 20 + 0.1 $C_B$ | | 300 | ns |
| | | Fast mode plus | | | 120 | ns |
| | | High-speed mode, $C_B$ - 100pF (MAX) | 10 | | 80 | ns |
| | | High-speed mode, $C_B$ - 400pF (MAX) | 20 | | 160 | ns |
| Setup Time of STOP Condition | $t_{SU}$, $t_{STO}$ | Standard mode | 4 | | | μs |
| | | Fast mode | 600 | | | ns |
| | | Fast mode plus | 260 | | | ns |
| | | High-speed mode | 160 | | | ns |
| Capacitive Load for SDA and SCL | $C_B$ | Standard mode | | | 400 | pF |
| | | Fast mode | | | 400 | pF |
| | | Fast mode plus | | | 550 | pF |
| | | High-speed mode | | | 400 | pF |

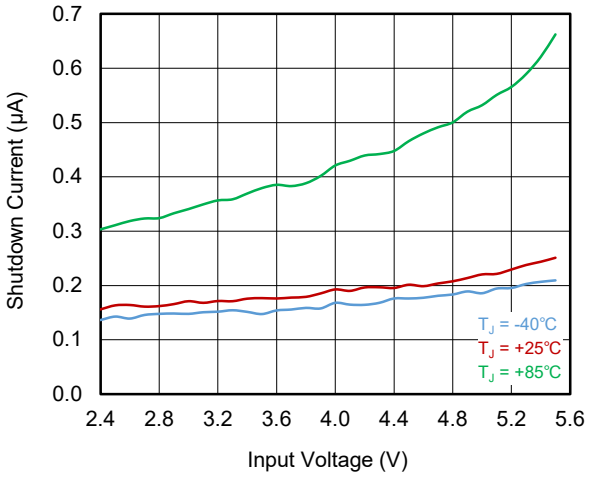
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = +25℃, $V_{IN}$ = 5.0V, $V_{OUT}$ = 0.9V, unless otherwise noted.

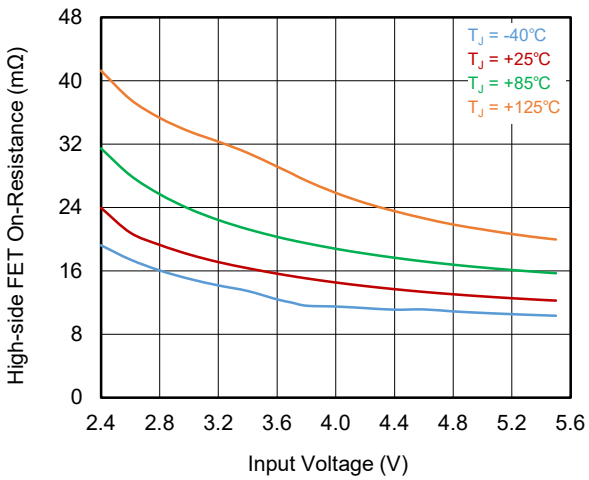
Quiescent Current vs. Input Voltage



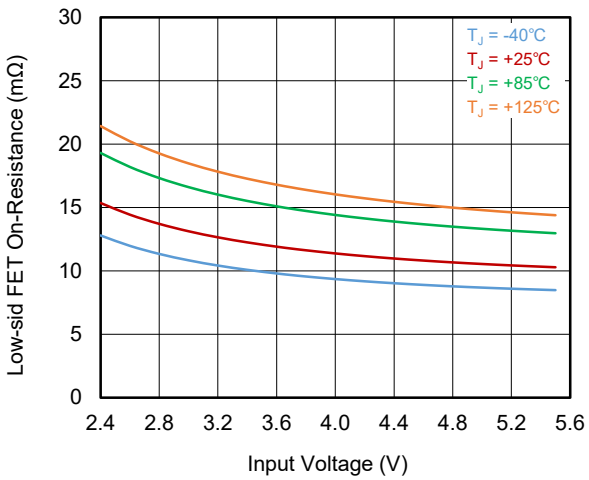

Shutdown Current vs. Input Voltage



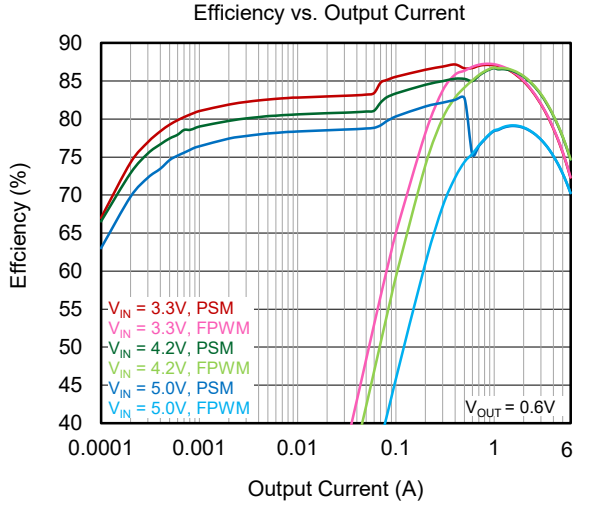

High-side FET On-Resistance vs. Input Voltage



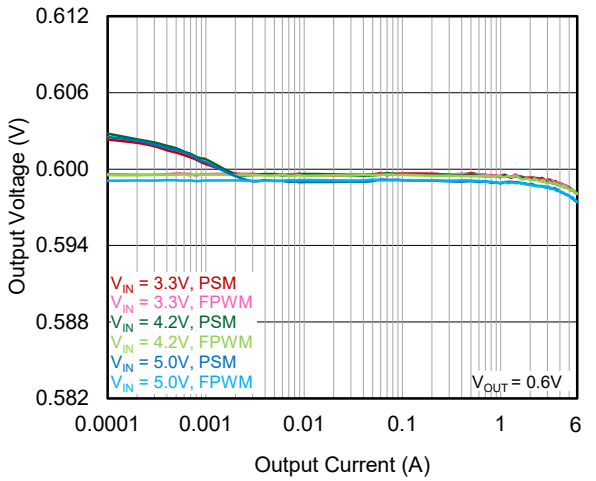

Low-side FET On-Resistance vs. Input Voltage




Efficiency vs. Output Current



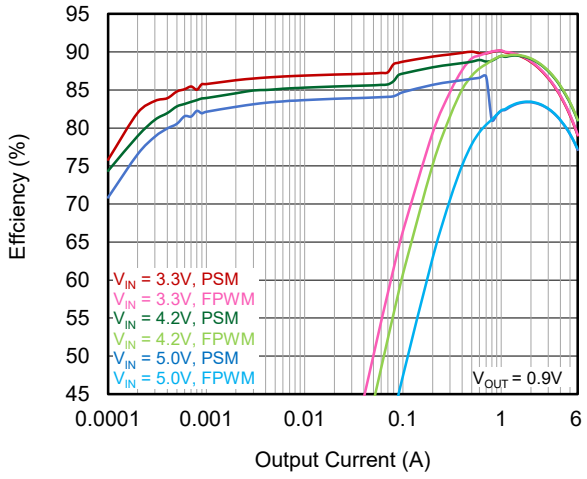

Output Voltage vs. Output Current



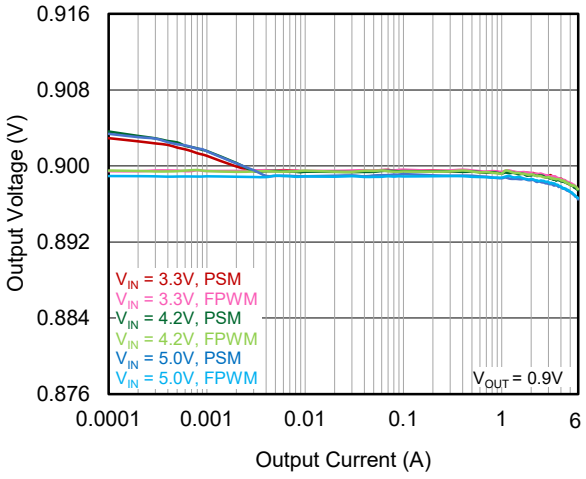
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$ = +25℃, $V_{IN}$ = 5.0V, $V_{OUT}$ = 0.9V, unless otherwise noted.

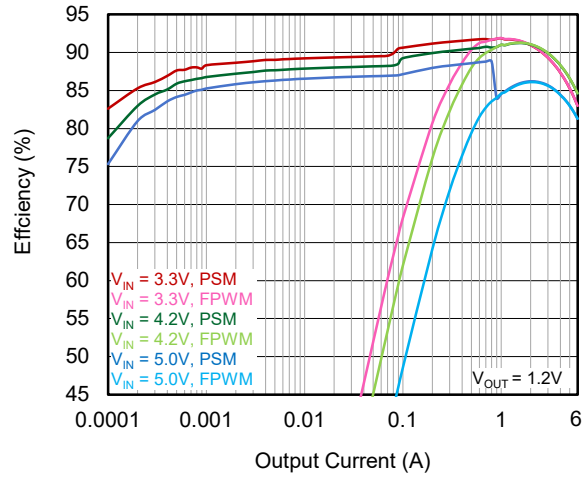
Efficiency vs. Output Current



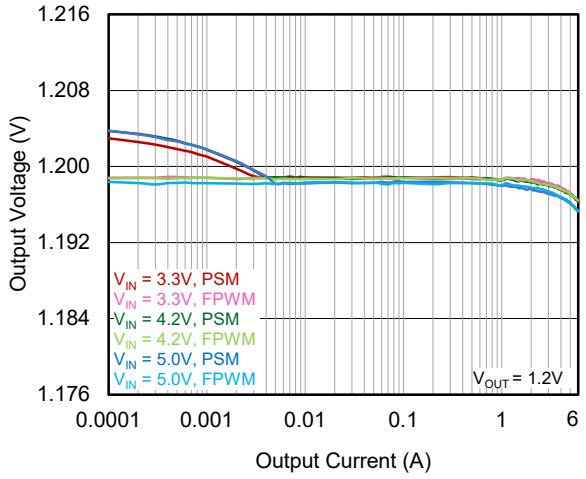

Output Voltage vs. Output Current



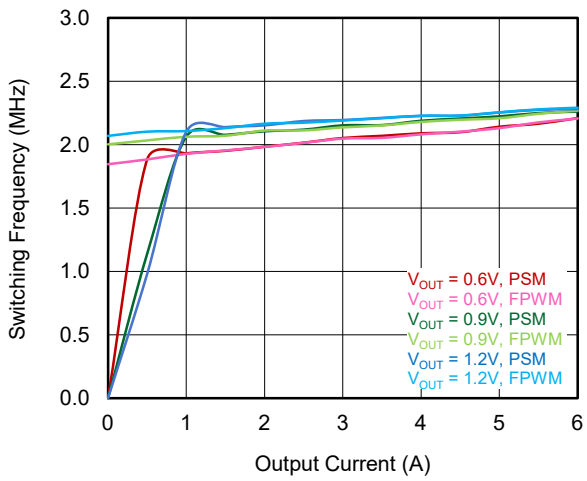

Efficiency vs. Output Current



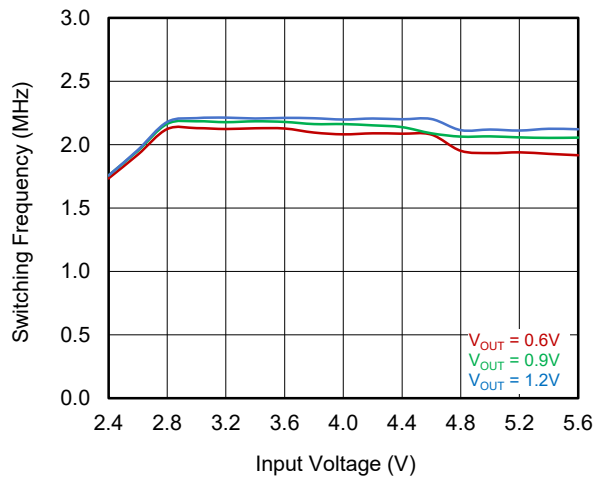

Output Voltage vs. Output Current




Switching Frequency vs. Output Current



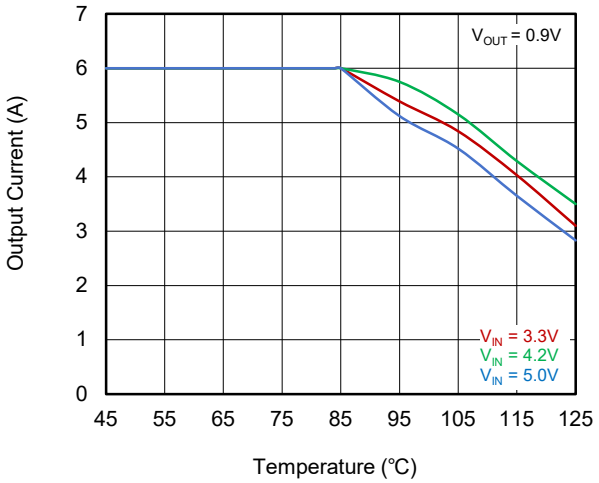

Switching Frequency vs. Input Voltage



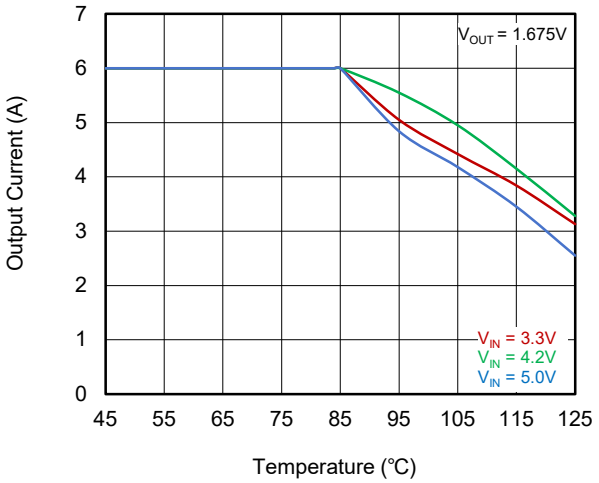
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$ = +25℃, $V_{IN}$ = 5.0V, $V_{OUT}$ = 0.9V, unless otherwise noted.

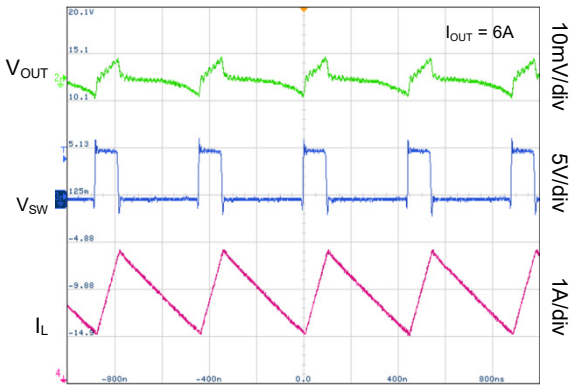
Output Current vs. Temperature




Output Current vs. Temperature

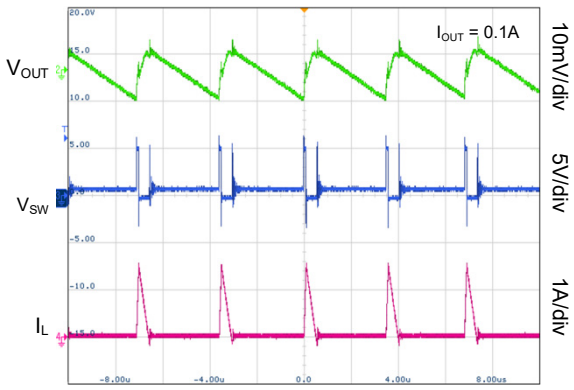



PWM Operation



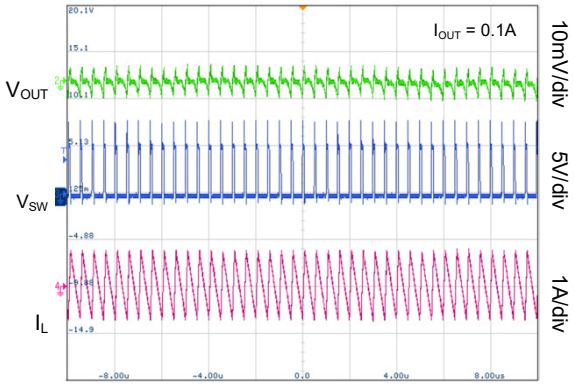

Time (200ns/div)

PSM Operation



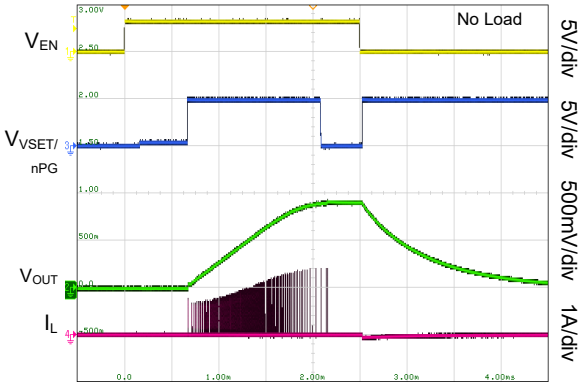

Time (2μs/div)

Forced PWM Operation




Time (2μs/div)

Start-up and Shutdown by EN Pin

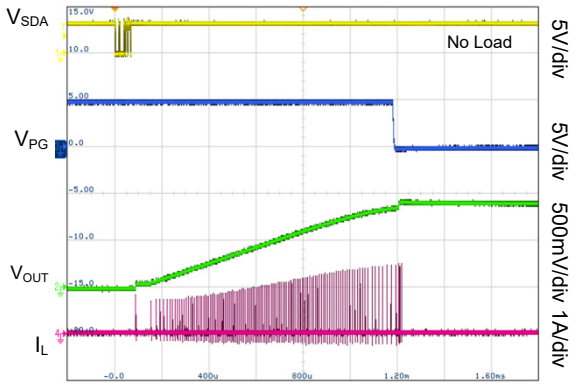



Time (500μs/div)

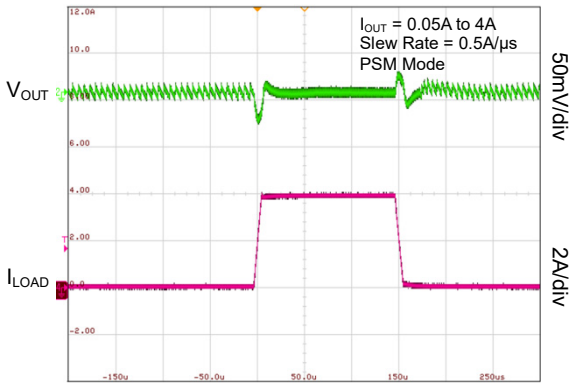
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$ = +25℃, $V_{IN}$ = 5.0V, $V_{OUT}$ = 0.9V, unless otherwise noted.

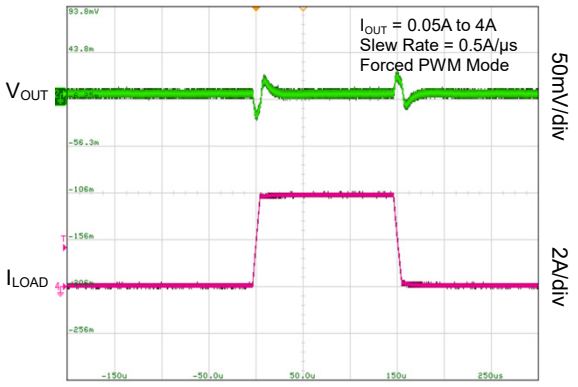
Start-up by Software Enable Device Bit



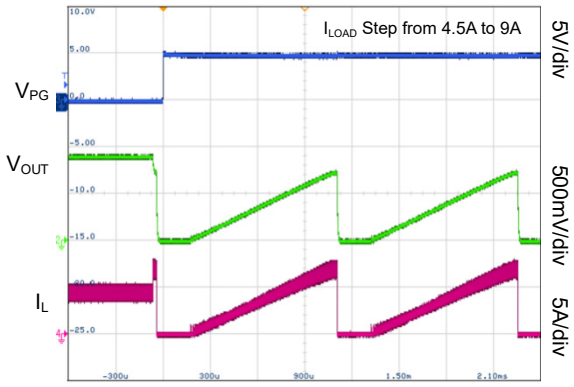

Load Transient



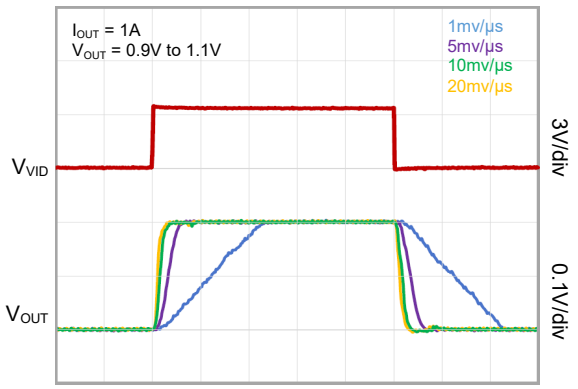

Load Transient




HICCUP Protection




VOUT Transition with Different Slew Rate Settings



## FUNCTIONAL BLOCK DIAGRAM

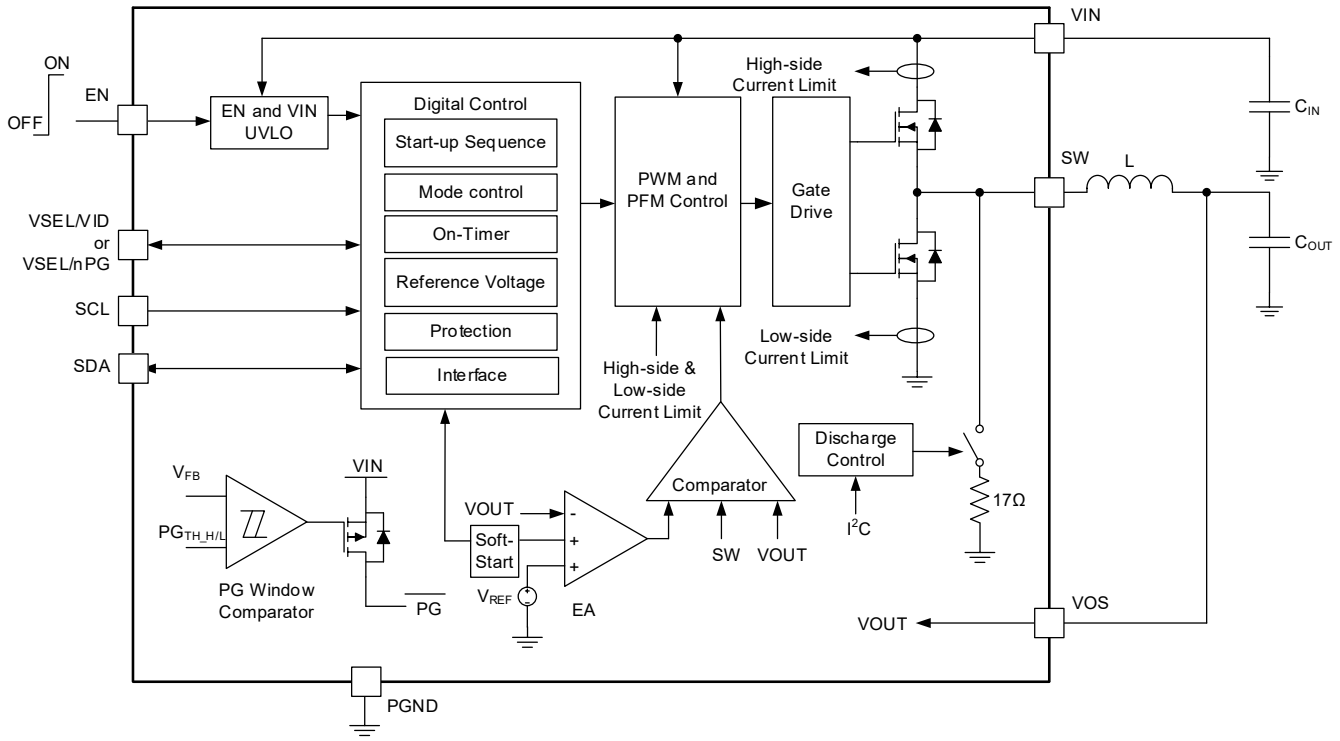



**Figure 2. Block Diagram**

# DETAILED DESCRIPTION

## Overview

The SGM6037 family of synchronous Buck converter consumes 5μA (TYP) quiescent current and offers up to 6A of DC load current in a small WLCSP package. The device adopts the constant on-time (COT) architecture to provide superior load transient performance. In addition, the advanced control architecture offers excellent load and line regulation performance.

The device operates in PWM mode with 2.3MHz of fixed switching frequency at medium to heavy load. At light load, the device automatically operates in power-save mode to provide excellent light load efficiency. The device only requires two 22μF ceramic output capacitors to achieve minimal output voltage ripple at light load and heavy load.

## Feature Description

### Power-Save Mode

As the load current decreases, the inductor current reaches around 0A in a switching cycle, and the operation mode becomes discontinuous. The SGM6037 automatically enters power-save mode (PSM) in discontinuous mode. Equation 1 below calculates the device on-time in PSM.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 416ns \quad (1)$$

In order to maintain regulation, the output voltage is slightly increased above the programmed voltage. Adding more output capacitors will minimize the output voltage rise in PSM.

### Forced PWM Mode (FPWM)

The SGM6037 is able to operate in FPWM mode to achieve fixed switching frequency and output ripple across the entire operating load range. FPWM is configurable in CONTROL register (**REG0x03**) via I²C.

### Start-up

When the input voltage is above the UVLO rising threshold of 2.2V (TYP), toggling the enable pin to logic high to start up the device. Before the output voltage starts ramping up, the device has an enable delay of 640μs (TYP). During the enable delay, the device establishes the internal reference, and reads the resistor connected to the VSET/VID or VSET/nPG pin to determine the start-up output voltage. The internal registers can be programmed via I²C after the enable delay.

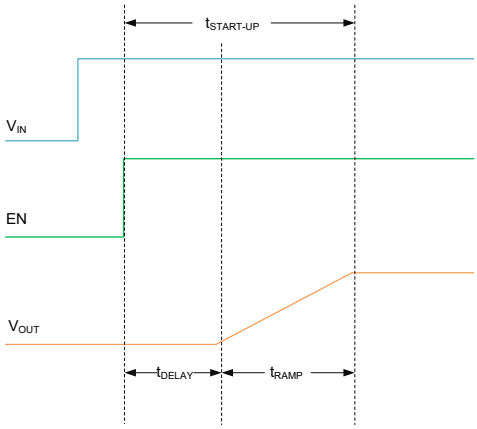



**Figure 3. Start-up Sequence**

The device initiates an internal soft-start when the enable delay finishes. The internal soft-start time is fixed to 1ms to ramp up the output voltage from 0V to the programmed output voltage. The soft-start mechanism effectively reduces the inrush current drawn from the input source, as well as providing a controlled output voltage rising ramp. For pre-biased output voltage start-up, the device starts up from the pre-biased voltage to the programmed output voltage.

### Switch Current Limit and Hiccup Short-Circuit Protection

The device implements over-current protection when the load exceeds the maximum allowed 6A to prevent excessive current drawn from battery type inputs. During an output short scenario or a saturated inductor, the inductor current will reach the current limit threshold. When current limit threshold is reached, the device turns off the high-side switch to terminate the inductor current from further increase, and the low-side switch turns on to ramp down the inductor current to the low-side switch current limit.

During the short-circuit event, as the output voltage drops below 0.3V, the current limit threshold is foldback to 4A for 6A version to prevent the device from excessive temperature rise. When the high-side switch current limit and low-side current limit are triggered for 64 consecutive times, the switching is terminated immediately to enter hiccup short protection mode of 128μs hiccup off-time. The device resumes operation after hiccup off-time with the soft-start sequence. If the over-current or short condition remains, the device remains in the hiccup cycle until the fault condition is removed.

## DETAILED DESCRIPTION (continued)

**Under-Voltage Lockout (UVLO)**

The SGM6037 offers input under-voltage lockout to prevent false triggering with unstable input source. The device's UVLO rising voltage is 2.2V (TYP) and falling threshold is 2.1V (TYP). The device stops operation as soon as the input voltage drops below the falling threshold. The output voltage discharge is active when UVLO falling threshold is reached, and the output voltage discharge function is programmable via the CONTROL register. The internal register settings are not cleared when UVLO is triggered.

When the input voltage drops below the falling threshold, the UVLO bit in the STATUS register is set, and all register settings will reset until the input voltage drops below 1.8V (TYP).

**Thermal Warning and Shutdown**

The SGM6037 is a high power density device, thus when the junction temperature rises above the $T_{JW}$, a thermal pre-warning indicator in the STATUS register will toggle high to alert the host, however the device will continue operating.

As the junction temperature continues to rise and exceeds above the $T_{SD}$, the device stops switching, enabling active discharge to discharge the output voltage and enters thermal shutdown. The device has a 20℃ (TYP) thermal shutdown hysteresis to allow the device to resume operation automatically with internal soft-start. The register settings are not changed during thermal shutdown.

## Device Functional Modes

**Enable and Disable (EN)**

$I^2C$ interface is live when the EN pin is toggled logic high after the enable delay time. When the EN pin is toggled to logic low, power FETs are off as well as the internal control circuits. Register settings are reset except the EN_OUTPUT_DISCHG bit. EN pin cannot be left floating.

Device enters shutdown mode when EN pin is logic low. $I^2C$ communication is terminated in this mode.

The EN pin supports 1.2V I/O logic with 0.66V rising threshold and 0.58V falling threshold.

The device also supports a software enable and disable via EN_DEVICE bit in CONTROL register while EN pin is toggled to logic high. When the device is enabled by this bit, the device starts up with $t_{RAMP}$, and no $t_{DELAY}$ is required. When the device is disabled by this bit, the device stops switching, but $I^2C$ communication remains active.

**Output Discharge**

The device implements $I^2C$ programmable output voltage discharge function for application requiring sequencing control. The internal discharge path discharges the output voltage through the SW pin to ground. There are four scenarios to discharge the output voltage: EN pin is toggled to logic low, EN_DEVICE bit is set to 0, input voltage UVLO or device thermal shutdown.

Output voltage discharge function is disabled when the EN_OUTPUT_DISCHG bit is set to 0. The output discharge function remains active as long as the input voltage is higher than 1V (TYP) and the EN_OUTPUT_DISCHG bit is retained. When a rising edge of the EN pin is applied, the EN_OUTPUT_DISCHG bit is reset.

**Start-up Output Voltage and $I^2C$ Slave Address Selection (VSET)**

In start-up phase, during the enable delay period, the resistor is connected to VSET/VID or VSET/nPG pin to program the output voltage as well as device slave address through an internal R2D (resistor to digital) converter. Table 1 lists the programmable options.

During the enable delay time, a current source is applied on the VSET resistor. The internal ADC converts the voltage on the VSET pin to a digital signal to program the output voltage and $I^2C$ slave address. Once this R2D conversion completes, the current source is turned off to avoid unnecessary current consumption. Any capacitance higher than 30pF is not recommended to connect between the VSET pin to ground.

If $I^2C$ command is issued to change the output voltage, the device will ramp up to the VSET resistor programmed output voltage first before ramping up/down to the $I^2C$ programmed output voltage.

## DETAILED DESCRIPTION (continued)

**Table 1. Start-up Output Voltage and I²C Slave Address Options**

| START-UP OUTPUT VOLTAGE (TYP) | RESISTOR (E96 SERIES, ±1% ACCURACY) AT VSET/VID OR VSET/nPG PIN | I²C SLAVE ADDRESS |
|---|---|---|
| 1.15V | 249kΩ | 1000 110 |
| 1.10V | 205kΩ | 1000 101 |
| 1.05V | 162kΩ | 1000 100 |
| 1.00V | 133kΩ | 1000 011 |
| 0.95V | 105kΩ | 1000 010 |
| 0.90V | 86.6kΩ | 1000 001 |
| 0.85V | 68.1kΩ | 1001 000 |
| 0.80V | 56.2kΩ | 1001 001 |
| 0.75V | 44.2kΩ | 1001 010 |
| 0.70V | 36.5kΩ | 1001 011 |
| 0.65V | 28.7kΩ | 1001 100 |
| 0.60V | 23.7kΩ | 1001 101 |
| 0.55V | 18.7kΩ | 1001 110 |
| 0.50V | 15.4kΩ | 1001 111 |
| 0.45V | 12.1kΩ | 1000 000 |
| 0.40V | 10kΩ | 1000 111 |

### VID

The device offers 2 selectable output voltage registers via the VID pin, and dynamic voltage scaling (DVS) is supported via these 2 registers. VID pin is pulled to logic low, the output voltage follows **REG0x01**, and VID pin is pulled to logic high, the output voltage follows **REG0x02**.

Output voltage adjustment can be made via either I²C programming or toggling the VID pin, and the output voltage ramp up and down speed is also configurable via the RAMP_SPEED bits.

### Active-Low Power Good

The SGM6037 offers variants for an active-low power good option if VID function is not used. The device starts to compare the actual output voltage with the VSET resistor programmed output voltage after the enable delay time. When the voltage reaches 91% (TYP) of programmed output voltage, after 200μs delay, the VSET/nPG is pulled low. The VSET/nPG pin remains low as long as the output voltage is within 91% to 111% of the programmed output voltage.

For the VSET/nPG version, a resistor must be connected from this pin to ground to properly configure the start-up voltage and I²C slave address. VOUT Register 2 is disabled and this pin's source current is up to 1mA. Due to the active-low logic configuration, in device shutdown, leakage current is increased through the resistor connected to this pin, since the VSET/nPG pin is pulled high.

**Table 2. VSET/nPG Pin Logic**

| DEVICE CONDITIONS | | nPG LOGIC STATUS |
|---|---|---|
| Enable | $0.91 \times V_{OUT_NOM} \le V_{VOS} \le 1.11 \times V_{OUT_NOM}$ | Low |
| | $V_{VOS} < 0.91 \times V_{OUT_NOM}$ or $V_{VOS} > 1.11 \times V_{OUT_NOM}$ | High |
| Shutdown | EN = Low | High |
| Thermal Shutdown | $T_J > T_{SD}$ | High |
| UVLO | $1.8V < V_{IN} < V_{UVLO}$ | High |
| Power Supply Removal | $V_{IN} < 1.8V$ | Undefined |

# DETAILED DESCRIPTION (continued)

## I²C Interface

### I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM6037 parameters and get status reports. I²C is the well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM6037 operates as a slave device that provides 16 address options as shown in Table 1.

The interface of SGM6037 supports four communication modes defined in the I²C specification: standard mode (100kbps), fast mode (400kbps), fast mode plus (1Mbps) and high-speed mode (3.4Mbps). The data transfer protocols for the standard mode, fast mode and fast mode plus are the same, while the protocol for high-speed is different.

## I²C Data Communication for Standard Mode, Fast Mode and Fast Mode Plus

### START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

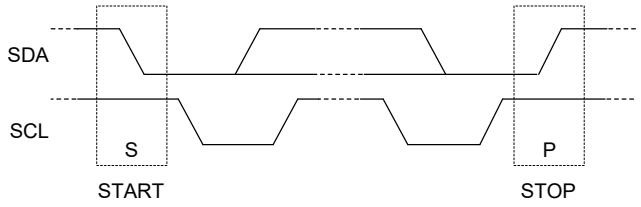



**Figure 4. I²C Bus in START and STOP Conditions**

### Data Bit Transmission and Validity

The data bit (high or low) must remain stable during clock high period. The state of SDA can only change when SCL is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 5.

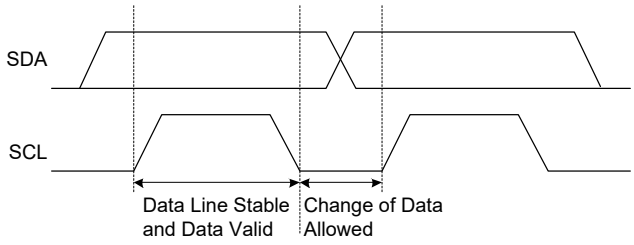



**Figure 5. I²C Bus Bit Transfer**

### Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 6 shows the byte transfer process with I²C interface.

## DETAILED DESCRIPTION (continued)

### Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

### Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 7.

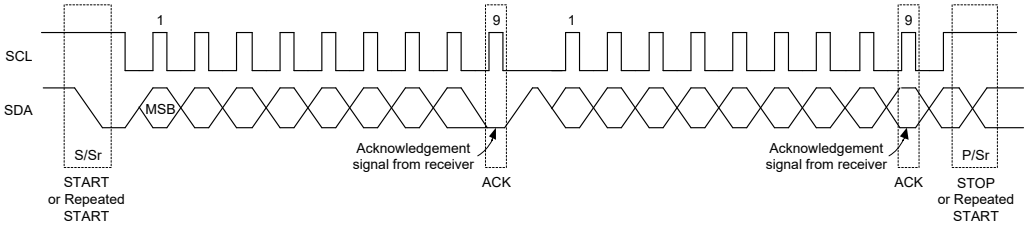



**Figure 6. Byte Transfer Process**

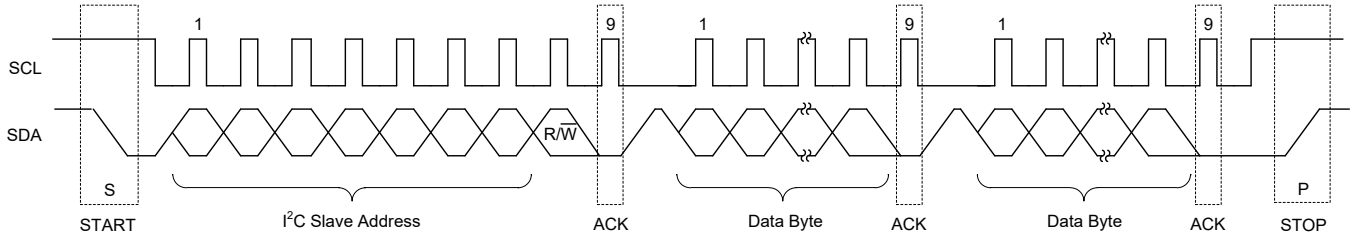



**Figure 7. Data Transfer Transaction in Standard Mode, Fast Mode and Fast Mode Plus**

## DETAILED DESCRIPTION (continued)

**WRITE:** If the master wants to write in the register, the third byte can be written directly as shown in Figure 8 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

**READ:** If the master wants to read a single register (Figure 9), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

### High-Speed (HS) Mode

The protocol for high-speed mode is different from standard mode, fast mode and fast mode plus. The high-speed mode is entered after the master sends the HS master code 00001XXX after a start condition. The HS master code is sent at standard mode, fast mode and fast mode plus with rate less than 1Mbps. The slave device is not allowed to acknowledge the HS master code, while they need to recognize and shift the interface to HS mode. Then, the master sends a repeated start condition. After that, the transaction in HS mode begins where the protocol is the same as standard mode, fast mode and fast mode plus except that the transmission rate is increased to 3.4 Mbps. The master sends a stop condition to stop the HS mode. Instead, repeated start condition is necessary to maintain transmission in HS mode.

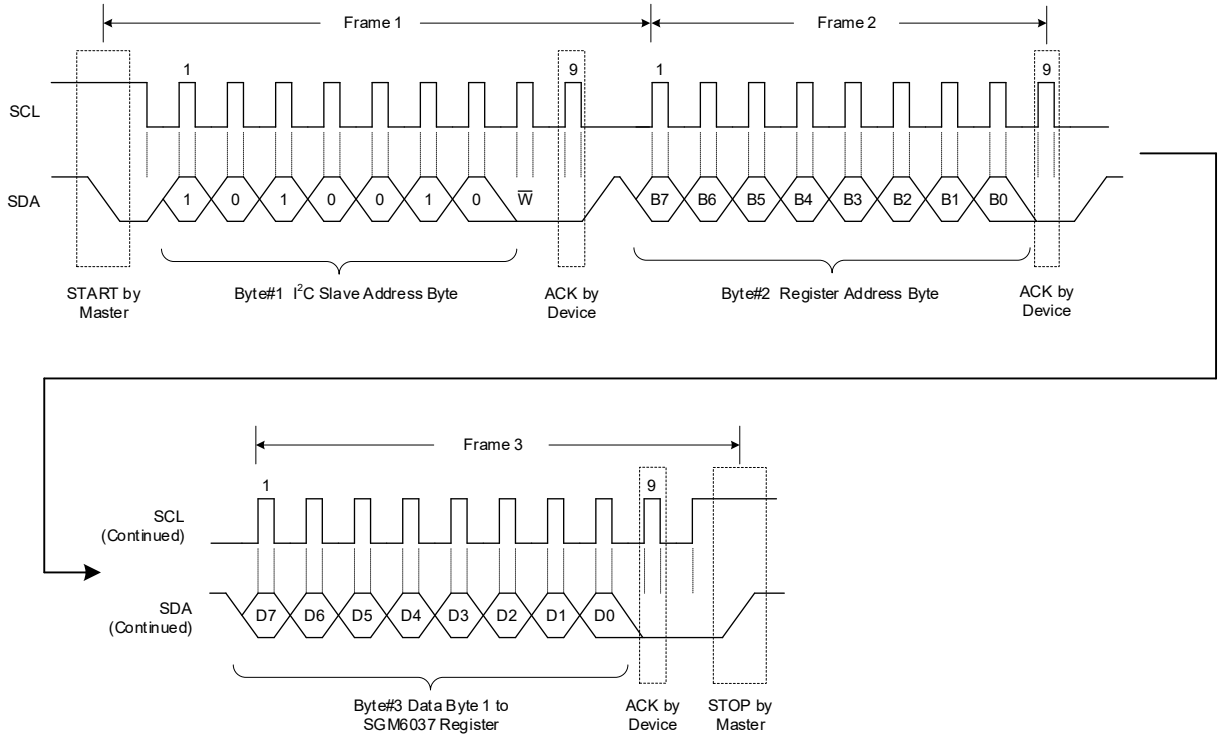



**Figure 8. A Single Write Transaction in Standard Mode, Fast Mode and Fast Mode Plus**

## DETAILED DESCRIPTION (continued)

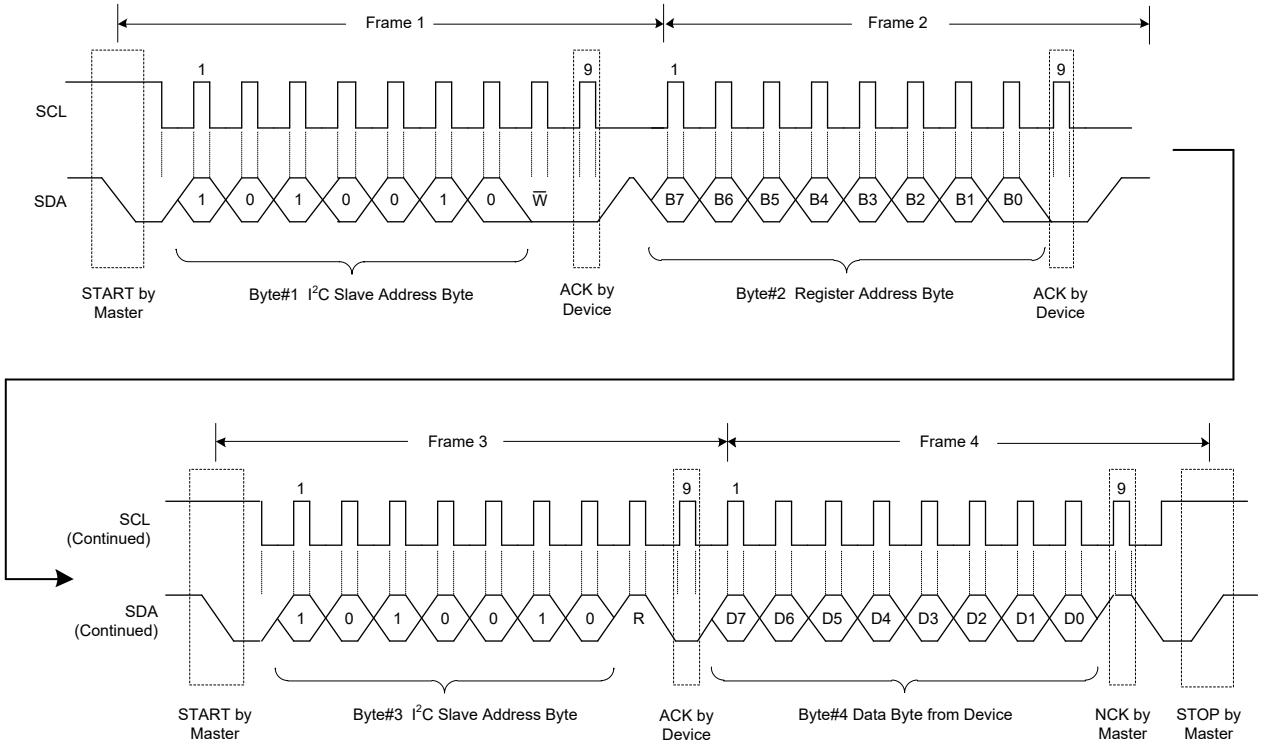



**Figure 9. A Single Read Transaction in Standard Mode, Fast Mode and Fast Mode Plus**

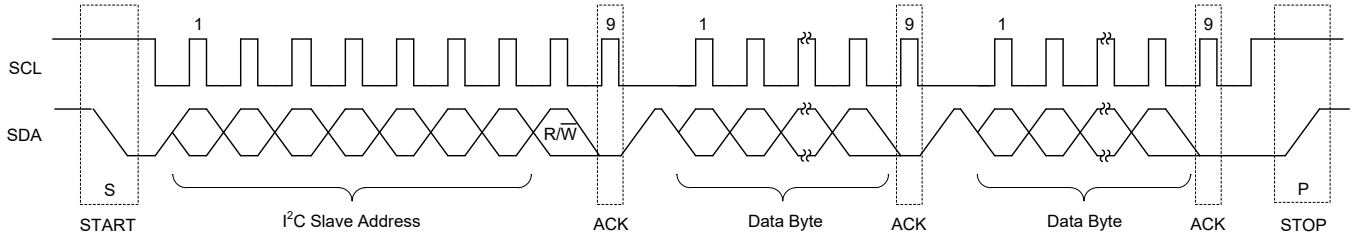



**Figure 10. Data Transfer Transaction in High-Speed Mode**

# REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

## I²C Address Map of SGM6037

| ADDRESS | REGISTER NAME | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|---|---|---|---|---|---|---|---|---|---|
| 0x01 | VOUT Register 1 | VO1_SET[7:0] | | | | | | | |
| 0x02 | VOUT Register 2 | VO2_SET[7:0] | | | | | | | |
| 0x03 | CONTROL Register | RESET | EN_FPWM_CHANGE | EN_DEVICE | EN_FPWM | EN_OUTPUT_DISCHG | EN_HICCUP | RAMP_SPEED | |
| 0x05 | STATUS Register | Reserved | | | T_WARN | HICCUP | Reserved | Reserved | UVLO |

Bit Types:
R: Read only
R/W: Read/Write

### REG0x01: VOUT Register 1

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:0] | VO1_SET[7:0] | - | R/W | Output Voltage<br>0x00 = 400mV<br>0x01 = 405mV<br>…<br>0x64 = 900mV<br>…<br>0xFE = 1670mV<br>0xFF = 1675mV |

### REG0x02: VOUT Register 2 [Reset = 0x64]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:0] | VO2_SET[7:0] | 0110 0100 | R/W | Output Voltage<br>0x00 = 400mV<br>0x01 = 405mV<br>…<br>0x64 = 900mV (default)<br>…<br>0xFE = 1670mV<br>0xFF = 1675mV |

## REGISTER MAPS (continued)

### REG0x03: CONTROL Register [Reset = 0x6F]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7] | RESET | 0 | R/W | 1 = Reset all registers to default. |
| D[6] | EN_FPWM_CHANGE | 1 | R/W | Enable FPWM mode during output voltage change.<br>0 = Keep the current mode status during output voltage change.<br>1 = Force the device in FPWM during output voltage change. (default) |
| D[5] | EN_DEVICE | 1 | R/W | Software Enable Device<br>0 = Disable the device. All registers values are still kept.<br>1 = Re-enable the device with a new start-up without the $t_{DELAY}$ period. (default) |
| D[4] | EN_FPWM | 0 | R/W | Enable FPWM Mode<br>0 = Set the device in power save mode at light loads. (default)<br>1 = Set the device in forced PWM mode at light loads. |
| D[3] | EN_OUTPUT_DISCHG | 1 | R/W | Enable Output Discharge<br>0 = Disable output discharge.<br>1 = Enable output discharge. (default) |
| D[2] | EN_HICCUP | 1 | R/W | Enable HICCUP<br>0 = Disable HICCUP. Enable latching protection.<br>1 = Enable HICCUP. Disable latching protection. (default) |
| D[1:0] | RAMP_SPEED | 11 | R/W | Voltage Ramp Speed<br>00 = 20mV/μs (0.25μs/step)<br>01 = 10mV/μs (0.5μs/step)<br>10 = 5mV/μs (1μs/step)<br>11 = 1mV/μs (5μs/step, default) |

### REG0x05: STATUS Register [Reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION |
|---|---|---|---|---|
| D[7:5] | Reserved | - | - | Reserved. |
| D[4] | T_WARN | 0 | R | Thermal warning.<br>1 = Junction temperature is higher than +130℃. |
| D[3] | HICCUP | 0 | R | 1 = Device has HICCUP status once. |
| D[2] | Reserved | - | - | Reserved. |
| D[1] | Reserved | - | - | Reserved. |
| D[0] | UVLO | 0 | R | 1 = The input voltage is less than the UVLO falling threshold. |

# APPLICATION INFORMATION

## Typical Application

Figure 4 below shows a typical schematic for a 0.9V output application with a wide input voltage range.

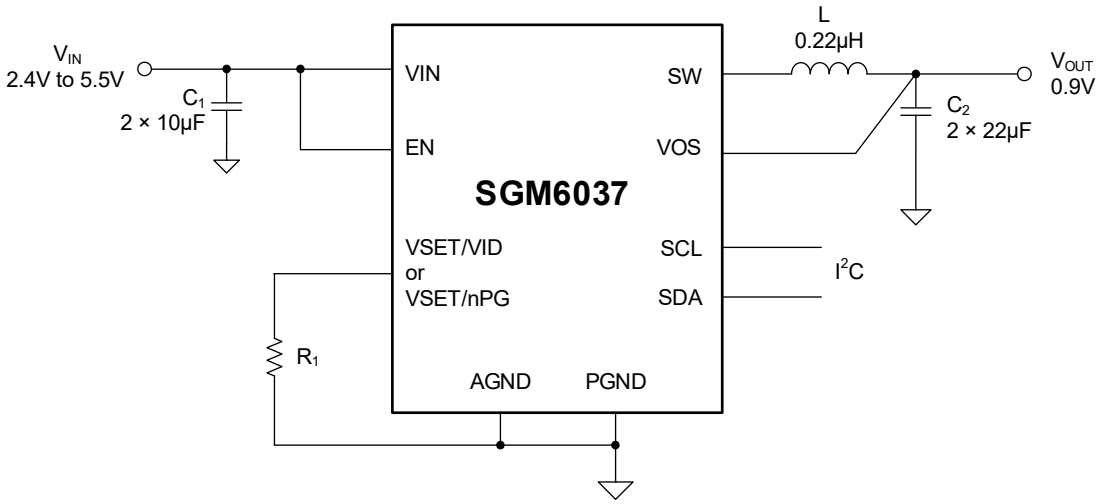



**Figure 11. 6A Output Current Typical Application**

## Design Requirements

Table 3 below shows the operation conditions of this design example.

**Table 3. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input Voltage | 2.4V to 5.5V |
| Output Voltage | 0.9V |
| Maximum Output Current | 6A |

Table 4 lists the components used for the example.

**Table 4. List of Components**

| REFERENCE | DESCRIPTION | MANUFACTURER |
|---|---|---|
| $C_1$ | 10μF, ceramic capacitor, 6.3V, X7R, size 0603, CL10B106MQ8NRNC | Samsung |
| $C_2$ | 22μF, ceramic capacitor, 6.3V, X7R, size 0805, GRM21BZ70J226ME44L | Murata |
| $L_1$ | 0.22μH, power inductor, XAL4020-221ME ($I_{RMS}$ = 12A, DCR = 5.81mΩ) | Coilcraft |
| $R_1$ | Depending on the start-up output voltage, size 0603 | Std |

# REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

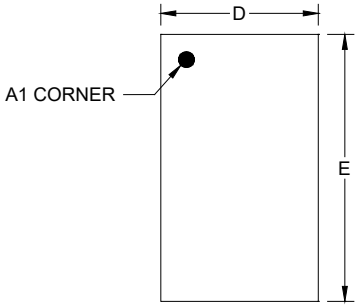
| JULY 2026 – REV.A.1 to REV.A.2 | Page |
|---|---|
| Updated Input Leakage Current, $t_{RAMP}$, $I_{LIM}$ values in ELECTRICAL CHARACTERISTICS | 5 |
| Updated Start-up and Shutdown by EN Pin in TYPICAL PERFORMANCE CHARACTERISTICS | 10 |

| JUNE 2026 – REV.A to REV.A.1 | Page |
|---|---|
| Added a note to $t_{HIGH}$ in I²C INTERFACE TIMING CHARACTERISTICS, and added I²C interface description | 6, 16 to 19 |
| Updated Efficiency vs. Output Current and Output Voltage vs. Output Current in TYPICAL PERFORMANCE | 8, 9 |
| Updated Table 2 and Table 4 | 15, 22 |

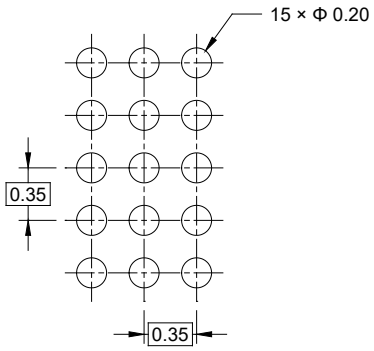
| Changes from Original to REV.A (DECEMBER 2024) | Page |
|---|---|
| Changed from product preview to production data | All |

# PACKAGE OUTLINE DIMENSIONS

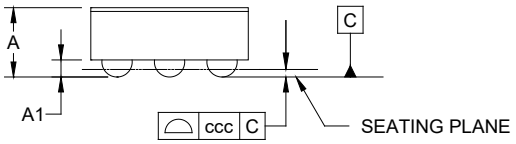
## WLCSP-1.05×1.78-15B



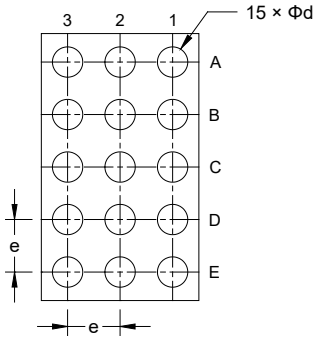

**TOP VIEW**




**RECOMMENDED LAND PATTERN** (Unit: mm)




**SIDE VIEW**



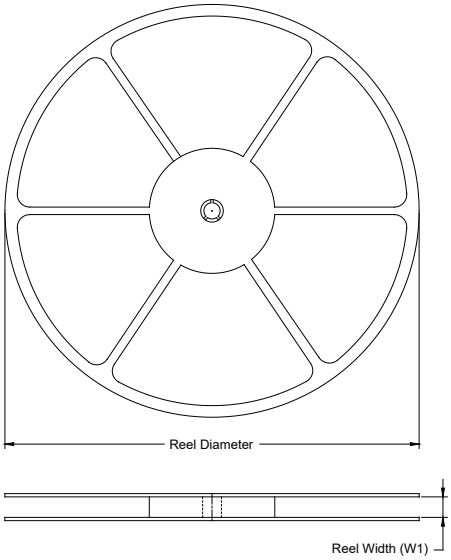

**BOTTOM VIEW**

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 0.500 |
| A1 | 0.094 | - | 0.134 |
| D | 1.020 | - | 1.080 |
| E | 1.750 | - | 1.810 |
| d | 0.172 | - | 0.232 |
| e | 0.350 BSC | | |
| ccc | 0.050 | | |

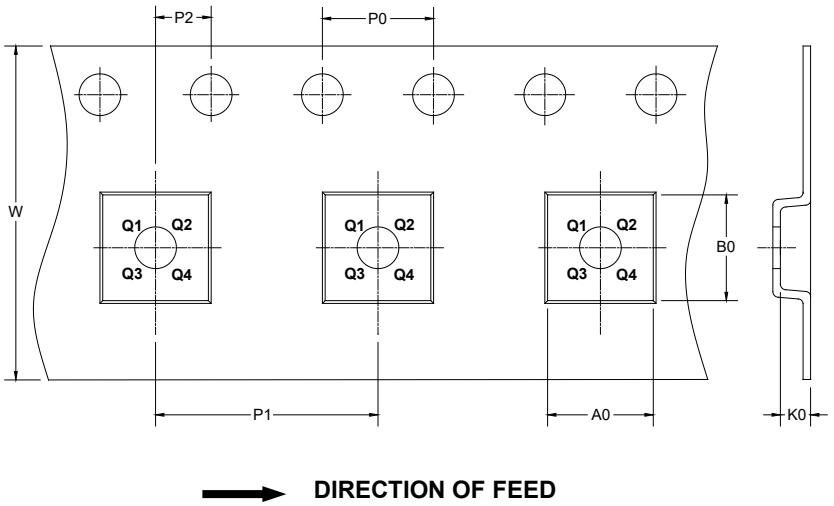
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



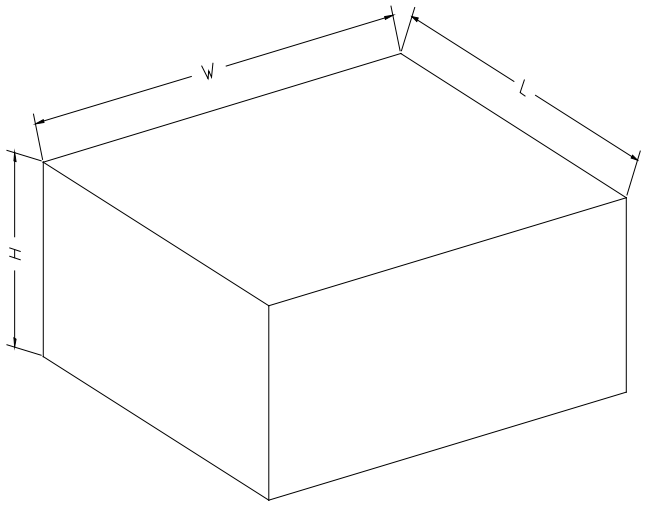

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP-1.05×1.78-15B | 7" | 9.0 | 1.16 | 1.88 | 0.65 | 4.0 | 4.0 | 2.0 | 8.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 7″ (Option) | 368 | 227 | 224 | 8 |
| 7″ | 442 | 410 | 224 | 18 |

DD0002