SGM58600A/SGM58601A/SGM58602A Ultra-Low Noise, 24-Bit Analog-to-Digital Converters

GENERAL DESCRIPTION

The SGM58600A, SGM58601A and SGM58602A are low noise, 24-bit, 60kSPS, sigma-delta (Σ-Δ) analog-to-digital converters (ADCs).

The SGM58600A, SGM58601A and SGM58602A have a fourth-order sigma-delta modulator plus a fifth-order Sinc filter ($Sinc^5$) optimized for low noise performance.

The flexible input multiplexer supports single-ended input or differential input configurations.

The SGM58600A, SGM58601A and SGM58602A feature a selectable input buffer that increases the input impedance, and the low noise programmable gain amplifier (PGA) provides gains from 1 to 128 in binary steps.

The devices have an SPI-compatible interface.

The devices have an internal on-chip oscillator. It is switched on by default after the system powers up. The internal oscillator can be switched off by software and configured as an external clock source.

The SGM58600A is available in Green SSOP-20 and TQFN-3.5×3.5-20L packages, the SGM58601A is available in Green SSOP-28 and TQFN-5×5-28L packages, and the SGM58602A is available in a Green TQFN-5×5-20L package. They are all specified from -40℃ to +125℃.

FEATURES

- **Supply Voltage Ranges:**
  - **Analog Supply: 5V**
  - **Digital Supply: 2.7V to 5V**
- **Noise-Free Resolution: Up to 22 Bits**
- **Data Output Rate: Up to 60kSPS**
- **Integral Nonlinearity (INL):**
  0.00045%FSR (TYP) at PGA[2:0] = 1
- **24-Bit No Missing Codes**
- **Fast Channel Cycling**
  - **18.4 Bits Noise-Free (21.2 Effective Bits) at 1.4kHz**
- **Flexible Input Multiplexer**
  - **2 Single-Ended Inputs or 1 Differential Inputs (SGM58600A)**
  - **8 Single-Ended Inputs or 4 Differential Inputs (SGM58601A)**
  - **3 Single-Ended Inputs or 2 Differential Inputs (SGM58602A)**
- **Low Noise Programmable Gain Amplifier:**
  30nV Input-Referred Noise
- **One-Shot Conversions with Single-Cycle Settling**
- **Chopper-Stabilized Input Buffer**
- **Support Self and System Calibration for All PGA Settings**
- **Support SPI-Compatible Serial Interface**

APPLICATIONS

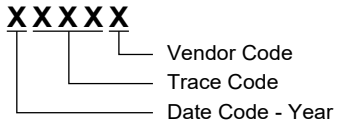
Lab Instrumentation
Measurement and Test
Industrial Process Control
Medical Instruments

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM58600A	SSOP-20	-40℃ to +125℃	SGM58600AXSS20G/TR	SGM58600A XSS20 XXXXX	Tape and Reel, 2000
			SGM58600AXSS20SG/TR	SGM58600A XSS20 XXXXX	Tape and Reel, 500
	TQFN-3.5×3.5-20L	-40℃ to +125℃	SGM58600AXTRL20G/TR	SGM0DE XTRL20 XXXXX	Tape and Reel, 5000
			SGM58600AXTRL20SG/TR	SGM0DE XTRL20 XXXXX	Tape and Reel, 500
SGM58601A	SSOP-28	-40℃ to +125℃	SGM58601AXSS28G/TR	SGM58601A XSS28 XXXXX	Tape and Reel, 2000
			SGM58601AXSS28SG/TR	SGM58601A XSS28 XXXXX	Tape and Reel, 500
	TQFN-5×5-28L	-40℃ to +125℃	SGM58601AXTQK28G/TR	SGM58601A XTQK28 XXXXX	Tape and Reel, 5000
			SGM58601AXTQK28SG/TR	SGM58601A XTQK28 XXXXX	Tape and Reel, 500
SGM58602A	TQFN-5×5-20L	-40℃ to +125℃	SGM58602AXTRM20G/TR	SGM58602A XTRM20 XXXXX	Tape and Reel, 5000
			SGM58602AXTRM20SG/TR	SGM58602A XTRM20 XXXXX	Tape and Reel, 500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND ..... -0.3V to 6V
DVDD to DGND ..... -0.3V to AVDD
AGND to DGND ..... -0.3V to 0.3V
Input Current (Continuous) 10mA
Analog Inputs to AGND ..... -0.3V to AVDD + 0.3V
Digital Inputs
DIN, SCLK, nCS, nRESET, nSYNC/nPDWN to DGND ..... -0.3V to 6V
D0/CLKOUT, D1, D2, D3, XTAL1/CLKIN, XTAL2 to DGND ..... -0.3V to DVDD + 0.3V
Package Thermal Resistance
SSOP-20, θ_{JA} ..... 67.4℃/W
SSOP-20, θ_{JB} ..... 36.2℃/W
SSOP-20, θ_{JC} ..... 28.8℃/W
TQFN-3.5×3.5-20L, θ_{JA} ..... 43.9℃/W
TQFN-3.5×3.5-20L, θ_{JB} ..... 13.6℃/W
TQFN-3.5×3.5-20L, $\theta_{JC\ (TOP)}$ ..... 32℃/W
TQFN-3.5×3.5-20L, $\theta_{JC\ (BOT)}$ ..... 1.8℃/W
SSOP-28, θ_{JA} ..... 60.2℃/W
SSOP-28, θ_{JB} ..... 34.4℃/W
SSOP-28, θ_{JC} ..... 28.2℃/W
TQFN-5×5-28L, θ_{JA} ..... 27.1℃/W
TQFN-5×5-28L, θ_{JB} ..... 8.8℃/W
TQFN-5×5-28L, $\theta_{JC\ (TOP)}$ ..... 19℃/W
TQFN-5×5-28L, $\theta_{JC\ (BOT)}$ ..... 1.7℃/W
TQFN-5×5-20L, θ_{JA} ..... 27.2℃/W
TQFN-5×5-20L, θ_{JB} ..... 8.5℃/W
TQFN-5×5-20L, $\theta_{JC\ (TOP)}$ ..... 19.9℃/W
TQFN-5×5-20L, $\theta_{JC\ (BOT)}$ ..... 1.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±8000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

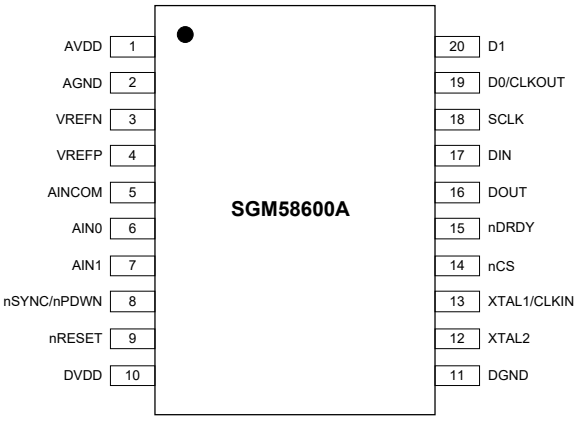
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

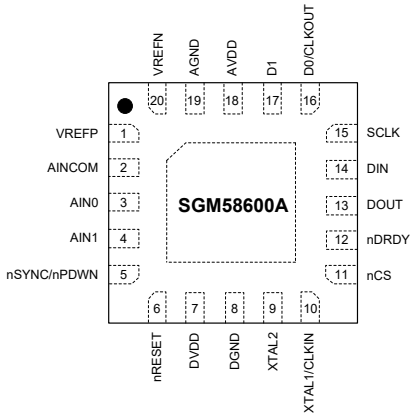
PIN CONFIGURATIONS

SGM58600A (TOP VIEW)



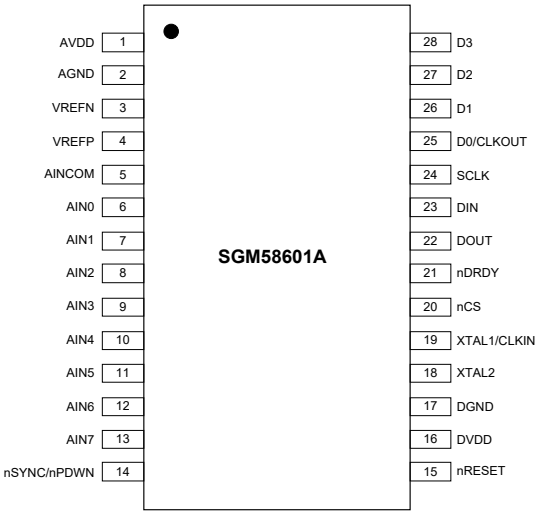
SSOP-20

SGM58600A (TOP VIEW)



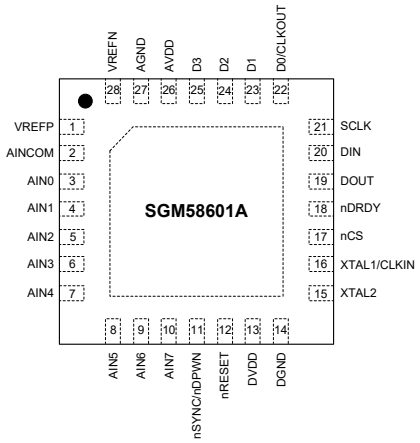
TQFN-3.5×3.5-20L

SGM58601A (TOP VIEW)



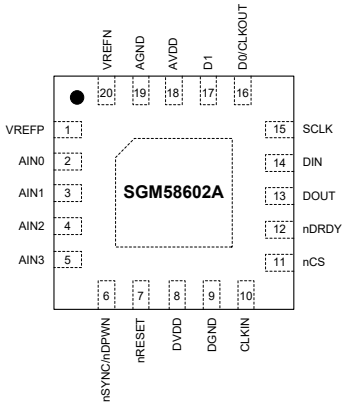
SSOP-28

SGM58601A (TOP VIEW)



TQFN-5×5-28L

SGM58602A (TOP VIEW)



TQFN-5×5-20L

PIN DESCRIPTION

PIN					NAME	TYPE (1)	FUNCTION
SGM58600A		SGM58601A		SGM58602A			
SSOP-20	TQFN-3.5×3.5-20L	SSOP-28	TQFN-5×5-28L	TQFN-5×5-20L			
1	18	1	26	18	AVDD	A	Analog Power Supply.
2	19	2	27	19	AGND	A	Analog Ground.
3	20	3	28	20	VREFN	AI	Negative Reference Input.
4	1	4	1	1	VREFP	AI	Positive Reference Input.
5	2	5	2	–	AINCOM	AI	Analog Input Common.
6	3	6	3	2	AIN0	AI	Analog Input 0.
7	4	7	4	3	AIN1	AI	Analog Input 1.
–	–	8	5	4	AIN2	AI	Analog Input 2.
–	–	9	6	5	AIN3	AI	Analog Input 3.
–	–	10	7	–	AIN4	AI	Analog Input 4.
–	–	11	8	–	AIN5	AI	Analog Input 5.
–	–	12	9	–	AIN6	AI	Analog Input 6.
–	–	13	10	–	AIN7	AI	Analog Input 7.
8	5	14	11	6	nSYNC/nPDWN	DI (2)	Synchronization Input/Power-Down Input. Active low.
9	6	15	12	7	nRESET	DI (2)	Reset Input. Active low.
10	7	16	13	8	DVDD	D	Digital Power Supply.
11	8	17	14	9	DGND	D	Digital Ground.
12	9	18	15	–	XTAL2	D (3)	Crystal Oscillator Connection.
13	10	19	16	–	XTAL1/CLKIN	D/DI	Crystal Oscillator Connection/Clock Input.
–	–	–	–	10	CLKIN	D/DI	Clock Input.
14	11	20	17	11	nCS	DI (2)	Chip Select. Active low.
15	12	21	18	12	nDRDY	DO	Data Ready Output. Active low.
16	13	22	19	13	DOUT	DO	Serial Data Output.
17	14	23	20	14	DIN	DI (2)	Serial Data Input.
18	15	24	21	15	SCLK	DI (2)	Serial Clock Input.
19	16	25	22	16	D0/CLKOUT	DIO (4)	Digital Input/Output 0/Clock Output.
20	17	26	23	17	D1	DIO (4)	Digital Input/Output 1.
–	–	27	24	–	D2	DIO (4)	Digital Input/Output 2.
–	–	28	25	–	D3	DIO (4)	Digital Input/Output 3.
–	Exposed Pad	–	Exposed Pad	Exposed Pad	AGND	–	Exposed pad should be soldered to PCB board and connected to AGND.

NOTES:

1. A = analog, AI = analog input, D = digital, DI = digital input, DO = digital output, DIO = digital input and output.

2. Schmitt-trigger logic input.

3. If the external clock input is applied to XTAL1/CLKIN, stay disconnected.

4. It is the Schmitt-trigger logic input when the pin is used as an input.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = 5V, V_{DVDD} = 3.3V, V_{REF} = 2.5V, T_A = -40℃ to +125℃, f_{CLK} = 7.68MHz (internal), PGA[2:0] = 1, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Inputs							
Full-Scale Input Voltage (AIN_P - AIN_N)					±2V_{REF}/PGA		V
Absolute Input Voltage (AIN0 - AIN7, AINCOM to AGND)		Buffer off		AGND - 0.1		AVDD + 0.1	V
		Buffer on		AGND		AVDD	
Programmable Gain Amplifier				1		128	
Differential Input Impedance		Buffer off	PGA[2:0] = 1		130		kΩ
			PGA[2:0] = 2 or 4		68		
			PGA[2:0] = 8		260		
			PGA[2:0] = 16, 32, 64 or 128		190		
		Buffer on			6		MΩ
Sensor Detection Current Sources	I_{SDC}	SDCS[1:0] = 01			0.65		μA
		SDCS[1:0] = 10			2.45		
		SDCS[1:0] = 11			9.65		
System Performance							
Resolution				24			Bit
No Missing Codes		All data rates and PGA settings		24			Bit
Data Rate	f_{DATA}	f_{CLK} = 7.68MHz		2.5		60000	SPS (1)
Integral Nonlinearity	INL	Differential input, PGA[2:0] = 1			0.00045	0.0010	%FSR (2)
Offset Error		After self-calibration		On the level of the noise			
Offset Drift		PGA[2:0] = 1			200	600	nV/℃
		PGA[2:0] = 64			25	80	
Gain Error		After self-calibration, buffer on, T_A = +25℃	PGA[2:0] = 1		0.004	0.035	%
			PGA[2:0] = 64		0.06	0.13	
Gain Drift		PGA[2:0] = 1			0.55	1.5	ppm/℃
		PGA[2:0] = 64			1.2	2.5	
Common Mode Rejection Ratio	CMRR	f_{CM} (3) = 60Hz, f_{DATA} = 30kSPS (4)		100	110		dB
Noise				See Noise Performance Tables			
AVDD Power Supply Rejection		±5% Δ in AVDD		75	92		dB
DVDD Power Supply Rejection		±10% Δ in DVDD			100		dB
Voltage Reference Inputs							
Reference Input Voltage	V_{REF}	V_{REF} ≡ V_{REFP} - V_{REFN}		0.5	2.5	2.6	V
Negative Reference Input	V_{REFN}	Buffer off		AGND - 0.1		V_{REFP} - 0.5	V
		Buffer on		AGND		V_{REFP} - 0.5	
Positive Reference Input	V_{REFP}	Buffer off		V_{REFN} + 0.5		V_{AVDD} + 0.1	V
		Buffer on		V_{REFN} + 0.5		V_{AVDD}	

NOTES:

1. SPS = Samples per second.

2. FSR = Full-scale range = 4V_{REF}/PGA.

3. f_{CM} = Common mode input signal frequency.

4. Setting a digital filter notch at 60Hz (f_{DATA} = 60SPS, 30SPS, 15SPS, 10SPS, 5SPS, or 2.5SPS), this can improve the common mode rejection of this frequency.

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 5V, V_{DVDD} = 3.3V, V_{REF} = 2.5V, T_A = -40℃ to +125℃, f_{CLK} = 7.68MHz (internal), PGA[2:0] = 1, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Reference Inputs							
Voltage Reference Impedance	Z_{eff}	f_{CLK} = 7.68MHz (internal)	buffer off		45		kΩ
			buffer on		5.0		MΩ
Digital Input/Output							
Input High Voltage	V_{IH}			0.8 × V_{DVDD}		V_{DVDD}	V
Input Low Voltage	V_{IL}			DGND		0.2 × V_{DVDD}	V
Output High Voltage	V_{OH}	I_{OH} = 5mA		0.8 × V_{DVDD}			V
Output Low Voltage	V_{OL}	I_{OL} = 5mA				0.2 × V_{DVDD}	V
Input Hysteresis					0.5		V
Input Leakage		0 < $V_{DIGITAL\ INPUT}$ < DVDD				1	μA
Master Clock Rate		Internal oscillator		7.36	7.68	7.95	MHz
		External oscillator driving CLKIN, external crystal between XTAL1 and XTAL2			7.68		
Power Requirements							
AVDD Supply Voltage	V_{AVDD}			4.75		5.25	V
DVDD Supply Voltage	V_{DVDD}			2.7		AVDD	V
AVDD Current		Power-down mode, external crystal mode			0.47	5.00	μA
		Standby mode, external crystal mode			395	460	μA
		Normal mode, external crystal mode	PGA[2:0] = 1, buffer off		3.00	4.15	mA
			PGA[2:0] = 64, buffer off		5.10	7.40	
			PGA[2:0] = 1, buffer on		3.55	4.80	
			PGA[2:0] = 64, buffer on		5.50	7.90	
		Power-down mode, internal oscillator mode			0.45	5.00	μA
		Standby mode, internal oscillator mode			0.45	5.00	μA
		Normal mode, internal oscillator mode	PGA[2:0] = 1, buffer off		3.20	4.25	mA
			PGA[2:0] = 64, buffer off		5.25	7.50	
			PGA[2:0] = 1, buffer on		3.70	4.90	
			PGA[2:0] = 64, buffer on		5.60	8.00	
DVDD Current		Power-down mode, external crystal mode			0.14	2.00	μA
		Standby mode, external crystal mode, CLKOUT off, DVDD = 3.3V,	SGM58600A/SGM58601A		125	150	μA
			SGM58602A		95	120	
		Normal mode, external crystal mode, CLKOUT off, DVDD = 3.3V			0.60	1.00	mA
		Power-down mode, internal oscillator mode			0.14	2.00	μA
		Standby mode, internal oscillator mode, CLKOUT off, DVDD = 3.3V			0.14	2.00	μA
		Normal mode, internal oscillator mode, CLKOUT off, DVDD = 3.3V			0.52	1.00	mA
Power Dissipation		Normal mode, internal oscillator mode, PGA[2:0] = 1, buffer off, DVDD = 3.3V, CLKOUT off			18	25	mW
		Standby mode, internal oscillator mode, DVDD = 3.3V, CLKOUT off			3	32	μW

TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
SCLK Cycle Time	t_1		50		ns
SCLK High Time	t_{2H}		25		ns
SCLK Low Time	t_{2L}		25		ns
nCS Falling Edge to First SCLK Rising Edge Setup Time (1)	t_3		0		ns
Valid DIN to SCLK Falling Edge Setup Time	t_4		20		ns
Valid DIN to SCLK Falling Edge Hold Time	t_5		5		ns
Delay from Last SCLK Edge for DIN to First SCLK Rising Edge for DOUT: RDATA, RDATAC, RREG Commands	t_6		20		ns
SCLK Rising Edge to Valid New DOUT, Propagation Delay (2)	t_7			20	ns
SCLK Rising Edge to DOUT Invalid, Hold Time	t_8		0		ns
Last SCLK Falling Edge to DOUT High-Impedance (3)	t_9		20		ns
nCS Low after Final SCLK Falling Edge	t_{10}		0		ns
Final SCLK Falling Edge of Command to First SCLK Rising Edge of Next Command	t_{11}	RREG, WREG, RDATA	100		ns
		RDATAC, nSYNC	100		ns
		RDATAC, nRESET, STANDBY, SELFOCAL, SYSOCAL, SELFGCAL, SYSGCAL, SELFCAL	Wait for nDRDY to go low		
nRESET, nSYNC/nPDWN, Pulse Width	t_{12}	See Figure 2	0.5		μs
Conversion Data Invalid while Being Updated (nDRDY Shown with No Data Retrieval)	t_{13}	See Figure 3	30		τ_{CLKIN} (4)

NOTES:

1. nCS can be tied low.
2. DOUT load = 20pF and 100kΩ to DGND.
3. DOUT goes high-impedance immediately when nCS goes high.
4. Master clock period (f_{CLK} = 7.68MHz (internal)).

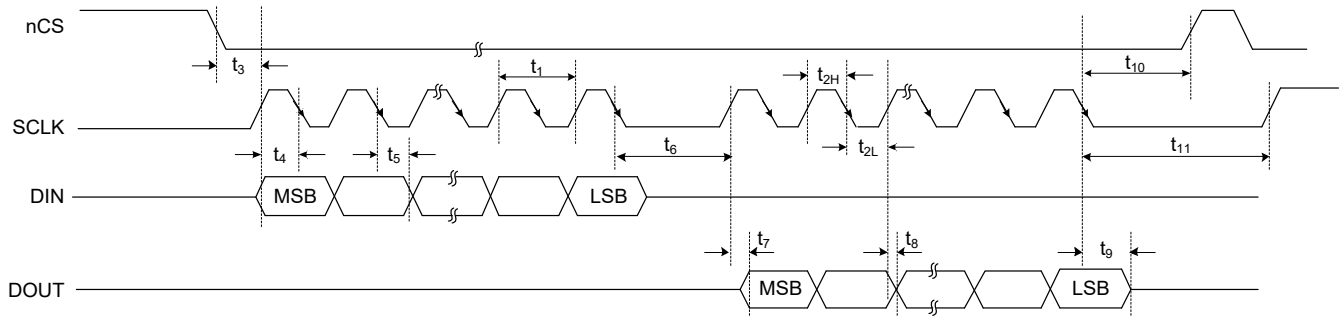


Figure 1. Serial Interface Timing Diagram

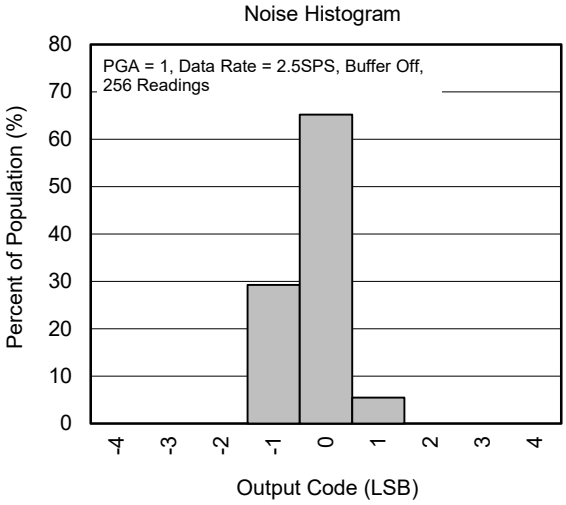


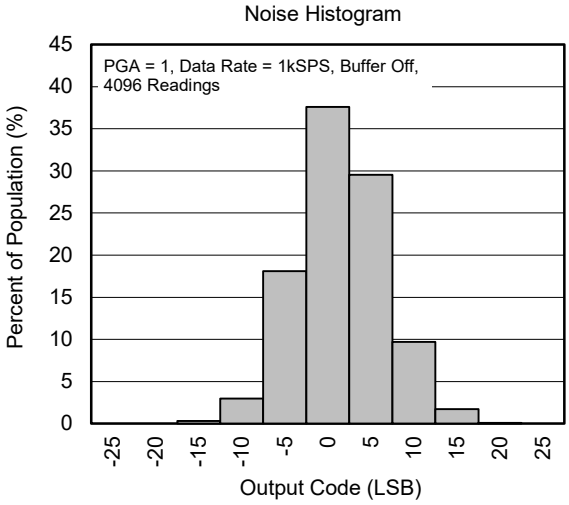
Figure 2. nRESET and nSYNC/nPDWN Timing Diagram

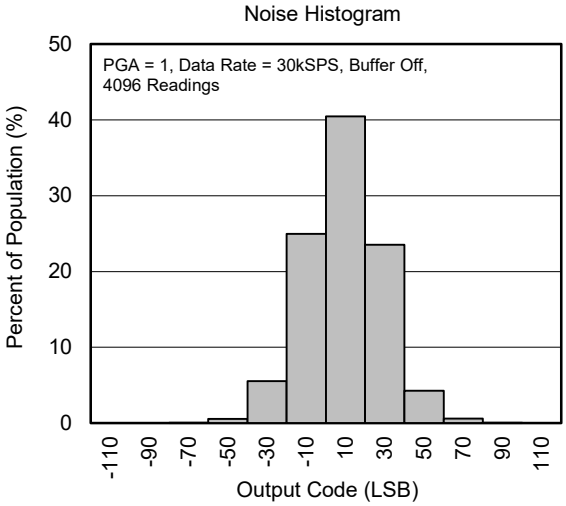


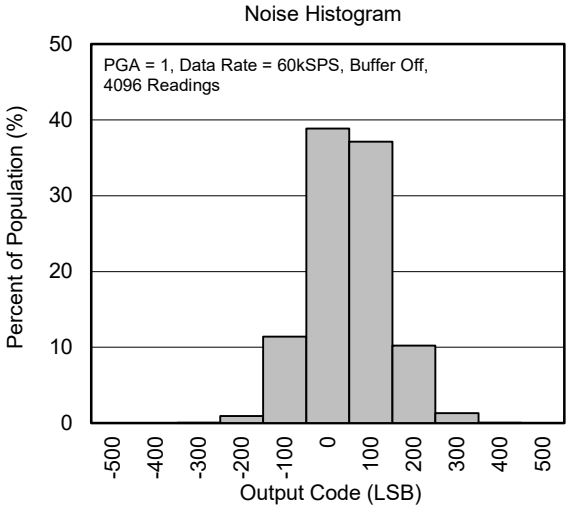
Figure 3. nDRDY Update Timing Diagram

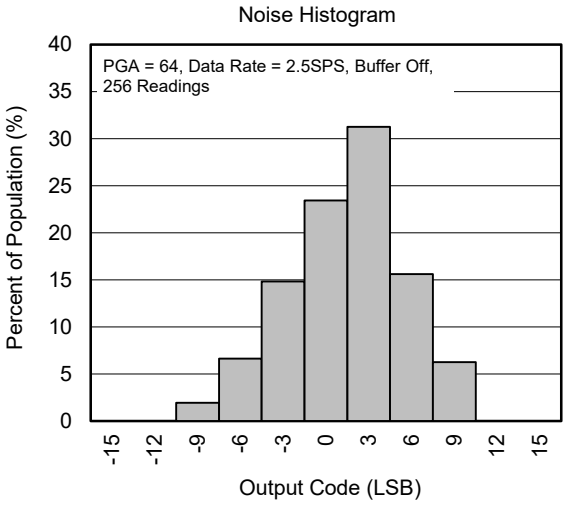
TYPICAL PERFORMANCE CHARACTERISTICS

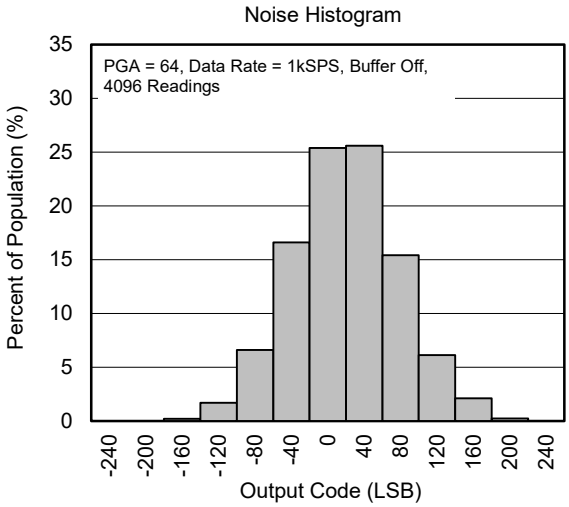




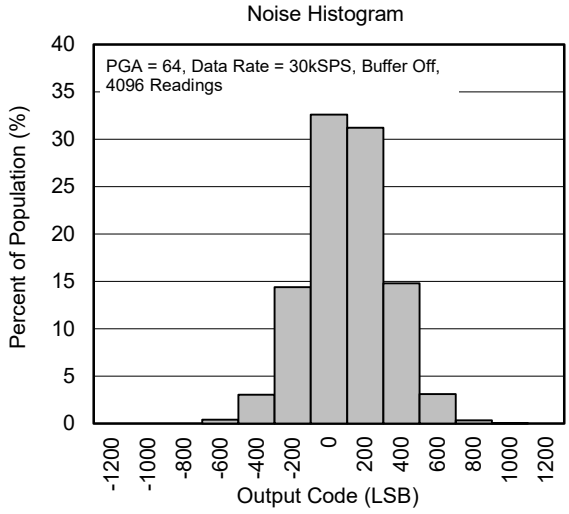


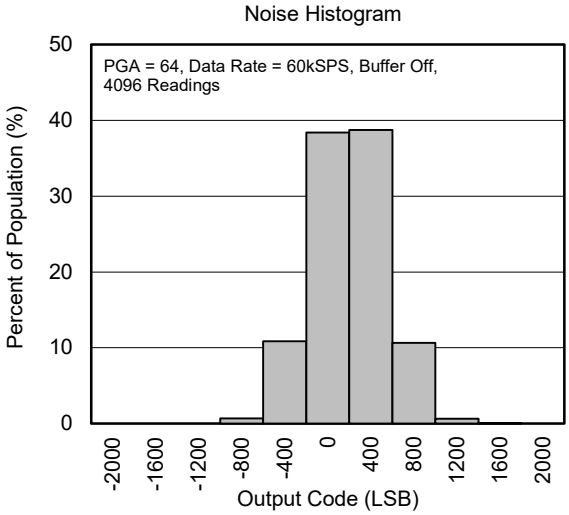


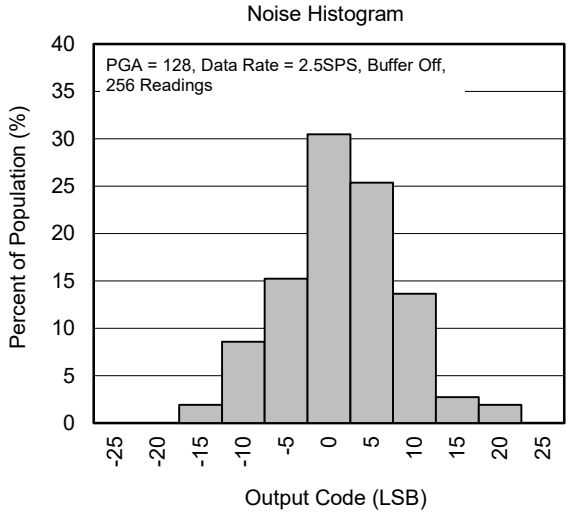


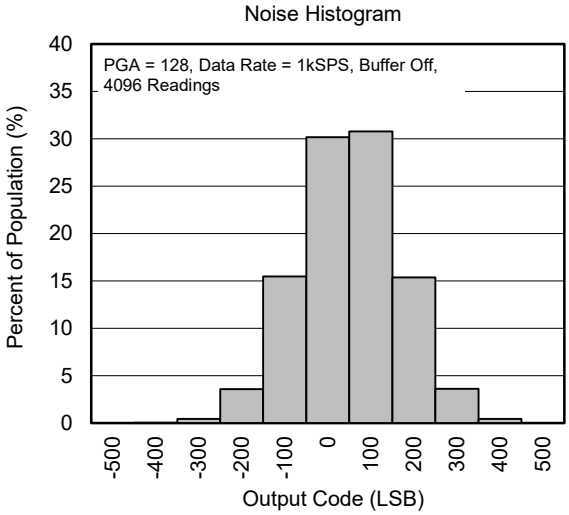


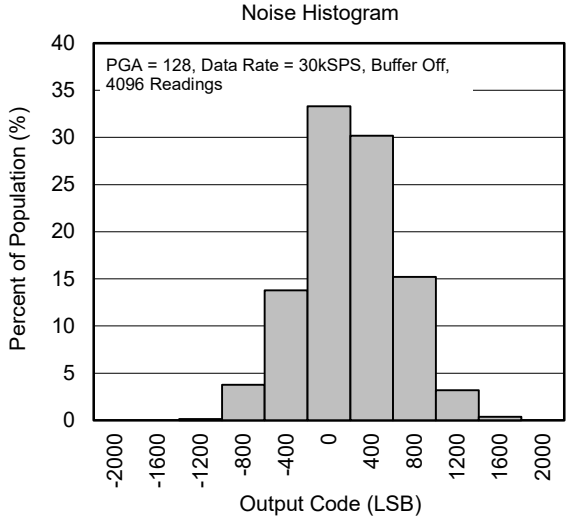
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

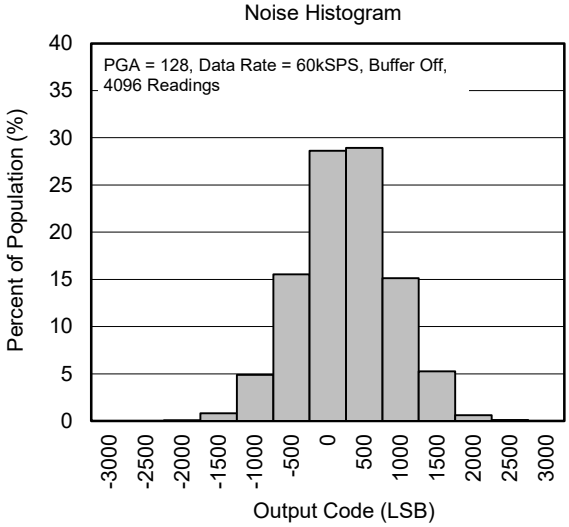




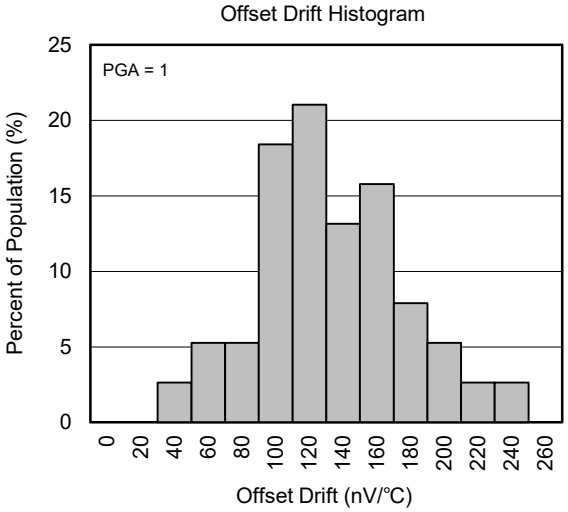


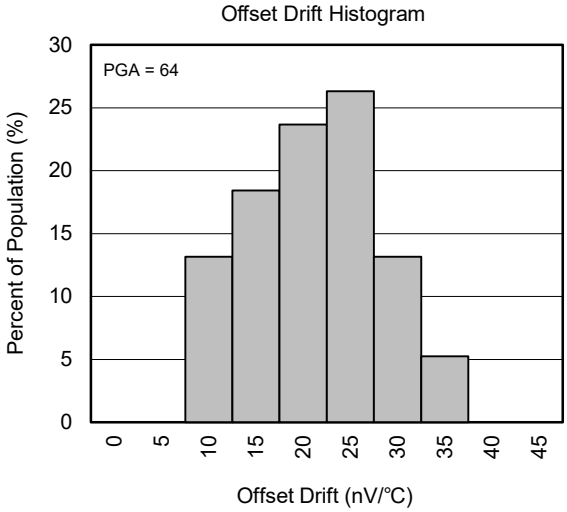


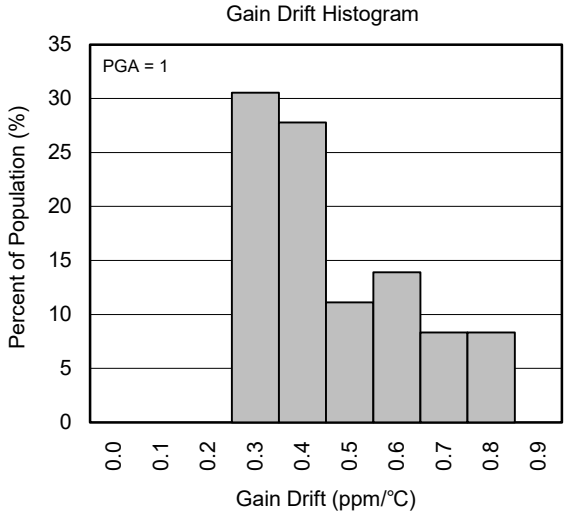


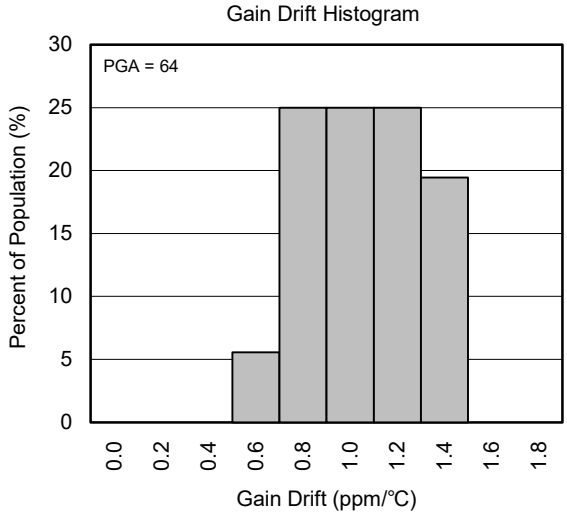


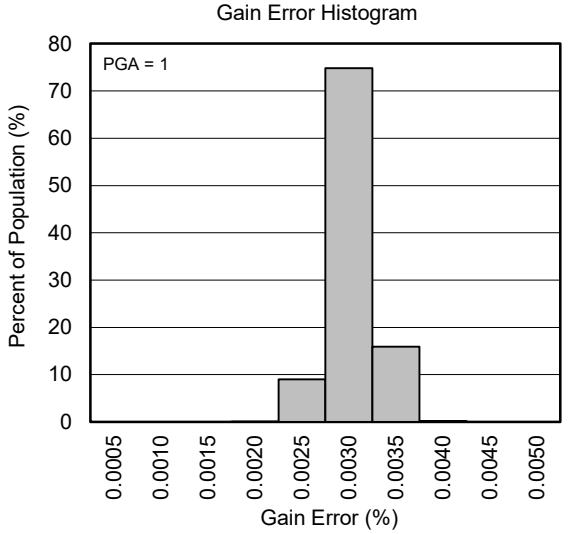
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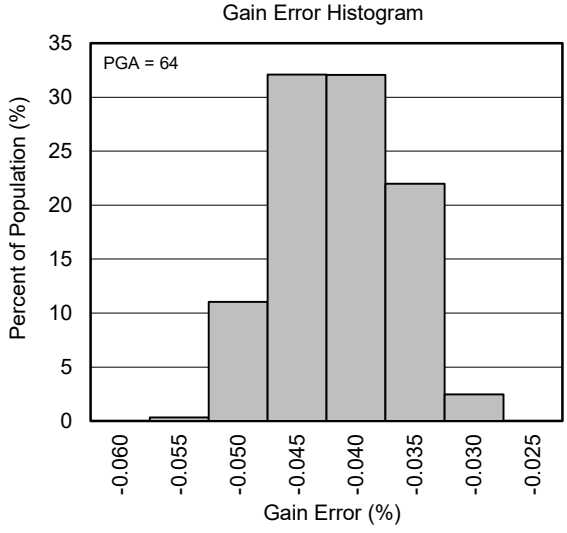






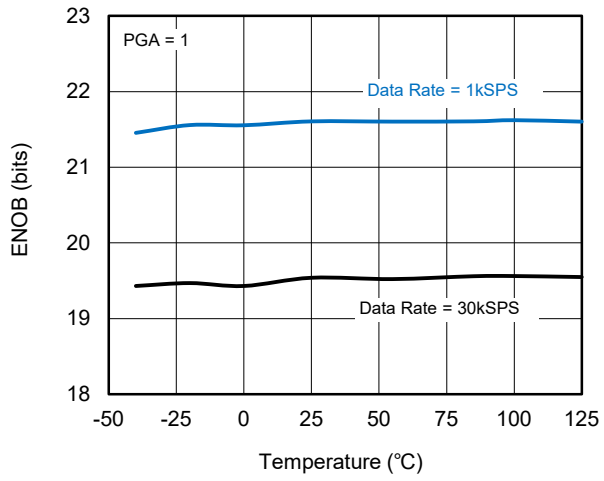




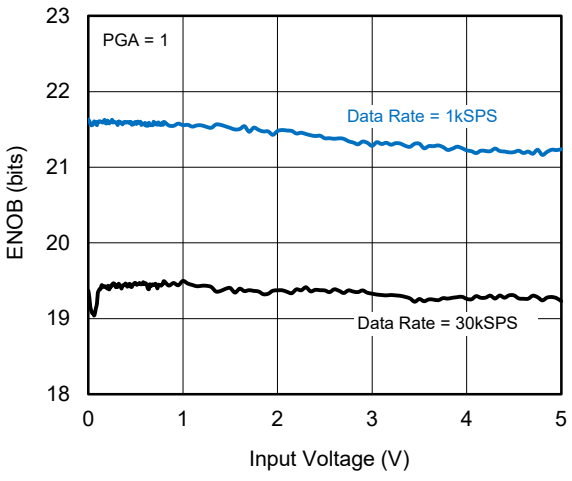


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

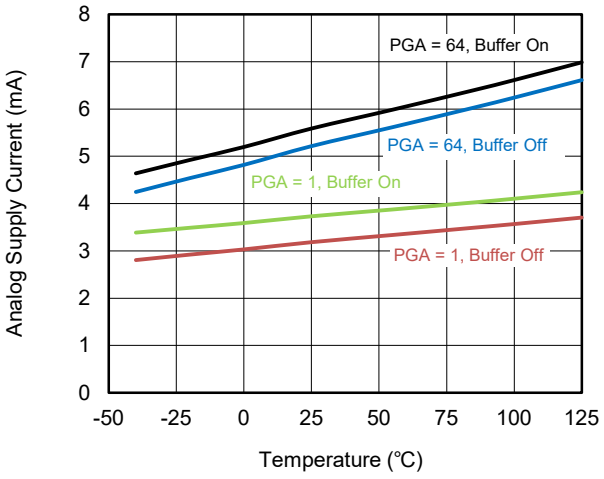
Effective Number of Bits vs. Temperature



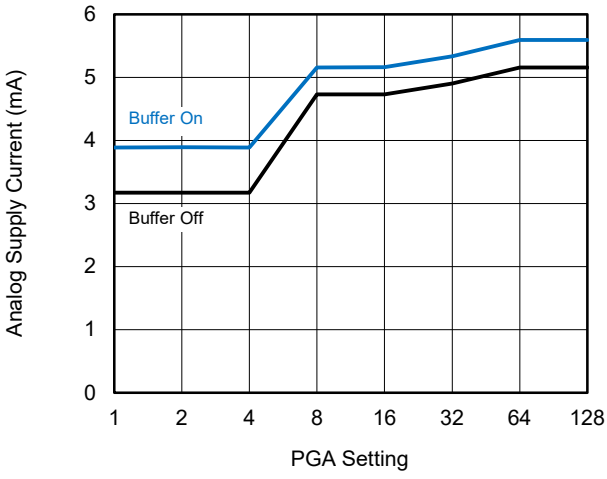
Effective Number of Bits vs. Input Voltage



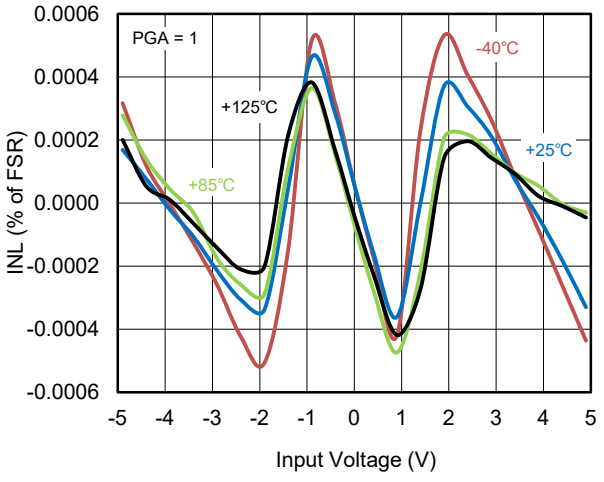
Analog Supply Current vs. Temperature



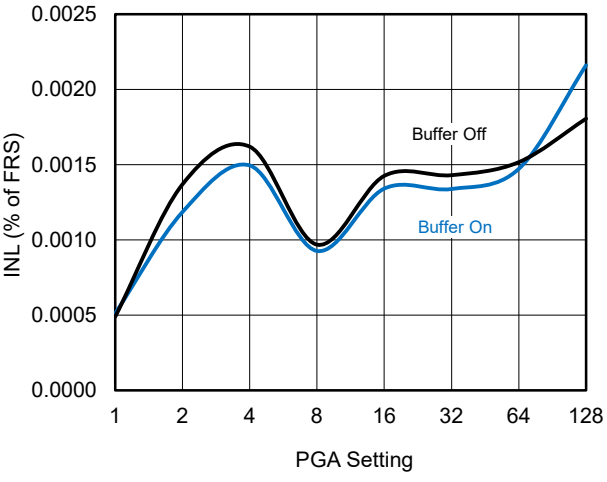
Analog Supply Current vs. PGA



Integral Nonlinearity vs. Input Voltage



Integral Nonlinearity vs. PGA



FUNCTIONAL BLOCK DIAGRAM

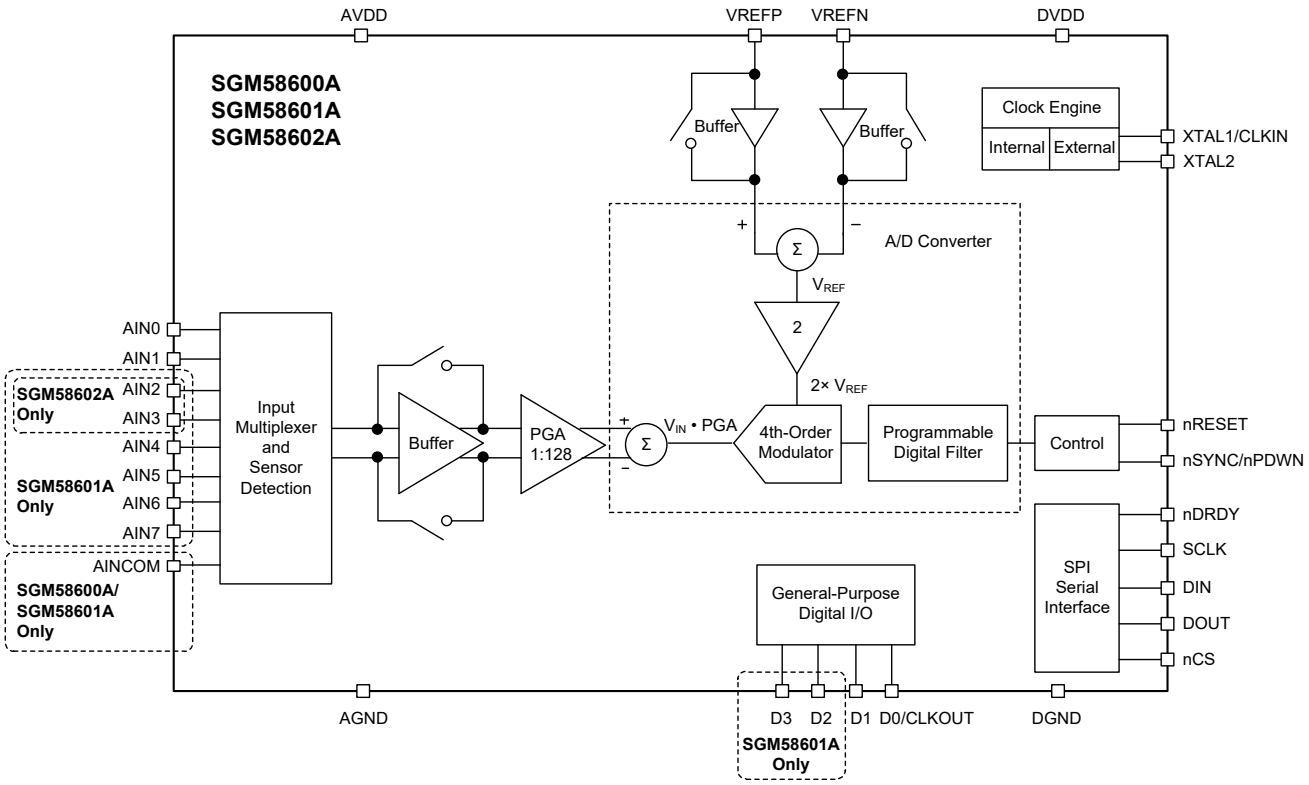


Figure 4. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM58600A, SGM58601A and SGM58602A are ultra-low noise analog-to-digital converters (ADCs). The block diagram of the SGM5860xA ADCs is shown in Figure 4.

The SGM58600A supports 1 differential input or 2 single-ended inputs and has 2 general-purpose digital I/Os. The SGM58601A supports 4 differential inputs or 8 single-ended inputs and has 4 general-purpose digital I/Os. The SGM58602A supports 2 differential inputs or 3 single-ended inputs and has 2 general-purpose digital I/Os.

These chips provide a configurable data rate from 2.5SPS to 60kSPS, the selection is a tradeoff between accuracy and speed.

Noise Performance

The typical noise performance with the inputs shorted externally is summarized from Table 1 to Table 6. For the six tables, the following conditions apply: T_A = +25℃, V_{AVDD} = 5V, V_{DVDD} = 3.3V, V_{REF} = 2.5V, and f_{CLK} = 7.68MHz (internal). The ENOB is given by:

$$ENOB = \frac{\ln(FSR / RMS\ Noise)}{\ln(2)} \quad (1)$$

Where:
FSR = Full-scale range.

The noise-free bits of resolution are shown in Table 3. Table 1 to Table 3 show that the chip performance when the input buffer is enabled. Table 4 to Table 6 show that the chip performance when the input buffer is disabled.

Input Multiplexer

The SGM58601A provides 9 analog inputs, which can be configured as 4 independent differential inputs, 8 single-ended inputs, or a combination of differential and single-ended inputs. The SGM58600A provides 3 analog inputs, which can be configured as 1 differential input or 2 single-ended inputs. The SGM58602A provides 4 analog inputs, which can be configured as 2 independent differential inputs, 3 single-ended inputs. When using the SGM58600A or SGM58602A programming the inputs, make sure to select only the available inputs when programming the input multiplexer control register (MUX).

To minimize the power consumption of the chip, it is better to keep unused input pins floating. While considering enhancing its immunity to environmental interference, those unused input pins can be connected to GND via a 10kΩ resistor.

Open/Short Sensor Detection

Figure 5 shows a demo connection of external sensor equal circuits, in which R_{SENS} is the sensor equal output impedance.

Please note that when the SDCS (Sensor Detection Current Source) is enabled, the input buffer is forced on regardless of BUFEN bit setting.

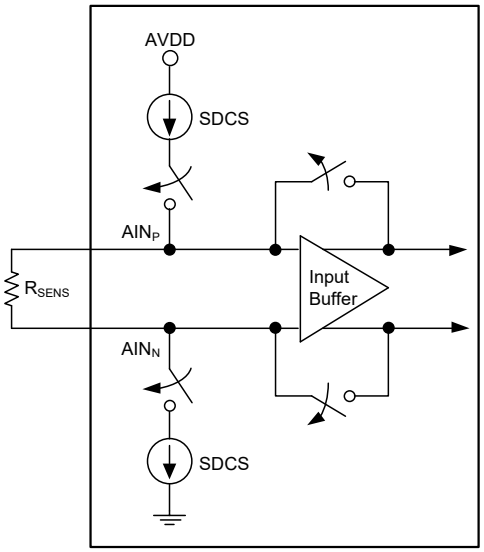


Figure 5. Sensor Detection Circuitry

DETAILED DESCRIPTION (continued)

Table 1. Input-Referred Noise (μV, RMS) with Buffer On

Data Rate (SPS)	PGA							
	1	2	4	8	16	32	64	128
2.5	0.291	0.163	0.074	0.069	0.047	0.034	0.028	0.027
5	0.377	0.172	0.101	0.086	0.064	0.048	0.044	0.042
10	0.404	0.200	0.123	0.110	0.102	0.064	0.057	0.051
15	0.512	0.198	0.170	0.136	0.112	0.087	0.074	0.078
25	0.533	0.246	0.225	0.184	0.140	0.107	0.081	0.081
30	0.630	0.278	0.231	0.192	0.150	0.103	0.109	0.097
50	0.760	0.411	0.293	0.251	0.199	0.156	0.126	0.122
60	0.812	0.487	0.303	0.260	0.222	0.156	0.140	0.142
100	1.138	0.576	0.438	0.363	0.284	0.201	0.182	0.182
500	2.183	1.113	0.863	0.816	0.628	0.461	0.396	0.394
1000	2.888	1.554	1.220	1.132	0.886	0.652	0.553	0.564
2000	3.951	2.126	1.658	1.550	1.239	0.929	0.784	0.762
3750	5.363	2.885	2.230	2.086	1.684	1.243	1.080	1.037
7500	7.401	4.054	3.139	2.904	2.276	1.757	1.494	1.444
15000	10.04	5.431	4.065	3.666	2.920	2.240	1.878	1.902
30000	12.09	6.571	4.926	4.268	3.284	2.477	2.156	2.117
60000	52.77	26.25	13.81	8.653	5.625	3.894	3.273	2.984

Table 2. Effective Number of Bits (ENOB, Bits) with Buffer On

Data Rate (SPS)	PGA							
	1	2	4	8	16	32	64	128
2.5	25.0	24.9	24.8	24.1	23.7	23.1	22.4	21.4
5	24.7	24.8	24.6	23.8	23.2	22.6	21.7	20.8
10	24.6	24.6	24.3	23.4	22.5	22.2	21.4	20.6
15	24.2	24.6	23.8	23.1	22.4	21.8	21.0	19.9
25	24.2	24.3	23.4	22.7	22.1	21.5	20.9	19.9
30	23.9	24.1	23.4	22.6	22.0	21.5	20.5	19.6
50	23.6	23.5	23.0	22.2	21.6	20.9	20.2	19.3
60	23.6	23.3	23.0	22.2	21.4	20.9	20.1	19.1
100	23.1	23.1	22.4	21.7	21.1	20.6	19.7	18.7
500	22.1	22.1	21.5	20.5	19.9	19.4	18.6	17.6
1000	21.7	21.6	21.0	20.1	19.4	18.9	18.1	17.1
2000	21.3	21.2	20.5	19.6	18.9	18.4	17.6	16.6
3750	20.8	20.7	20.1	19.2	18.5	17.9	17.1	16.2
7500	20.4	20.2	19.6	18.7	18.1	17.4	16.7	15.7
15000	19.9	19.8	19.2	18.4	17.7	17.1	16.3	15.3
30000	19.7	19.5	19.0	18.2	17.5	16.9	16.1	15.2
60000	17.5	17.5	17.5	17.1	16.8	16.3	15.5	14.7

Table 3. Noise-Free Resolution (Bits) with Buffer On

Data Rate (SPS)	PGA							
	1	2	4	8	16	32	64	128
2.5	22.7	22.3	22.0	21.6	21.1	20.6	20.0	18.9
5	22.3	22.2	21.5	21.2	20.7	20.3	19.4	18.7
10	22.1	22.1	21.5	20.8	20.1	19.9	19.1	18.0
15	21.8	21.8	21.2	20.7	20.0	19.5	18.6	17.7
25	21.6	21.6	21.0	20.3	19.6	19.2	18.3	17.4
30	21.3	21.4	21.0	20.1	19.5	18.9	18.2	17.1
50	20.9	21.0	20.3	19.7	19.1	18.4	17.8	16.9
60	20.8	20.9	20.3	19.6	19.0	18.5	17.7	16.6
100	20.3	20.3	19.8	19.1	18.3	17.8	17.1	16.2
500	19.2	19.1	18.6	17.7	17.0	16.5	15.7	14.7
1000	18.9	18.8	18.1	17.2	16.6	16.0	15.3	14.2
2000	18.4	18.3	17.6	16.8	16.1	15.6	14.8	13.8
3750	18.0	17.9	17.2	16.4	15.7	15.1	14.3	13.4
7500	17.5	17.3	16.8	15.9	15.2	14.6	13.9	12.8
15000	16.9	16.9	16.5	15.5	14.8	14.3	13.5	12.5
30000	16.6	16.7	16.1	15.3	14.7	14.1	13.3	12.3
60000	14.7	14.7	14.6	14.3	14.0	13.4	12.7	11.7

DETAILED DESCRIPTION (continued)

Table 4. Input-Referred Noise (μV, RMS) with Buffer Off

Data Rate (SPS)	PGA							
	1	2	4	8	16	32	64	128
2.5	0.315	0.162	0.093	0.065	0.038	0.036	0.025	0.028
5	0.376	0.183	0.122	0.101	0.065	0.049	0.048	0.036
10	0.512	0.236	0.156	0.127	0.090	0.072	0.063	0.057
15	0.442	0.266	0.159	0.129	0.111	0.087	0.065	0.072
25	0.905	0.332	0.228	0.168	0.143	0.089	0.085	0.084
30	0.927	0.293	0.236	0.176	0.155	0.111	0.102	0.096
50	1.385	0.529	0.273	0.261	0.191	0.146	0.132	0.123
60	1.444	0.587	0.313	0.253	0.219	0.162	0.143	0.130
100	1.636	0.772	0.435	0.346	0.282	0.212	0.175	0.172
500	2.431	1.234	0.899	0.816	0.625	0.473	0.396	0.390
1000	3.058	1.658	1.209	1.096	0.886	0.651	0.556	0.551
2000	4.109	2.198	1.678	1.557	1.202	0.931	0.798	0.770
3750	5.267	2.933	2.264	2.105	1.679	1.239	1.081	1.045
7500	7.250	4.012	3.005	2.891	2.285	1.739	1.422	1.441
15000	10.20	5.466	3.987	3.703	2.930	2.223	1.897	1.863
30000	12.54	6.766	4.927	4.256	3.316	2.561	2.138	2.157
60000	51.26	25.975	14.236	8.701	5.521	3.865	3.151	3.050

Table 5. Effective Number of Bits (ENOB, Bits) with Buffer Off

Data Rate (SPS)	PGA							
	1	2	4	8	16	32	64	128
2.5	24.9	24.9	24.7	24.2	24.0	23.1	22.6	21.4
5	24.7	24.7	24.3	23.6	23.2	22.6	21.6	21.0
10	24.2	24.3	23.9	23.2	22.7	22.1	21.2	20.4
15	24.4	24.2	23.9	23.2	22.4	21.8	21.2	20.0
25	23.4	23.8	23.4	22.8	22.1	21.7	20.8	19.8
30	23.4	24.0	23.3	22.8	21.9	21.4	20.6	19.6
50	22.8	23.2	23.1	22.2	21.6	21.0	20.2	19.3
60	22.7	23.0	22.9	22.2	21.4	20.9	20.1	19.2
100	22.5	22.6	22.5	21.8	21.1	20.5	19.8	18.8
500	22.0	22.0	21.4	20.5	19.9	19.3	18.6	17.6
1000	21.6	21.5	21.0	20.1	19.4	18.9	18.1	17.1
2000	21.2	21.1	20.5	19.6	19.0	18.4	17.6	16.6
3750	20.9	20.7	20.1	19.2	18.5	17.9	17.1	16.2
7500	20.4	20.2	19.7	18.7	18.1	17.5	16.7	15.7
15000	19.9	19.8	19.3	18.4	17.7	17.1	16.3	15.4
30000	19.6	19.5	19.0	18.2	17.5	16.9	16.2	15.1
60000	17.6	17.6	17.4	17.1	16.8	16.3	15.6	14.6

Table 6. Noise-Free Resolution (Bits) with Buffer Off

Data Rate (SPS)	PGA							
	1	2	4	8	16	32	64	128
2.5	22.6	22.2	21.9	21.6	21.1	20.6	20.0	18.9
5	22.3	22.1	21.6	21.2	20.7	20.3	19.4	18.7
10	22.0	21.8	21.3	20.8	20.1	19.9	19.1	18.0
15	21.8	21.5	21.3	20.7	20.0	19.5	18.6	17.7
25	21.4	21.6	21.0	20.3	19.6	19.2	18.3	17.4
30	21.2	21.4	21.0	20.1	19.5	18.9	18.2	17.1
50	20.6	20.8	20.4	19.7	19.1	18.4	17.8	16.9
60	20.5	20.6	20.3	19.6	19.0	18.5	17.7	16.6
100	20.2	20.2	19.7	19.1	18.3	17.8	17.1	16.2
500	19.2	19.1	18.6	17.7	17.0	16.5	15.7	14.7
1000	18.8	18.7	18.0	17.2	16.6	16.0	15.3	14.2
2000	18.4	18.2	17.6	16.8	16.1	15.6	14.8	13.8
3750	17.9	17.9	17.2	16.4	15.7	15.1	14.3	13.4
7500	17.5	17.4	16.8	15.9	15.2	14.6	13.9	12.8
15000	17.0	16.8	16.4	15.5	14.8	14.3	13.5	12.5
30000	16.7	16.6	16.1	15.3	14.7	14.1	13.3	12.3
60000	14.7	14.7	14.6	14.3	14.0	13.4	12.7	11.7

DETAILED DESCRIPTION (continued)

Programmable Gain Amplifier (PGA)

The PGA[2:0] is controlled by the ADCON register. It is recommended to recalibrate the analog-to-digital converter after changing the PGA setting.

Table 7. Full-Scale Input Voltage (V_{IN}) vs. PGA Setting

PGA Setting	Full-Scale Input Voltage (1) (V_{REF} = 2.5V)
1	±5V
2	±2.5V
4	±1.25V
8	±0.625V
16	±312.5mV
32	±156.25mV
64	±78.125mV
128	±39.0625mV

NOTE:

1. Positive inputs minus negative inputs are the voltage range and at the same time to make sure that both positive inputs and negative inputs are absolutely positive respect to ground (listed in the Electrical Characteristics section).

Modulator Input Circuitry

The SGM5860xA modulator measures the input signal by using internal capacitors that are continuously sampled and reverse sampled between the differential inputs.

When the chip is converting, it draws current from input. The equal input impedance $Z_{eff} = V_{IN}/I_{AVERAGE}$. Figure 6 shows the input equal circuitry by their effective impedances.

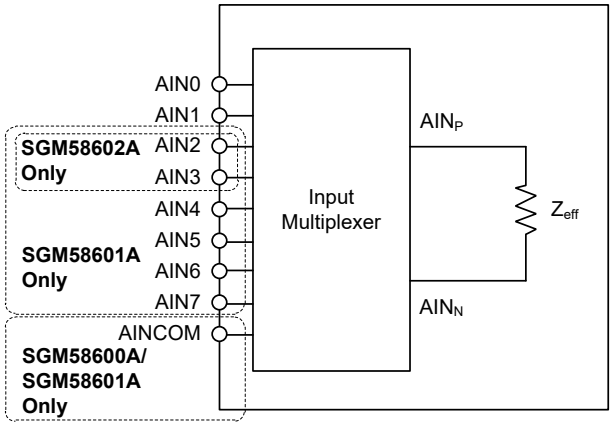


Figure 6. Analog Input Effective Impedances with Buffer On/Off

The effective impedances with buffer off for f_{CLK} = 7.68MHz (internal) is shown in Table 8.

Table 8. Effective Impedances with Buffer Off

PGA Setting	Z_{eff} (kΩ)
1	130
2	68
4	68
8	260
16	190
32	190
64	190
128	190

NOTE:

1. f_{CLK} = 7.68MHz (internal).

Analog Input Buffer

To increase the input impedance of SGM5860xA, the input buffer can be enabled by the BUFEN bit in the STATUS register. The input impedance equal circuits are shown in Figure 6. Table 9 lists the values of Z_{eff} for the different PGA settings. The equal input impedance changes inversely with the CLK frequency (f_{CLK}). For example, when the f_{CLK} is reduced by half to 3.84MHz, Z_{eff} for PGA[2:0] = 1 will double from 6MΩ to 12MΩ.

Table 9. Effective Impedances with Buffer On

PGA Setting	Z_{eff} (MΩ)
1	6
2	4
4	4
8	10
16	8
32	4
64	4
128	2

NOTE:

1. f_{CLK} = 7.68MHz (internal).

Voltage Reference Inputs (VREFP, VREFN)

The voltage reference of the SGM5860xA ADC is the differential voltage between V_{REFP} and V_{REFN}: $V_{REF} = V_{REFP} - V_{REFN}$.

DETAILED DESCRIPTION (continued)

Digital Filter

Inside the chip, there is a Sinc^5 filter and an average filter after the modulator. Its equal architecture is shown in Figure 7.

Table 10 shows the data rate setting and real data rate under f_{CLK} = 7.68MHz. Note that if the f_{CLK} increases, the read data rate increases accordingly. For example, the f_{CLK} from 7.68MHz to 10MHz increases the data rate for DR[7:0] = 11110001 from 60000SPS to 78125SPS.

Table 10. Number of Averages and Data Rate Setting

DRATE DR[7:0]	Number of Averages for Programmable Filter (Num_Ave)	Data Rate (1) (SPS)
11110001	1	60000
11110000	1	30000
11100000	2	15000
11010000	4	7500
11000000	8	3750
10110000	15	2000
10100001	30	1000
10010010	60	500
10000010	300	100
01110010	500	60
01100011	600	50
01010011	1000	30
01000011	1200	25
00110011	2000	15
00100011	3000	10
00010011	6000	5
00000011	12,000	2.5

NOTE:

1. f_{CLK} = 7.68MHz (internal).

Frequency Response

The chip low-pass digital filter can be calculated based on the following equation:

$$|H(f)| = |H_{Sinc^5}(f)| \times |H_{Averager}(f)|$$
$$= \left| \frac{\sin\left(\frac{256\pi \times f}{f_{CLKIN}}\right)}{64 \times \sin\left(\frac{4\pi \times f}{f_{CLKIN}}\right)} \right|^5 \times \left| \frac{\sin\left(\frac{256\pi \times Num_Ave\ f}{f_{CLKIN}}\right)}{Num_Ave \times \sin\left(\frac{256\pi \times f}{f_{CLKIN}}\right)} \right| \quad (2)$$

To eliminate 50Hz (or 60Hz) noise from power supply, set the data rate equal to 2.5SPS, 5SPS, 10SPS, 15SPS, 30SPS, or 50SPS (or 60Hz).

Table 11. First-Notch Frequency and -3dB Bandwidth Filter

Data Rate (1) (SPS)	First-Notch (Hz)	-3dB Bandwidth (Hz)
60000	60000	12000
30000	30000	6106
15000	15000	4807
7500	7500	3003
3750	3750	1615
2000	2000	878
1000	1000	441
500	500	221
100	100	44.2
60 (2)	60	26.5
50 (3)	50	22.1
30 (2)	30	13.3
25 (3)	25	11.1
15 (2)	15	6.63
10 (4)	10	4.42
5 (4)	5	2.21
2.5 (4)	2.5	1.1

NOTES:

1. f_{CLK} = 7.68MHz (internal).
2. Notch at 60Hz.
3. Notch at 50Hz.
4. Notch at 50Hz and 60Hz.

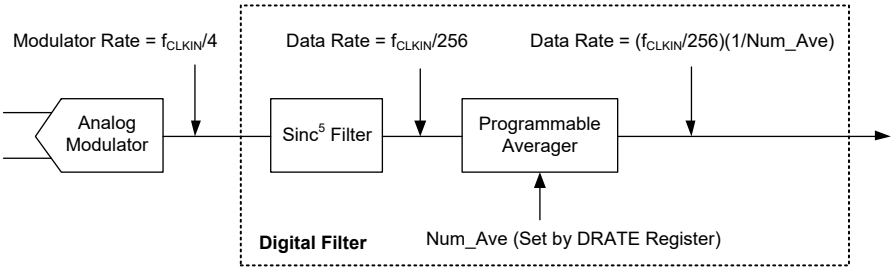


Figure 7. Architecture of the Analog Modulator and Digital Filter

DETAILED DESCRIPTION (continued)

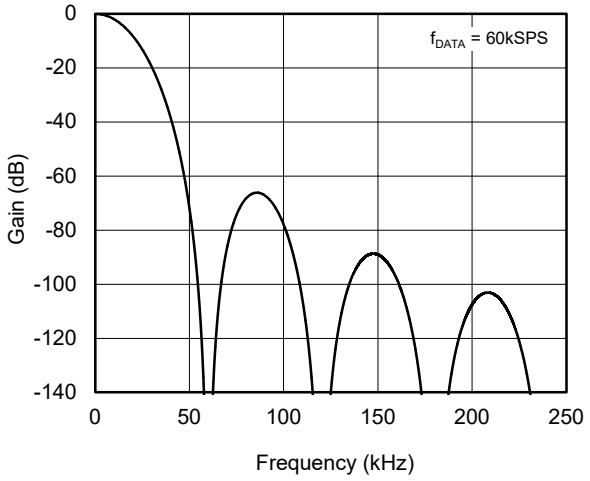


Figure 8. Frequency Response (Data Rate = 60kSPS)

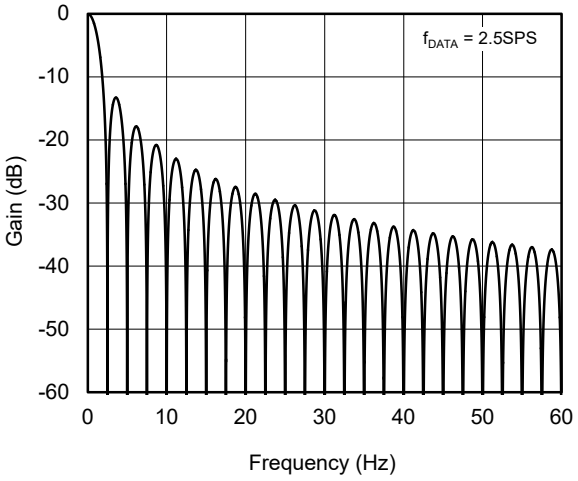


Figure 9. Frequency Response (Data Rate = 2.5SPS)

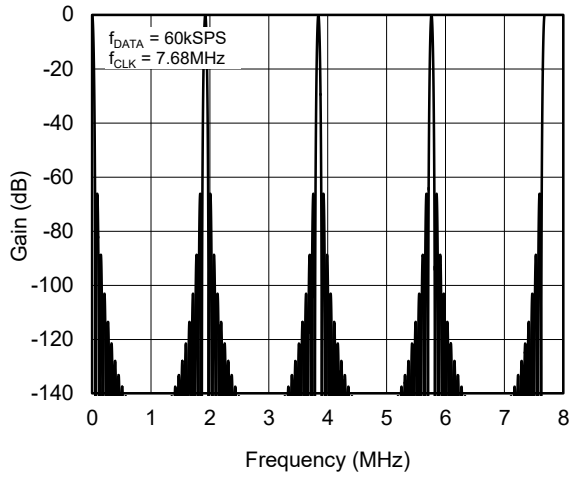


Figure 10. Frequency Response Out to 7.68MHz (Data Rate = 60kSPS)

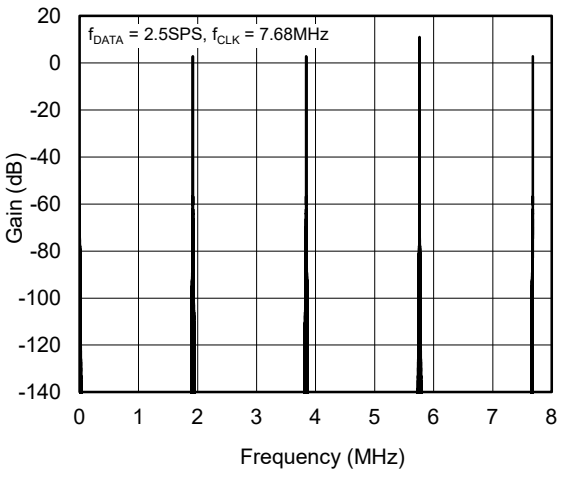


Figure 11. Frequency Response Out to 7.68MHz (Data Rate = 2.5SPS)

DETAILED DESCRIPTION (continued)

Settling Time

Table 12 shows the settling time for the different data rates.

Table 12. Settling Time for Different Data Rates

Data Rate (1) (SPS)	Settling Time (t_{14}) (ms)
60000	0.132
30000	0.23
15000	0.27
7500	0.33
3750	0.47
2000	0.69
1000	1.20
500	2.20
100	10.20
60	16.90
50	20.30
30	33.50
25	40.20
15	67.00
10	100.20
5	200.20
2.5	400.20

NOTES:

1. f_{CLK} = 7.68MHz (internal).

2. In one-shot mode, a small additional delay is needed to start the device from standby.

Settling Time Using the Input Multiplexer

The fastest way to switch the input multiplexer is to issue a WREG command immediately when nDRDY goes low, then the next channel conversion starts and the conversion data of previous channel can be read at the same time. Figure 12 shows a timing demo of channel switching and data read. Note that when cycling through channel, nDRDY goes low to indicate data is ready, and there is no data setting time (all processing data are discarded internally).

1. When nDRDY goes low, indicating that data is ready to read.

2. It will take 14 × τ_{CLKIN} for nDRDY to go from low to high, after WREG command is received by ADC.

Table 13 shows the throughput speed when cycling the input multiplexer.

Table 13. Multiplexer Cycling Throughput

Data Rate (1) (SPS)	Cycling Throughput ($1/t_{15}$) (Hz)
60000	7353
30000	4237
15000	3650
7500	2994
3750	2110
2000	1441
1000	831
500	454
100	98
60	59.2
50	49.3
30	29.8
25	24.8
15	15
10	10
5	5
2.5	2.5

NOTE:

1. f_{CLK} = 7.68MHz (internal).

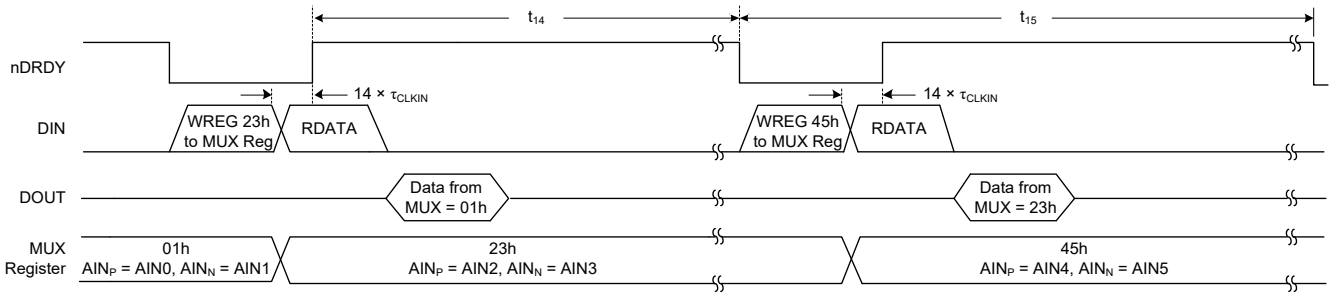


Figure 12. Cycling the SGM5860xA Input Multiplexer

DETAILED DESCRIPTION (continued)

Settling Time Using One-Shot Mode

Issuing a STANDBY command can let chip go into low power standby mode. A WAKEUP command can wake up the chip and perform one time one-shot conversion. It will take t_{14} conversion cycles to wake up and fully settle the conversion data. After the conversion, another STANDBY command is required to enter standby again. Figure 13 shows the sequence.

Settling Time while Continuously Converting

In the continuous mode, when there is a step change of the input, it usually needs several nDRDY periods to fully set up the data, which is shown in Table 14.

Table 14. Data Settling Delay vs. Data Rate

Data Rate (SPS)	Settling Time (nDRDY Periods)
60000	5
30000	5
15000	3
7500	2
3750	1
2000	1
1000	1
500	1
100	1
60	1
50	1
30	1
25	1
15	1
10	1
5	1
2.5	1

Data Format

The SGM5860xA output 24-bit data in binary two's complement format. The ideal output codes for different input signals are summarized as shown in Table 15.

Table 15. Ideal Output Code for Different Input Signals

Input Signal V_{IN} (AIN_P - AIN_N)	Ideal Output Code (1)
$\geq \frac{+2V_{REF}}{PGA}$	7FFFFFh
$\frac{+2V_{REF}}{PGA(2^{23}-1)}$	000001h
0	000000h
$\frac{-2V_{REF}}{PGA(2^{23}-1)}$	FFFFFFh
$\leq \frac{-2V_{REF}}{PGA}\left(\frac{2^{23}}{2^{23}-1}\right)$	800000h

NOTE:

1. Except for effects of INL, noise, offset, and gain errors.

General-Purpose Digital I/O (D0 to D3)

The SGM58601A has 4 digital I/O pins and the SGM58600A/SGM58602A have 2 digital I/O pins. All I/O pins are separately controllable by IO registers. During standby and power-down modes, the GPIOs are still active. If GPIOs work as output, they keep driving output. If the digital I/O pins are not used, either configure them as input and connect them to ground or configure them as outputs. This will reduce power dissipation.

Clock Output (D0/CLKOUT)

The clock output can be a clock source for other processor.

Clock Generation

The chip has an internal on-chip oscillator, which is switched on by default after the system powers up or after a reset event. The internal oscillator can be switched off and configured as an external clock source by setting the Status2 register (bit [4]).

After receiving the command to switch from the internal oscillator to the external clock source, the chip will take 4.6ms to fully set up the working clock block. During this period, any operation on the chip is prohibited.

The chip external clock source can be an external oscillator (need an external crystal 7.68MHz), or an external clock source. When the source is an oscillator, two capacitors (typically 5pF to 20pF) are needed to connect both of oscillator's output pins to ground.

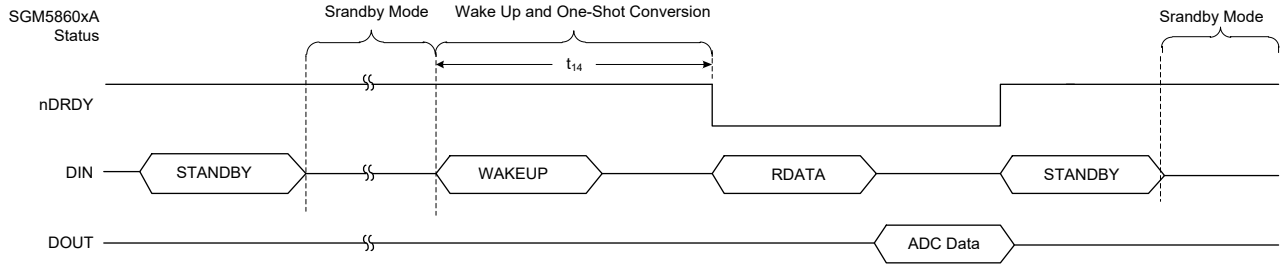


Figure 13. One-Shot Conversions Using the STANDBY Command

DETAILED DESCRIPTION (continued)

Calibration

The chip has offset calibration (OFCx) and gain calibration (FSCx) registers, which are used to compensate and minimize offset error and gain error of ADC results.

Offset errors are corrected with the offset calibration registers (OFCx) and gain errors are corrected with the full-scale calibration registers (FSCx).

The output of the SGM5860xA after calibration is given by:

$$\text{Output} = \left(\frac{\text{PGA} \times V_{IN}}{2V_{REF}} \times \frac{3}{4} - \frac{\text{OFC}}{0x400000} \right) \times \text{FSC} \times 2 \quad (3)$$

The OFC is a binary two's complement number, the ideal value is 0. The FSC is unipolar, and the ideal number is 0x555555. The OFC and the FSC keep the same with different data rate settlings. For noise consideration, the offset and full-scale errors can be calibrated at a lower data rate.

The SGM5860xA provides chip self-calibration and system calibration function (these are a series of command SELFOCAL, SELFGCAL, SELFCAL, SYSOCAL, and SYSGCAL). Once calibration is initiated, nDRDY goes high until the process is completed.

During the chip self-calibration, the internal data rate will be set to 1kSPS by the chip if it is greater than 1kSPS, otherwise, it will be calibrated according to the set data rate. In order to achieve a successful self-calibration, it is necessary to ensure that the reference voltage is fully set up and that the AVDD and DVDD of the chip must be compatible with the requirements in the specification. During this period, any operation on the chip is prohibited. After self-calibration, the default data rate is reset to the set data rate.

The calibration should be performed after ADC initialization and be performed again after the buffer any configuration changes or PGA resetting.

Self-Calibration

The time required for self-offset calibration for the different data rate settings is shown in Table 16. The calibration time is decreased with f_{CLK} increasing. After a self-offset calibration, the OFC registers is updated automatically.

The time required for self-gain calibration under the different data rate and PGA settings is shown in Table 17. The self-gain calibration can update the FSC registers.

Table 16. Self-Offset and System Offset Calibration Timing

Data Rate (1) (SPS)	Self-Offset Calibration and System Offset Calibration Time (ms)
60000	1.31
30000	1.42
15000	1.44
7500	1.51
3750	1.64
2000	1.88
1000	2.36
500	4.36
100	20.4
60	33.6
50	40.2
30	67
25	80
15	133
10	200
5	400
2.5	800

NOTE:

1. f_{CLK} = 7.68MHz (internal).

Table 17. Self-Gain Calibration Timing

Data Rate (1) (SPS)	PGA Setting (ms)	
	1, 2	4, 8, 16, 32, 64, 128
60000	2.5	7.28
30000	2.59	7.38
15000	2.62	7.4
7500	2.69	7.5
3750	2.83	7.62
2000	3.1	7.84
1000	3.58	8.4
500	6.6	15.38
100	30.5	71.4
60	50.4	118
50	60.2	141
30	100.2	233
25	120.4	280
15	200	468
10	300	702
5	600	1400
2.5	1194	2800

NOTE:

1. f_{CLK} = 7.68MHz (internal).

DETAILED DESCRIPTION (continued)

The time required for self-calibration under the different data rate settings is shown in Table 18. The self-calibration can update both the OFC and FSC registers.

Table 18. Self-Calibration Timing

Data Rate (1) (SPS)	PGA Setting (ms)	
	1, 2	4, 8, 16, 32, 64, 128
60000	3.7	8.47
30000	3.8	8.56
15000	3.83	8.6
7500	3.9	8.67
3750	4.03	8.8
2000	4.27	9.03
1000	4.77	9.53
500	8.77	17.53
100	40.77	81.53
60	67.43	134.86
50	80.76	161.52
30	134.09	268.19
25	160.76	321.52
15	267.42	534.84
10	400.7	801.4
5	800.7	1601.4
2.5	1600.6	3201.3

NOTE:

1. f_{CLK} = 7.68MHz (internal).

System Calibration

To perform a system offset calibration, the user must supply a zero input differential signal. The time required for system offset calibration under the different data rate settings is shown in Table 19. The system offset calibration can update the OFC registers.

To perform a system gain calibration, the user must supply a full-scale input signal to the SGM5860xA. The time required for system gain calibration under the different data rate settings is shown in Table 19. The system gain calibration can update the FSC registers.

Auto-Calibration

Auto-calibration is allowed to enable (ACAL bit in STATUS register) when completing the write command (WREG).

Serial Interface

The SGM5860xA has an SPI-compatible interface, including nCS, SCLK, DIN and DOUT.

Reset

There are two methods to reset the SGM5860xA: the nRESET input pin and RESET command.

Table 19. System Gain (Offset) Calibration Timing

Data Rate (1) (SPS)	System Gain Calibration Time (ms)
60000	1.32
30000	1.42
15000	1.44
7500	1.51
3750	1.64
2000	1.88
1000	2.38
500	4.38
100	20.4
60	33.6
50	40.2
30	67
25	80
15	133
10	200
5	400
2.5	800

NOTE:

1. f_{CLK} = 7.68MHz (internal).

Synchronization

There are two kinds of ways to synchronize input sampling, SYNC command and nSYNC/nPDWN pin control. The first method is to shift in 8-bit SYNC command, this makes the chip ready to synchronize, and then issue WAKEUP command to synchronize the sampling of the input signal on the first rising edge of SCLK shifted in by WAKEUP. The second method is to pull nSYNC/nPDWN pin low and then set it high, synchronization happens on the rising edge of nSYNC/nPDWN.

Standby Mode

In standby mode, the chip turns off all analog circuits and some of the digital circuits. The oscillator circuits still keep working. A WAKEUP command lets the chip exit standby mode. See Figure 13 for details.

Power-Down Mode

In power-down mode, all circuits are turned off, including oscillator and clock output. To enter power-down, set nSYNC/nPDWN pin low and keep it for 20 nDRDY cycles.

To get out of power-down mode, set the nSYNC/nPDWN pin high, it will take the chip about 30ms to wake up if an external crystal oscillator is used. It will take about 8192 CLKIN cycles to wake up if an external clock source is used. It will take the chip about 7μs to wake up if the internal clock source is used.

Power-Up

After a power-up, all registers are reset to their default values.

REGISTER MAPS

Table 20. Register Maps

Register Address	Register Name	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	STATUS: Status Register	01h	ID[3:0]				ORDER	ACAL	BUFEN	nDRDY
01h	MUX: Input Multiplexer Control Register	01h	PSEL[3:0]				NSEL[3:0]			
02h	ADCON: A/D Control Register	20h	0	CLK[1:0]		SDCS[1:0]		PGA[2:0]		
03h	DRATE: A/D Data Rate Register	F0h	DR[7:0]							
04h	IO: GPIO Control Register	E0h	DIR[3:0]				DIO[3:0]			
05h	OFC0: Offset Calibration Byte 0 - Least Significant Byte	00h	OFC[7:0]							
06h	OFC1: Offset Calibration Byte 1	00h	OFC[15:8]							
07h	OFC2: Offset Calibration Byte 2 - Most Significant Byte	00h	OFC[23:16]							
08h	FSC0: Full-Scale Calibration Byte 0 - Least Significant Byte	55h	FSC[7:0]							
09h	FSC1: Full-Scale Calibration Byte 1	55h	FSC[15:8]							
0Ah	FSC2: Full-Scale Calibration Byte 2 - Most Significant Byte	55h	FSC[23:16]							
0Bh	STATUS2: Status2 Register	10h	Reserved			OSC_ SEL	REF_ BUFP	REF_ BUFM	AIN_ BUFP	AIN_ BUFM

REG0x00: Status Register (STATUS) [Reset = 01h]

BITS	BIT NAME	DEFAULT	DESCRIPTION
D[7:4]	ID[3:0]	0000	Factory Programmable Identification Bits Read only.
D[3]	ORDER	0	Data Output Bit Order 0 = Most significant bit first (default) 1 = Least significant bit first ORDER setting has no effect on input data. Output data is always out by most significant byte firstly. ORDER setting only has effect on the shifting out sequence within byte.
D[2]	ACAL	0	Auto-Calibration 0 = Auto-calibration disabled (default) 1 = Auto-calibration enabled When auto-calibration is enabled, self-calibration starts at the completion of the WREG command that changes the values of the PGA[2:0] bits in the ADCON register, DR[7:0] in the DRATE register or BUFEN bit in the STATUS register.
D[1]	BUFEN	0	Analog Input Buffer Enable 0 = Buffer disabled. Positive and negative buffers are controlled by AIN_BUFP and AIN_BUFM further (default) 1 = Buffer enabled. Positive and negative buffers are enabled no matter how AIN_BUFP, AIN_BUFM are
D[0]	nDRDY		Data Ready Read only. This bit copies the status of nDRDY pin.

REGISTER MAPS (continued)

REG0x01: Input Multiplexer Control Register (MUX) [Reset = 01h]

BITS	BIT NAME	DEFAULT	DESCRIPTION
D[7:4]	PSEL[3:0]	0000	Positive Input Channel (AIN_P) Select 0000 = AIN0 (SGM5860xA) (default) 0001 = AIN1 (SGM5860xA) 0010 = AIN2 (SGM58601A/SGM58602A only) 0011 = AIN3 (SGM58601A/SGM58602A only) 0100 = AIN4 (SGM58601A only) 0101 = AIN5 (SGM58601A only) 0110 = AIN6 (SGM58601A only) 0111 = AIN7 (SGM58601A only) 1xxx = AINCOM (SGM58600A/SGM58601A only) Ensure only available inputs are selected when using the SGM58600A. When PSEL[3] = 1, PSEL[2], PSEL[1], PSEL[0] are don't care.
D[3:0]	NSEL[3:0]	0001	Negative Input Channel (AIN_N) Select 0000 = AIN0 (SGM5860xA) 0001 = AIN1 (SGM5860xA) (default) 0010 = AIN2 (SGM58601A/SGM58602A only) 0011 = AIN3 (SGM58601A/SGM58602A only) 0100 = AIN4 (SGM58601A only) 0101 = AIN5 (SGM58601A only) 0110 = AIN6 (SGM58601A only) 0111 = AIN7 (SGM58601A only) 1xxx = AINCOM (SGM58600A/SGM58601A only) Ensure to only select the available inputs when using the SGM58600A. When NSEL[3] = 1, NSEL[2], NSEL[1], NSEL[0] are don't care.

REG0x02: A/D Control Register (ADCON) [Reset = 20h]

BITS	BIT NAME	DEFAULT	DESCRIPTION
D[7]	Reserved	0	Reserved. Always 0. Read only.
D[6:5]	CLK[1:0]	01	D0/CLKOUT Clock Out Rate 00 = Clock out off 01 = Clock out frequency = f_{CLK} (default) 10 = Clock out frequency = $f_{CLK}/2$ 11 = Clock out frequency = $f_{CLK}/4$ When CLKOUT is not used, it is recommended to turn it off.
D[4:3]	SDCS[1:0]	00	Sensor Detection Current Sources 00 = Sensor detection off (default) 01 = Sensor detection current = 0.5μA 10 = Sensor detection current = 2μA 11 = Sensor detection current = 9μA
D[2:0]	PGA[2:0]	000	Programmable Gain Amplifier 000 = 1 (default) 001 = 2 010 = 4 011 = 8 100 = 16 101 = 32 110 = 64 111 = 128

REGISTER MAPS (continued)

REG0x03: A/D Data Rate Register (DRATE) [Reset = F0h]

BITS	BIT NAME	DEFAULT	DESCRIPTION
D[7:0]	DR[7:0]	1111 0000	Data Rate 1111 0001 = 60000SPS 1111 0000 = 30000SPS (default) 1110 0000 = 15000SPS 1101 0000 = 7500SPS 1100 0000 = 3750SPS 1011 0000 = 2000SPS 1010 0001 = 1000SPS 1001 0010 = 500SPS 1000 0010 = 100SPS 0111 0010 = 60SPS 0110 0011 = 50SPS 0101 0011 = 30SPS 0100 0011 = 25SPS 0011 0011 = 15SPS 0010 0011 = 10SPS 0001 0011 = 5SPS 0000 0011 = 2.5SPS The 17 valid data rate settings are shown in this table.

REG0x04: GPIO Control Register (IO) [Reset = E0h]

BITS	BIT NAME		DEFAULT	DESCRIPTION
D[7:4]	DIR[3:0]	DIR[3]	1	Digital I/O Direction for Pin D3 0 = It is an output 1 = It is an input (default) For SGM58601A only.
		DIR[2]	1	Digital I/O Direction for Pin D2 0 = It is an output 1 = It is an input (default) For SGM58601A only.
		DIR[1]	1	Digital I/O Direction for Pin D1 0 = It is an output 1 = It is an input (default)
		DIR[0]	0	Digital I/O Direction for Pin D0/CLKOUT 0 = It is an output (default) 1 = It is an input
D[3:0]	DIO[3:0]		0000	Status of Digital I/O Pins D3, D2, D1, D0/CLKOUT It is used for GPIO pins data read and write. When the GPIO pin is an input configuration, a write operation has no effect on it. A read operation is effective on both input pins and output pins. When D0/CLKOUT is used for clock output, DIO[0] setting has no effect.

REGISTER MAPS (continued)

REG0x05: Offset Calibration Byte 0 - Least Significant Byte (OFC0) [Reset = 00h]

BITS	BIT NAME	DEFAULT	DESCRIPTION
D[7:0]	OFC[7:0]	0000 0000	

REG0x06: Offset Calibration Byte 1 (OFC1) [Reset = 00h]

BITS	BIT NAME	DEFAULT	DESCRIPTION
D[7:0]	OFC[15:8]	0000 0000	

REG0x07: Offset Calibration Byte 2 - Most Significant Byte (OFC2) [Reset = 00h]

BITS	BIT NAME	DEFAULT	DESCRIPTION
D[7:0]	OFC[23:16]	0000 0000	

REG0x08: Full-Scale Calibration Byte 0 - Least Significant Byte (FSC0) [Reset = 55h]

BITS	BIT NAME	DEFAULT	DESCRIPTION
D[7:0]	FSC[7:0]	0101 0101	

REG0x09: Full-Scale Calibration Byte 1 (FSC1) [Reset = 55h]

BITS	BIT NAME	DEFAULT	DESCRIPTION
D[7:0]	FSC[15:8]	0101 0101	

REG0x0A: Full-Scale Calibration Byte 2 - Most Significant Byte (FSC2) [Reset = 55h]

BITS	BIT NAME	DEFAULT	DESCRIPTION
D[7:0]	FSC[23:16]	0101 0101	

REG0x0B: Status2 Register (STATUS2) [Reset = 10h]

BITS	BIT NAME	DEFAULT	DESCRIPTION
D[7:5]	Reserved	000	Reserved, should always be set to 000.
D[4]	OSC_SEL	1	Select Oscillator Source for ADC Modulator and Filter 0 = External clock source (external oscillator or external clock) 1 = Internal oscillator (default)
D[3]	REF_BUFP	0	Positive Reference Input Buffer Enable 0 = Buffer disabled (default) 1 = Buffer enabled
D[2]	REF_BUFM	0	Negative Reference Input Buffer Enable 0 = Buffer disabled (default) 1 = Buffer enabled
D[1]	AIN_BUFP	0	Positive Analog Input Buffer Enable 0 = Buffer disabled (default) 1 = Buffer enabled Functions when BUFEN = 0.
D[0]	AIN_BUFM	0	Negative Analog Input Buffer Enable 0 = Buffer disabled (default) 1 = Buffer enabled Functions when BUFEN = 0.

COMMAND DEFINITIONS

Table 21 summarizes the commands that control the operation of the SGM5860xA. All commands are single byte excluding RREG and WREG.

Table 21. Command Definitions

Command	Description	First Command Byte	Second Command Byte
WAKEUP	Complete SYNC and Exit Standby Mode	0000 0000 (00h)	
RDATA (2)	Read Data	0000 0001 (01h)	
RDATAC (2)	Read Data Continuous	0000 0011 (03h)	
SDATAC (2)	Stop Read Data Continuous	0000 1111 (0Fh)	
RREG	Read from Register ssss (1)	0001 ssss (1xh) (1)	0000 qqqq (1)
WREG	Write to Register ssss (1)	0101 ssss (5xh) (1)	0000 qqqq (1)
SELFCAL	Offset and Gain Self-Calibration	1111 0000 (F0h)	
SELFOCAL	Offset Self-Calibration	1111 0001 (F1h)	
SELFGCAL	Gain Self-Calibration	1111 0010 (F2h)	
SYSOCAL	System Offset Calibration	1111 0011 (F3h)	
SYSGCAL	System Gain Calibration	1111 0100 (F4h)	
SYNC	Synchronize the A/D Conversion	1111 1100 (FCh)	
STANDBY	Begin Standby Mode	1111 1101 (FDh)	
RESET	Reset to Power-Up Values	1111 1110 (FEh)	
WAKEUP	Complete SYNC and Exit Standby Mode	1111 1111 (FFh)	

NOTES:

1. qqqq = number of registers to be read/written - 1. For example, to read/write three registers, set qqqq = 0b0010. ssss = starting register address for read/write commands.

2. Issue this command after nDRDY goes low.

SELFCAL: Offset and Gain Self-Calibration

Issue an offset and gain self-calibration command. When the calibration starts, nDRDY goes high. When the calibration completes, nDRDY goes low, and settled data is ready. Do not perform any more operations during this calibration.

SELFOCAL: Offset Self-Calibration

Issue an offset self-calibration command. When beginning the calibration, nDRDY goes high. When the calibration completes, nDRDY goes low, and settled data is ready. Do not do any more operations during this calibration.

SELFGCAL: Gain Self-Calibration

Issue a gain self-calibration command. When beginning the calibration, nDRDY goes high. When the calibration completes, nDRDY goes low, and settled data is ready. Do not do any more operations during this calibration.

SYSOCAL: System Offset Calibration

Issue a system offset calibration command. When beginning the calibration, nDRDY goes high. When the calibration completes, nDRDY goes low, and settled data is ready. Do not do any more operations during this calibration.

SYSGCAL: System Gain Calibration

Issue a system gain calibration command. When beginning the calibration, nDRDY goes high. When the calibration completes, nDRDY goes low, and settled data is ready. Do not do any more operations during this calibration.

RESET: Reset Registers to Default Values

Reset all registers to default values except CLK[1:0] setting (which is in ADCON register).

COMMAND DEFINITIONS (continued)

WAKEUP: Complete SYNC or Exit Standby Mode

The WAKEUP command is used in conjunction with the SYNC and STANDBY commands. It provides two values: all zeros or all ones.

RDATAC: Read Data Continuous

When nDRDY is low, issue the RDATAC command, the chip will give out ADC conversion results continuously, see Figure 14 for details.

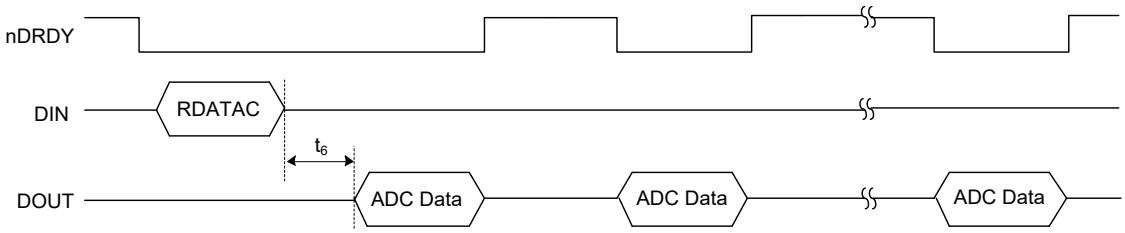


Figure 14. RDATAC Command Sequence

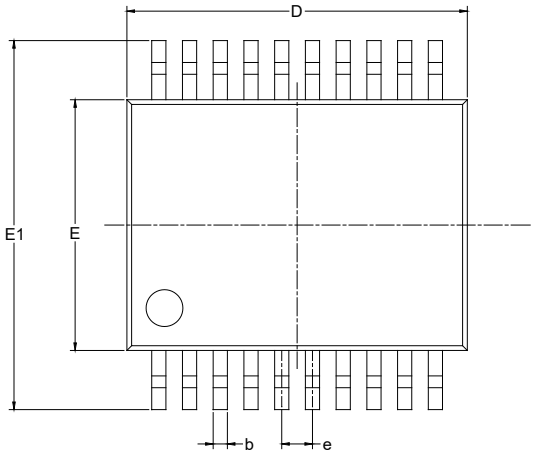
REVISION HISTORY

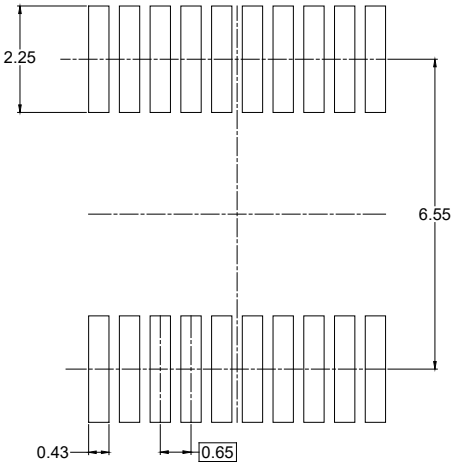
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (OCTOBER 2024)	Page
Changed from product preview to production data	All

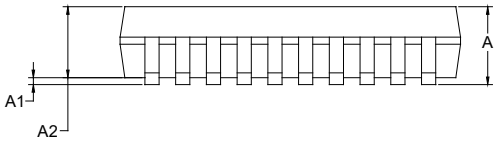
PACKAGE OUTLINE DIMENSIONS

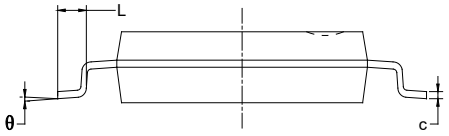
SSOP-20





RECOMMENDED LAND PATTERN (Unit: mm)



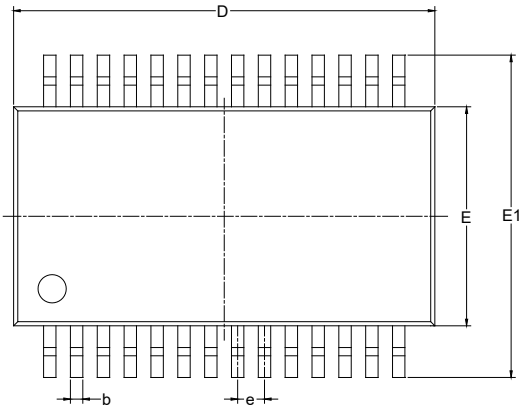


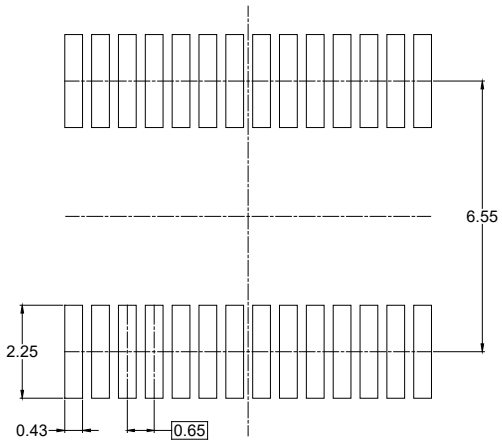
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.730		0.068
A1	0.050	0.230	0.002	0.009
A2	1.400	1.600	0.055	0.063
b	0.220	0.380	0.009	0.015
c	0.090	0.250	0.004	0.010
D	7.000	7.400	0.276	0.291
E	5.100	5.500	0.201	0.217
E1	7.600	8.000	0.299	0.315
e	0.65 BSC		0.026 BSC	
L	0.550	0.950	0.022	0.037
θ	0°	8°	0°	8°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

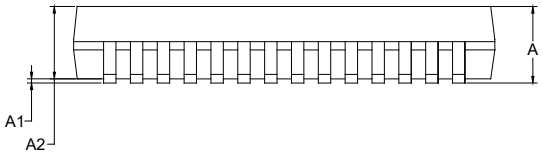
PACKAGE OUTLINE DIMENSIONS

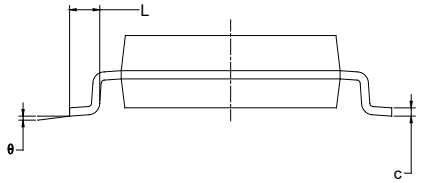
SSOP-28





RECOMMENDED LAND PATTERN (Unit: mm)



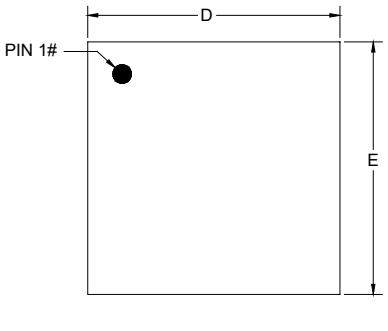


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		2.000		0.079
A1	0.050		0.002	
A2	1.650	1.850	0.065	0.073
b	0.220	0.380	0.009	0.015
c	0.090	0.250	0.004	0.010
D	9.900	10.500	0.390	0.413
E	5.000	5.600	0.197	0.220
E1	7.400	8.200	0.291	0.323
e	0.65 BSC		0.026 BSC	
L	0.550	0.950	0.022	0.037
θ	0°	8°	0°	8°

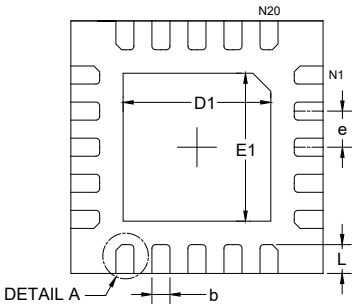
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

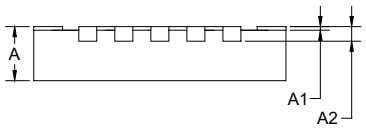
TQFN-3.5×3.5-20L



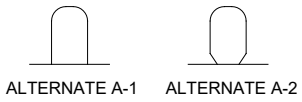
TOP VIEW



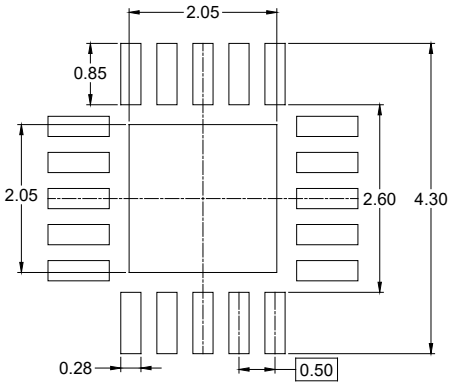
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



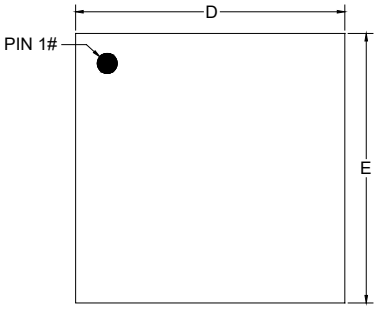
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	-	-	0.050
A2	0.203 REF		
D	3.450	3.500	3.550
D1	2.000	2.050	2.100
E	3.450	3.500	3.550
E1	2.000	2.050	2.100
b	0.200	0.250	0.300
e	0.500 BSC		
L	0.350	0.400	0.450

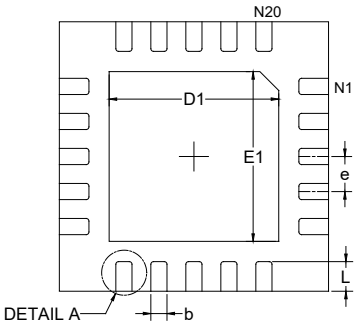
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

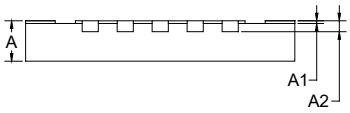
TQFN-5×5-20L



TOP VIEW



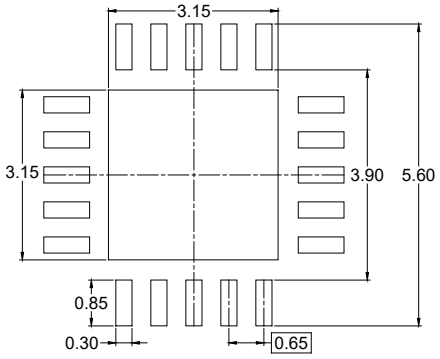
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



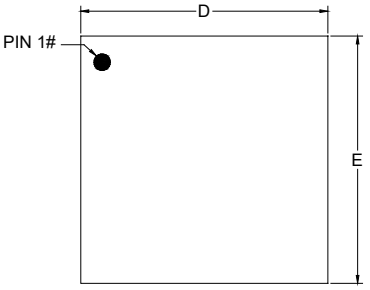
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
D	4.950	5.000	5.050
D1	3.100	3.150	3.200
E	4.950	5.000	5.050
E1	3.100	3.150	3.200
b	0.250	0.300	0.350
e	0.650 BSC		
L	0.500	0.550	0.600

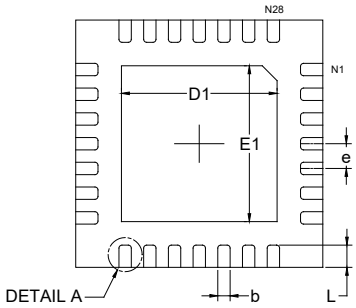
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

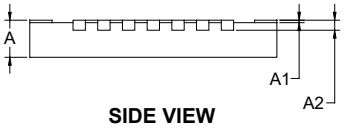
TQFN-5×5-28L



TOP VIEW



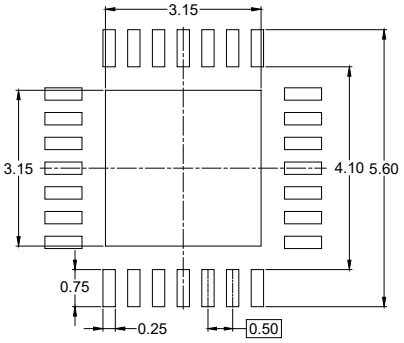
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



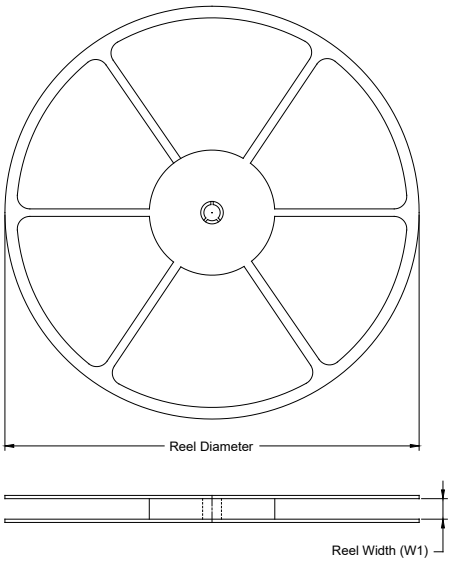
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
D	4.950	5.000	5.050
D1	3.100	3.150	3.200
E	4.950	5.000	5.050
E1	3.100	3.150	3.200
b	0.200	0.250	0.300
e	0.500 BSC		
L	0.400	0.450	0.500

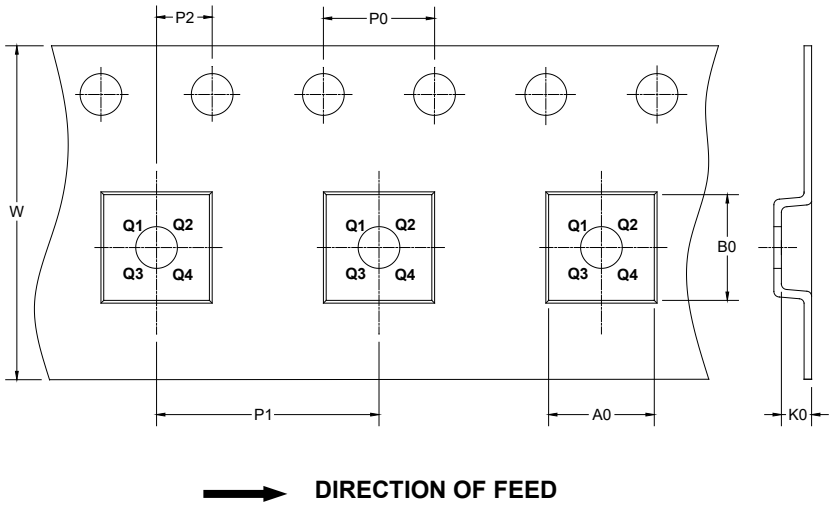
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



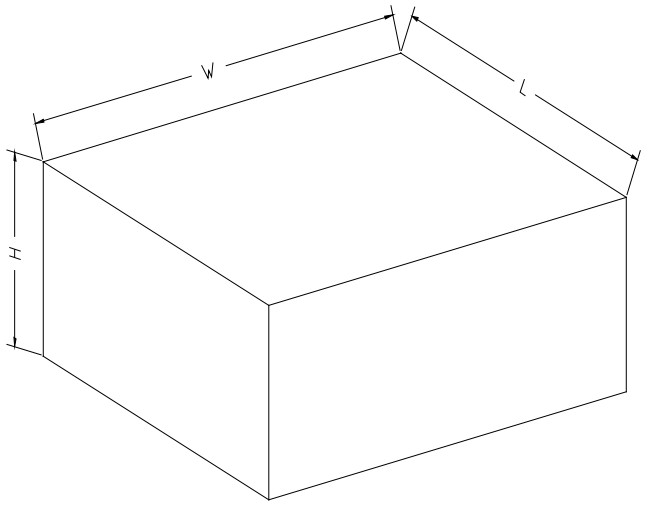
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SSOP-20	13″	16.4	8.40	7.75	2.50	4.0	12.0	2.0	16.0	Q1
SSOP-28	13″	16.4	8.20	10.50	2.34	4.0	12.0	2.0	16.0	Q1
TQFN-3.5×3.5-20L	13″	12.4	3.80	3.80	0.95	4.0	8.0	2.0	12.0	Q2
TQFN-5×5-20L	13″	12.4	5.30	5.30	1.10	4.0	8.0	2.0	12.0	Q2
TQFN-5×5-28L	13″	12.4	5.30	5.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002