# SGM58200
# Ultra-Small, Low-Power, 24-Bit ADC with Internal Reference

## GENERAL DESCRIPTION

The SGM58200 is a low-power, 24-bit, precision, sigma-delta (Σ-Δ) analog-to-digital converter (ADC). It operates from a 3V to 5.5V supply.

The SGM58200 contains an on-chip reference and oscillator. It has an $I^2C$-compatible interface, and it can select four $I^2C$ slave addresses. The data rate of the filter is up to 960SPS. The SGM58200 has an on-chip PGA, which can provide input ranges to as low as ±256mV from the power supply.

The input multiplexer supports 4 single-ended inputs or 2 differential inputs configuration.

The SGM58200 is available in Green MSOP-10 and UTQFN-2×1.5-10L packages. It operates over an ambient temperature range of -40℃ to +125℃.

## FEATURES

- **Single-Supply Voltage Range: 3V to 5.5V**
  - **$I^2C$ Bus Voltage Range: 3V to 5.5V**
- **Low Quiescent Current:**
  - **Continuous Mode: 255μA (TYP)**
  - **Power-Down Mode: 0.8μA (TYP)**
- **Selectable Data Rates: 6.25SPS to 960SPS**
- **Input Multiplexer**
  - **4 Single-Ended Inputs or 2 Differential Inputs**
- **Internal Programmable Gain Amplifier (PGA)**
- **Internal Voltage Reference and Oscillator**
- **Selectable Digital Comparator**
- **$I^2C$-Compatible Serial Interface**
- **Available in Green MSOP-10 and UTQFN-2×1.5-10L Packages**

## APPLICATIONS

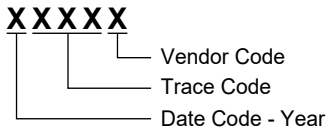
Portable Devices
Process Control
Battery Monitoring System
Temperature Measurement

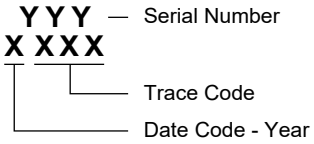
# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM58200 | MSOP-10 | -40℃ to +125℃ | SGM58200XMS10G/TR | SGM58200<br>XMS10<br>XXXXX | Tape and Reel, 4000 |
| | UTQFN-2×1.5-10L | -40℃ to +125℃ | SGM58200XURA10G/TR | CN0<br>XXXX | Tape and Reel, 3000 |

## MARKING INFORMATION

NOTE: XXXX = Date Code and Trace Code. XXXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)

$V_{DD}$ ..... -0.3V to 5.5V

Analog Input Voltage..... -0.3V to 5.5V

SDA, SCL, ADDR, ALERT/RDY Voltage ..... -0.3V to 5.5V

Input Current (Momentary)..... 100mA

Input Current (Continuous) ..... 10mA

Junction Temperature..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s)..... +260℃

ESD Susceptibility

HBM..... 4000V

CDM ..... 1000V

## RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

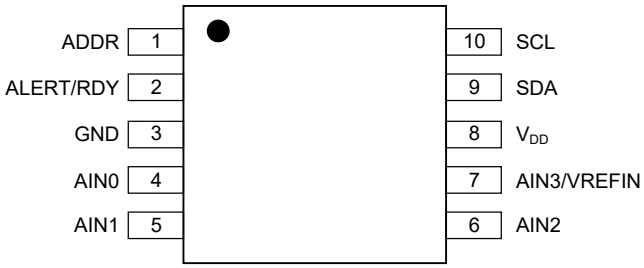
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

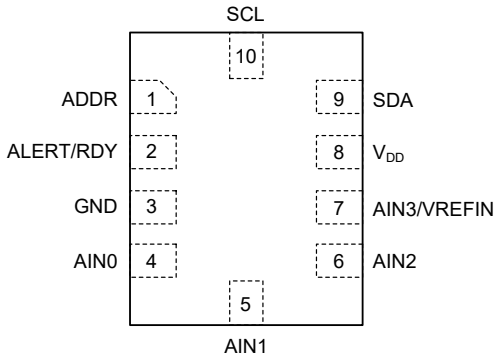
## PIN CONFIGURATIONS

(TOP VIEW)




MSOP-10

(TOP VIEW)




UTQFN-2×1.5-10L

## PIN DESCRIPTION

| PIN | | NAME | TYPE | FUNCTION |
|---|---|---|---|---|
| MSOP-10 | UTQFN-2×1.5-10L | | | |
| 1 | 1 | ADDR | DI | $I^2C$ Address Selection Pin. |
| 2 | 2 | ALERT/RDY | DO | Digital Comparator Output/Conversion Ready Pin. |
| 3 | 3 | GND | G | Ground. |
| 4 | 4 | AIN0 | AI | Positive Input of Differential Channel 1 or Input of Single-Ended Channel 1. |
| 5 | 5 | AIN1 | AI | Negative Input of Differential Channel 1 or Input of Single-Ended Channel 2. |
| 6 | 6 | AIN2 | AI | Positive Input of Differential Channel 2 or Input of Single-Ended Channel 3. |
| 7 | 7 | AIN3/VREFIN | AI | Negative Input of Differential Channel 2 or Input of Single-Ended Channel 4, or External Reference Input. |
| 8 | 8 | $V_{DD}$ | P | Power Supply Pin. It can be operated from 3V to 5.5V. |
| 9 | 9 | SDA | DIO | Serial Data Pin. |
| 10 | 10 | SCL | DI | Serial Clock Input Pin. |

NOTE: AI = analog input, DI = digital input, DO = digital output, DIO = digital input and output, P = power, G = ground.

# ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 3.3V, Full-Scale (FS) = ±2.048V, External Reference = 2.048V, maximum and minimum specifications apply from $T_A$ = -40℃ to +125℃, typical values are at $T_A$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Analog Input** | | | | | | | |
| Full-Scale Input Voltage (1) | | $V_{IN}$ = $AIN_P$ - $AIN_N$ | | | ±4.096/PGA | | V |
| Analog Input Voltage | | $AIN_P$ or $AIN_N$ to GND | | GND | | $V_{DD}$ | V |
| Differential Input Impedance | | | | | See Table 1 | | |
| **System Performance** | | | | | | | |
| Resolution | | No missing codes | | 24 | | | Bits |
| Data Rate | DR | | | | See Table 5 | | SPS |
| Data Rate Variation | | All data rates | | -6 | | 6 | % |
| Output Noise | | | | See Table 6 and Table 7 | | | |
| Integral Nonlinearity | INL | DR = 8SPS, FS = ±2.048V, best fit (99% of full-scale) | | | 6 | 20 | ppm |
| Offset Error | | FS = ±2.048V | differential inputs | | 50 | 120 | μV |
| | | | single-ended inputs | | 100 | 400 | |
| Offset Drift | | FS = ±2.048V | | | 0.1 | 3 | μV/°C |
| Offset Power-Supply Rejection | | FS = ±2.048V | | | 80 | | μV/V |
| Gain Error (2) | | FS = ±2.048V at +25℃ | | | 0.08 | 0.25 | % |
| Gain Drift (3) | | FS = ±0.256V | | | 1 | | ppm/℃ |
| | | FS = ±2.048V | | | 1 | 10 | |
| | | FS = ±6.144V (1) | | | 1 | | |
| Gain Power-Supply Rejection | | | | | 30 | 150 | ppm/V |
| PGA Gain Match (2) | | Match between any two PGA gains | MSOP-10 | | 0.1 | 0.35 | % |
| | | | UTQFN-2×1.5-10L | | 0.1 | 0.40 | |
| Gain Match | | Match between any two inputs | | | 0.01 | 0.08 | % |
| Offset Match | | Match between any two gains | | | 30 | 400 | μV |
| 50/60Hz Rejection | | FS = ±2.048V | | | 95 | | dB |
| Channel-to-Channel Crosstalk | | At DC and FS = ±2.048V, differential or single-ended inputs adjacent channels | | | 120 | | dB |
| Common-Mode Rejection Ratio | CMRR | At DC and FS = ±0.256V | | | 110 | | dB |
| | | At DC and FS = ±2.048V | | | 110 | | |
| | | At DC and FS = ±6.144V (1) | | | 110 | | |
| **Internal Clock** | | | | | | | |
| Frequency | | DR_SEL = 0 | | 393 | 410 | 434 | kHz |

NOTES:

1. The full-scale range of the ADC scaling. In any event, it should not exceed $V_{DD}$ + 0.3V be applied to this device.
2. Testing with external reference.
3. Gain temperature drift is defined as the maximum change of gain error measured over the specified temperature range. The gain error drift is calculated using the box method, as described by Equation: Gain Error Drift = ($GE_{MAX}$ - $GE_{MIN}$)/($T_{MAX}$ - $T_{MIN}$). Where:

• $GE_{MAX}$ and $GE_{MIN}$ are the maximum and minimum gain errors, respectively.
• $T_{MAX}$ and $T_{MIN}$ are the maximum and minimum temperatures, respectively, over the temperature range -40℃ to +125℃.

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 3.3V, Full-Scale (FS) = ±2.048V, External Reference = 2.048V, maximum and minimum specifications apply from $T_A$ = -40℃ to +125℃, typical values are at $T_A$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Reference** | | | | | | | |
| Internal Reference | | | | | 2.048 | | V |
| External Reference | | | | 0.5 | | 2.5 | V |
| External Reference Input Current | | VREFIN = 2.5V, continuous mode | | | 0.45 | | μA |
| **Digital Input/Output** | | | | | | | |
| High Input Voltage (4) | $V_{IH}$ | | | 0.7 × $V_{BUS}$ | | | V |
| Low Input Voltage (4) | $V_{IL}$ | | | | | 0.3 × $V_{BUS}$ | V |
| Low Output Voltage | $V_{OL}$ | $I_{OL}$ = 3mA | | | 0.07 | 0.4 | V |
| High Input Leakage Current (5) | $I_{IH}$ | $V_{IH}$ = 5.5V | | | 0.1 | 1 | μA |
| Low Input Leakage Current (5) | $I_{IL}$ | $V_{IL}$ = GND | | | 0.1 | 1 | μA |
| **Power-Supply Requirements** | | | | | | | |
| Power-Supply Voltage | $V_{DD}$ | | | 3 | | 5.5 | V |
| Supply Current | $I_{DD}$ | $V_{DD}$ = 5.5V | Power-down current at +25℃ (6) | | 0.8 | 1.2 | μA |
| | | | Power-down current up to +125℃ (6) | | 1.8 | 3.5 | |
| | | | Operating current at +25℃ | | 255 | 350 | |
| | | | Operating current up to +125℃ | | 270 | 380 | |
| Power Dissipation | $P_D$ | $V_{DD}$ = 5V | | | 1.05 | | mW |
| | | $V_{DD}$ = 3.3V | | | 0.6 | | |

NOTES:

4. There are 2 scenarios: $V_{DD}$ = 5V, $V_{BUS}$ can be 3V to 5V; $V_{DD}$ = 3.3V, $V_{BUS}$ should be 3.3V. Note that $V_{BUS}$ = 3V may cause leakage in some extreme conditions, and it's better to make it higher than 3.1V. For $V_{BUS}$ = $V_{DD}$, $V_{IL}$/$V_{IH}$ = 30%/70% of $V_{BUS}$. For $V_{BUS}$ = 3.3V and $V_{DD}$ = 5V, $V_{IL}$/$V_{IH}$ = 20%/80% of $V_{BUS}$.

5. Meet the "loss of $V_{DD}$" requirement of $I^2C$ fast mode. When $V_{DD}$ is lost, the leakage drawn from the pin is controlled.

6. Power-down current increases to 2.3μA at +25℃ and 3.5μA at +125℃ when Config1 BUS_FLEX bit is set to '1'.

## TIMING CHARACTERISTICS

| PARAMETER | SYMBOL | STANDARD MODE | | FAST MODE | | HIGH-SPEED MODE | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| SCL Operating Frequency | $f_{SCL}$ | 0.01 | 0.1 | 0.01 | 0.4 | 0.01 | 3.4 | MHz |
| Bus Free Time between START and STOP Condition | $t_1$ | 4700 | | 600 | | 160 | | ns |
| Hold Time after Repeated START Condition. After This Period, the First Clock is Generated | $t_2$ | 4000 | | 600 | | 160 | | ns |
| SCL Clock Low Time | $t_3$ | 4700 | | 1300 | | 160 | | ns |
| SCL Clock High Time | $t_7$ | 4000 | | 600 | | 60 | | ns |
| Repeated START Condition Setup Time | $t_9$ | 4700 | | 600 | | 160 | | ns |
| Stop Condition Setup Time | $t_{10}$ | 4000 | | 600 | | 160 | | ns |
| Data Hold Time | $t_5$ | 0 | | 0 | | 0 | | ns |
| Data Setup Time | $t_8$ | 250 | | 100 | | 10 | | ns |
| Clock/Data Fall Time (1) | $t_6$ | | 300 | | 300 | | 160 | ns |
| Clock/Data Rise Time | $t_4$ | | 1000 | | 300 | | 160 | ns |

NOTE:
1. $t_6$ (MIN) for SDA output is 20ns for normal/fast mode and 10ns for high-speed mode. Glitch filter capability is 50ns for normal/fast mode and 10ns for high-speed mode.

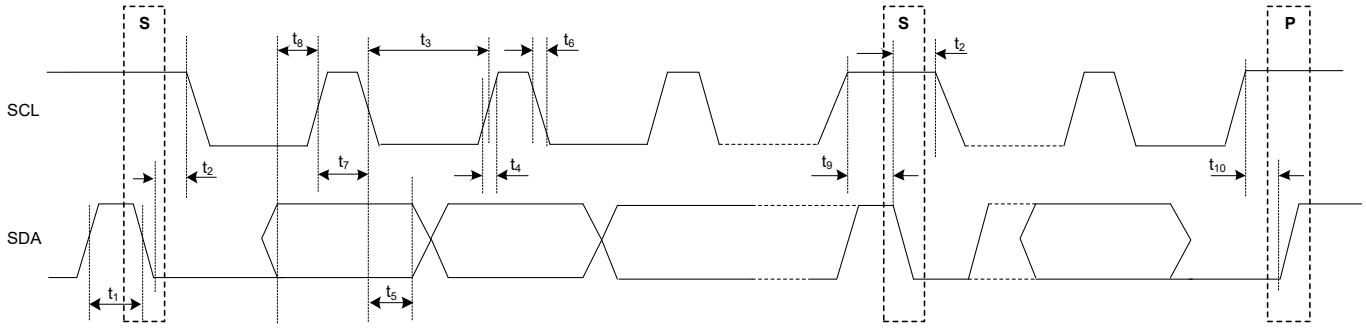



**Figure 1. I²C Timing Diagram**

## FUNCTIONAL BLOCK DIAGRAM

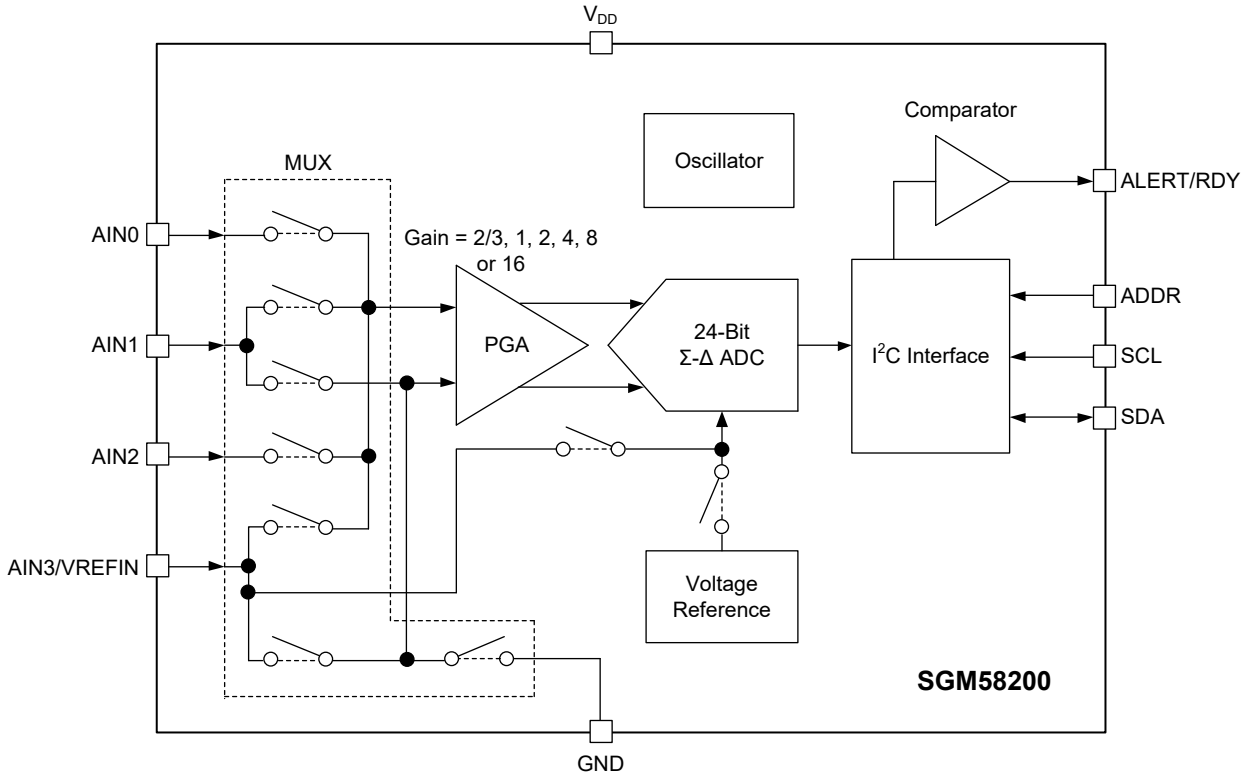



**Figure 2. Functional Block Diagram**

# DETAILED DESCRIPTION

## Overview

The SGM58200 is a low-power, 24-bit, sigma-delta (Σ-Δ) analog-to-digital converter (ADC).

The SGM58200 supports both differential inputs and single-ended inputs.

The SGM58200 has two working modes: single-shot mode and continuous conversion mode.

In single-shot mode, the ADC performs one conversion and gives full settled data, no data needs to be discarded. Once ADC completes the conversion, it then goes to low-power shutdown mode.

In continuous modes, the ADC begins a new conversion automatically after a previous conversion is completed. Every conversion result is given out. The data rate is equal to the configured data rate.

## Quickstart Guide

The basic connection of ADC is shown in Figure 3. The communication interface is $I^2C$ compatible. The SGM58200 works in slave mode. The $I^2C$ address is configured as 0b1001000 (ADDR is connected to GND).

Figure 4, Figure 5 and Figure 6 show a demo read and write operation sequence.

For example, writing to the configuration register 0x01 sets the SGM58200 to continuous conversion mode, we need the following order:

1. First byte, 0b1001000 (first 7-bit is $I^2C$ address), the $8^{th}$ bit is read/write bit which is low writing now
2. Second byte, 0b00000001 (points to Config register 0x01)
3. Third byte, 0b10000100 (MSB of the Config register to be written, Bit[8] = 0 means the continuous mode)
4. Fourth byte, 0b10000011 (LSB of the Config register to be written, Bit[7:5] = '100' means data rate 100Hz)

For example, to read the conversion result from SGM58200, the following order can be followed:

1. First byte, 0b1001000 (first 7-bit is $I^2C$ address), the $8^{th}$ bit is read/write bit which is low writing now
2. Second byte, 0b00000000 (points to Conversion register 0x00)
3. Third byte, 0b10010001 (first 7-bit is $I^2C$ address), the $8^{th}$ bit is read/write bit which is high reading now
4. Fourth byte, the SGM58200 answer with the MSB of the Conversion register
5. Fifth byte, the SGM58200 answer with the LSB of the Conversion register

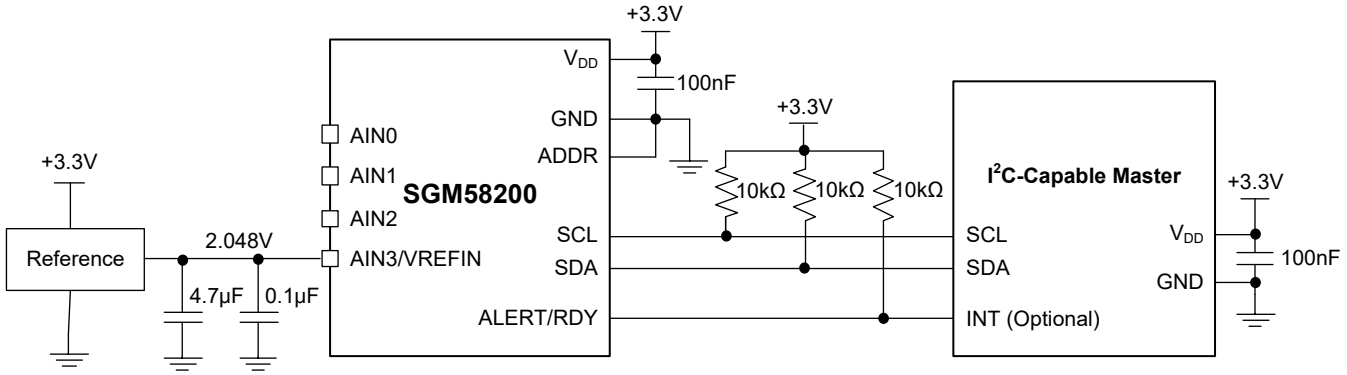
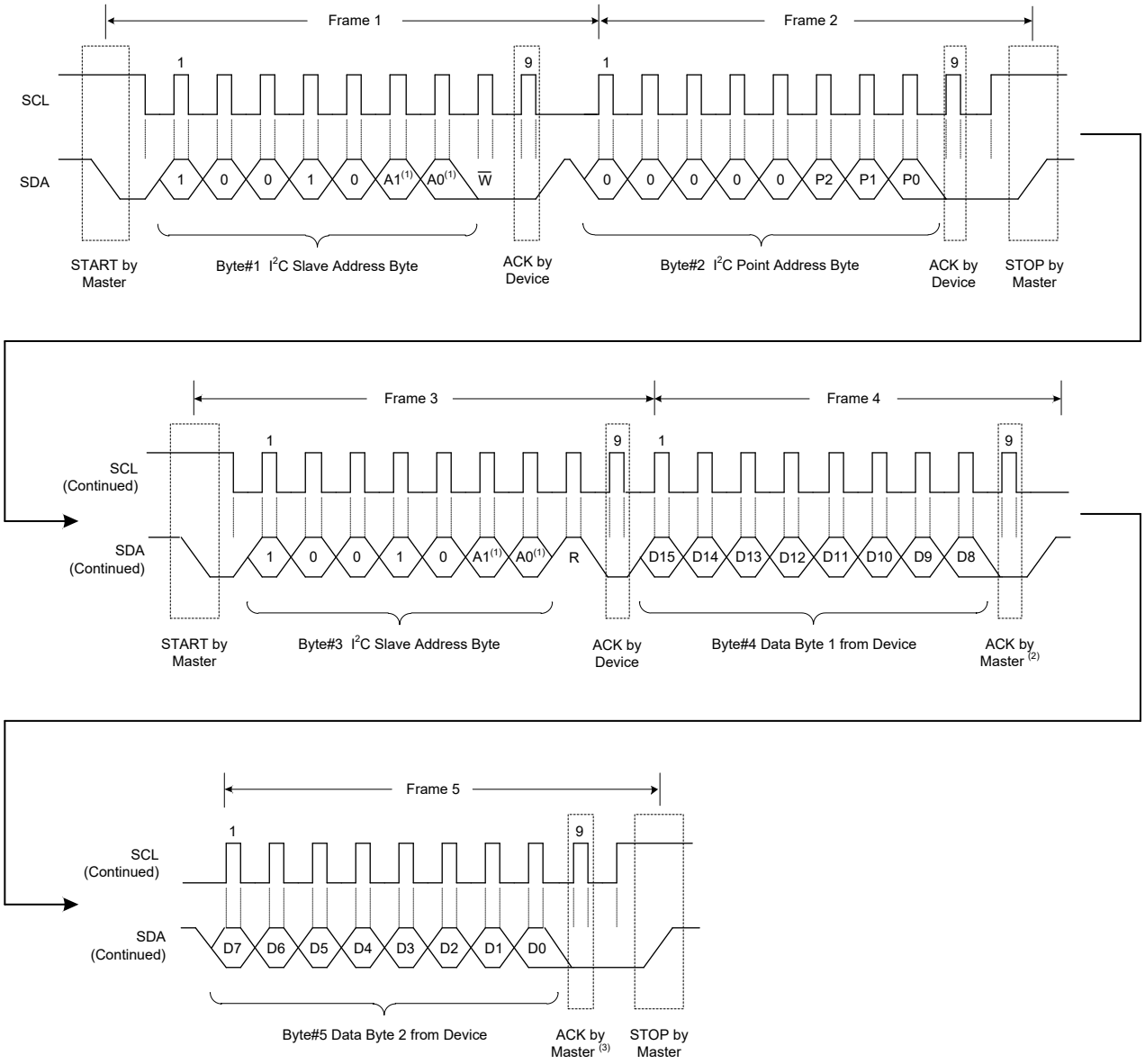



**Figure 3. Basic Hardware Configuration**

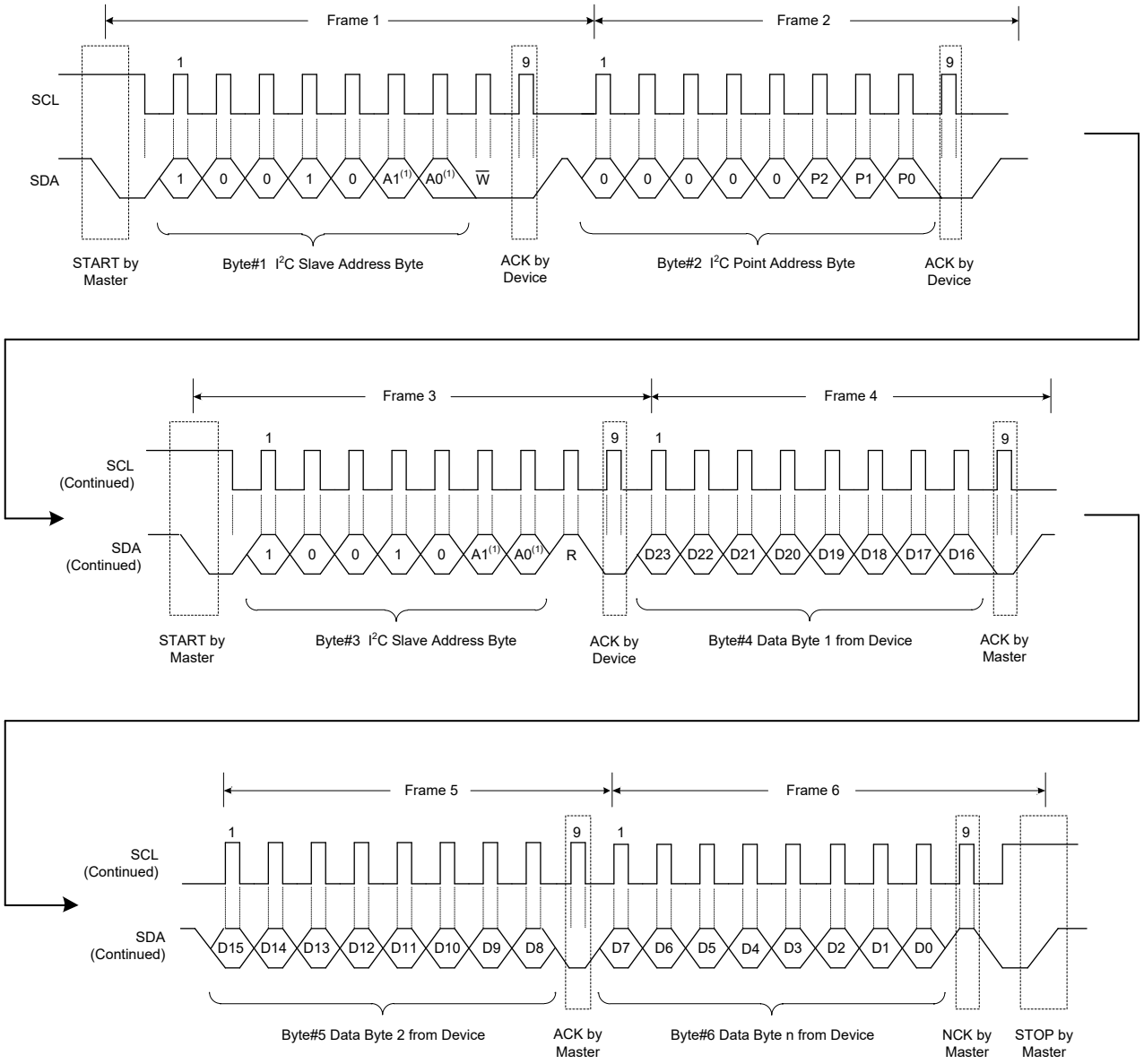
## DETAILED DESCRIPTION (continued)




NOTES:
1. The A0 and A1 values depend on the ADDR pin.
2. SDA can be set high by master to terminate a single-byte read operation.
3. SDA can be set high by master to terminate a two-byte read operation.

**Figure 4. Timing Diagram for Read Word Register**

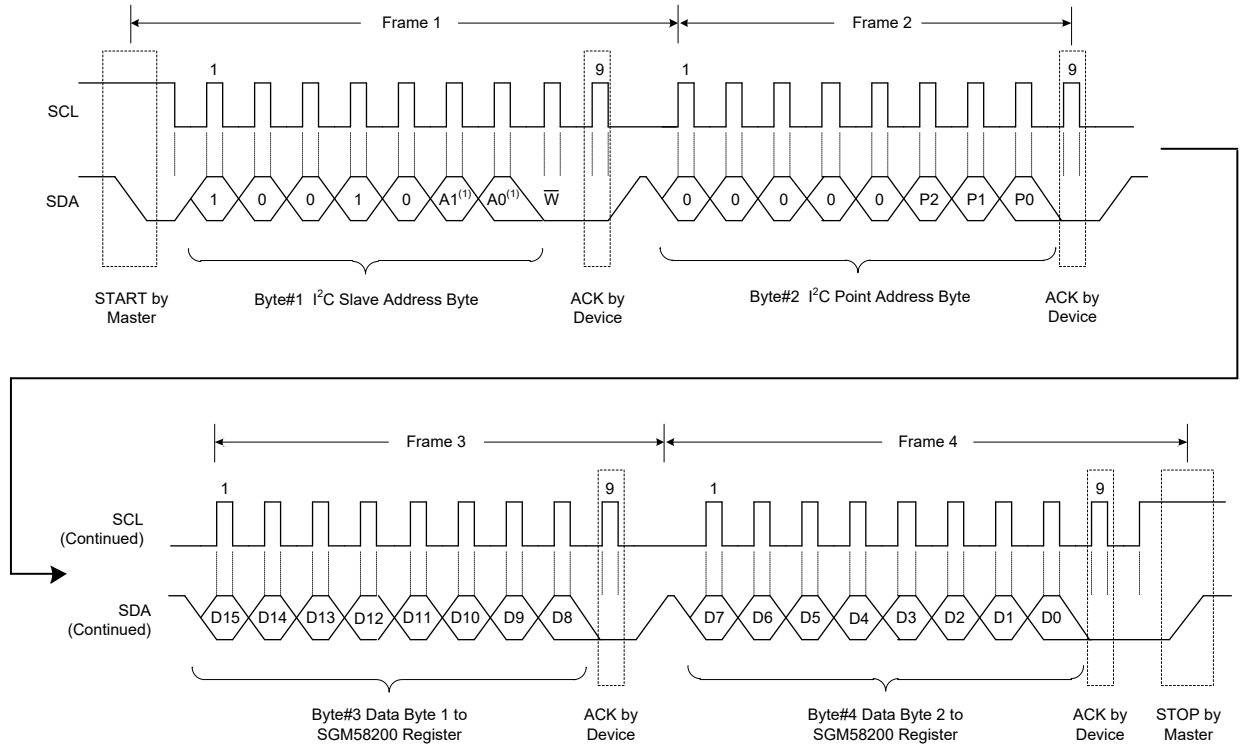
## DETAILED DESCRIPTION (continued)




NOTES:
1. The A0 and A1 values depend on the ADDR pin.
2. SDA can be set high by master to terminate a single-byte read operation.
3. SDA can be set high by master to terminate a two-byte read operation.

**Figure 5. Timing Diagram for Reading Three Bytes Register**

## DETAILED DESCRIPTION (continued)




NOTE:
1. The A0 and A1 values depend on the ADDR pin.

**Figure 6. Timing Diagram for Write Word Register**

### Multiplexer

The SGM58200 has a flexible input multiplexer. It can be configured as 2 differential inputs or 4 single-ended inputs.

Whether the input is configured as differential inputs or single-ended inputs, the absolute voltage on any inputs pin must be in the range from GND to $V_{DD}$.

### Analog Inputs

The SGM58200 has a switched capacitor input stage. There are charge and discharge current when ADC is working. The equal effective input impedance can be estimated by $R_{EFF} = V_{IN}/I_{AVERAGE}$.

The differential input impedance is $Z_{DIFF}$ in Figure 7. Table 1 shows the typical differential input impedance.

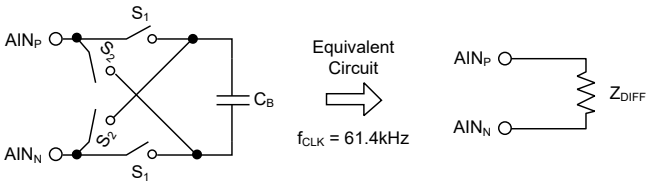



**Figure 7. Simplified Analog Input Circuit**

**Table 1. Differential Input Impedance**

| FS (V) | Differential Input Impedance |
|---|---|
| ±6.144V (1) | 37.5MΩ |
| ±4.096V (1) | 25MΩ |
| ±2.048V | 12.5MΩ |
| ±1.024V | 6.25MΩ |
| ±0.512V | 6.25MΩ |
| ±0.256V | 6.25MΩ |

NOTE:
1. FS = Full-scale range of the ADC scaling. In any event, it should not exceed $V_{DD}$ + 0.3V be applied to this device.

# DETAILED DESCRIPTION (continued)

## Full-Scale Input

The SGM58200 has an internal PGA. The PGA can be set to gains of 2/3, 1, 2, 4, 8 or 16. Table 2 and Table 3 show the corresponding full-scale (FS) ranges.

Analog input voltages can never exceed the analog input voltage limits.

**Table 2. PGA Gain Full-Scale Range with Internal Reference**

| PGA Setting | FS (V) |
|---|---|
| 2/3 | ±6.144V (1) |
| 1 | ±4.096V (1) |
| 2 | ±2.048V |
| 4 | ±1.024V |
| 8 | ±0.512V |
| 16 | ±0.256V |

NOTE:

1. FS = Full-scale range of the ADC scaling. In any event, it should not exceed $V_{DD}$ + 0.3V be applied to this device.

**Table 3. PGA Gain Full-Scale Range with External Reference**

| PGA Setting | FS (V) |
|---|---|
| 2/3 | $\pm 3 \times V_{REF}$ |
| 1 | $\pm 2 \times V_{REF}$ |
| 2 | $\pm V_{REF}$ |
| 4 | $\pm V_{REF}/2$ |
| 8 | $\pm V_{REF}/4$ |
| 16 | $\pm V_{REF}/8$ |

## Data Format

The SGM58200 conversion result data is in binary two's complement format.

Table 4 shows the ideal output codes for different input signals.

**Table 4. Ideal Output Code for Different Input Signals**

| Input Signal $V_{IN}$ ($AIN_P$ - $AIN_N$) | Ideal Output Code (1) |
|---|---|
| ≥ FS ($2^{23}$ - 1)/$2^{23}$ | 7FFFFFh |
| +FS/$2^{23}$ | 000001h |
| 0 | 0 |
| -FS/$2^{23}$ | FFFFFFh |
| ≤ -FS | 800000h |

NOTE:

1. Except for effects of INL, noise, offset, and gain errors.

## Aliasing

For some applications, an RC external filtering is recommended.

## Operating Modes

The SGM58200 has two working modes, continuous mode and single-shot mode.

In continuous mode, the ADC begins a new conversion automatically after a previous conversion is completed. Every conversion result is given out.

In single-shot mode, if OS bit is written to '1', a single-shot conversion is started, during the conversion process, the OS bit is kept '0', and the chip doesn't response to OS bit operation. If conversion data is ready, the OS bit is set to '1' and the chip goes power-down automatically, and user can write '1' to OS bit to call a single-shot conversion again.

## Power-Up and Reset

When the SGM58200 is powered up, all registers are reset to default values.

The SGM58200 supports $I^2C$ general call reset command. Details see $I^2C$ General Call section.

## Duty Cycling for Low Power

In some power sensitive application, the SGM58200 can work in sampling and power-down mode periodically. The duty cycle of working time and power-down time can be controlled by microcontroller flexibly.

For example, if the SGM58200 is configured as sample data rate at 960Hz, we can operate it with 125ms duty cycle. It means that we call the chip do single-shot conversion every 125ms, it will take the chip 3.2ms for sampling and then stay in power-down mode for 121.8ms. Under this working mode, it will reduce 39/40 power consumption compare with 960Hz operation in continuous mode.

# DETAILED DESCRIPTION (continued)

## Data Rate

**Table 5. ADC Output Data Rate (SPS)**

| DR[2:0] Bits in Config Register | DR_SEL Bit in Config1 Register | |
|---|---|---|
| | DR_SEL = 0 | DR_SEL = 1 |
| 000 | 6.25Hz | 7.5Hz |
| 001 | 12.5Hz | 15Hz |
| 010 | 25Hz | 30Hz |
| 011 | 50Hz | 60Hz |
| 100 | 100Hz | 120Hz |
| 101 | 200Hz | 240Hz |
| 110 | 400Hz | 480Hz |
| 111 | 800Hz | 960HZ |

## Comparator

The SGM58200 has an inside comparator that can be used to check ADC conversion results with high threshold and low threshold. When the result exceeds the limited setting, the chip can give an alert on the ALERT/RDY pin.

The comparator has two workings modes: traditional mode and window comparator mode. These modes are configurable. Under both working modes, the comparator can be configured as latch output or no-latch output (COMP_LAT bit in Config register). In latch output mode, the latched comparator output can be cleared by issuing an SMBus alert response or by reading the Conversion register. The ALERT/RDY pin output active polarity (low or high) can be configured by COMP_POL bit in Config register. Demos are shown in Figure 8 and Figure 9.

The comparator output trigger waiting times can be set by COMP_QUE[1:0] in Config register. It means comparator output can wait until the ADC results beyond the threshold configured times (which can be one, two, or four times). Details see Config Register section.

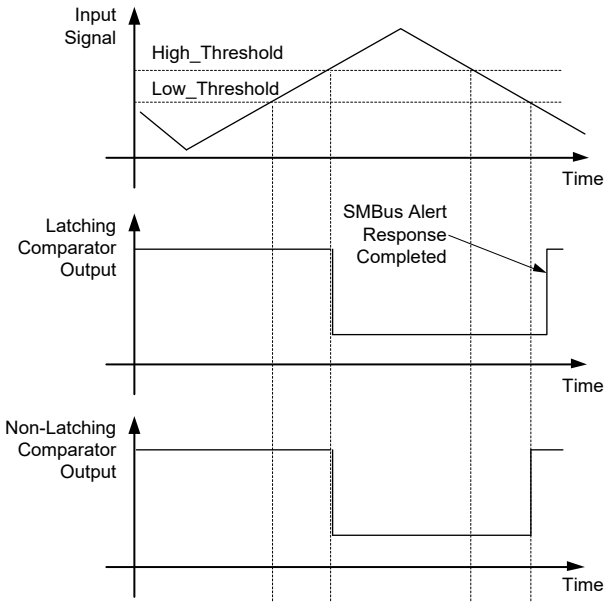



**Figure 8. Alert Pin Timing Diagram when Configured as A Traditional Comparator**

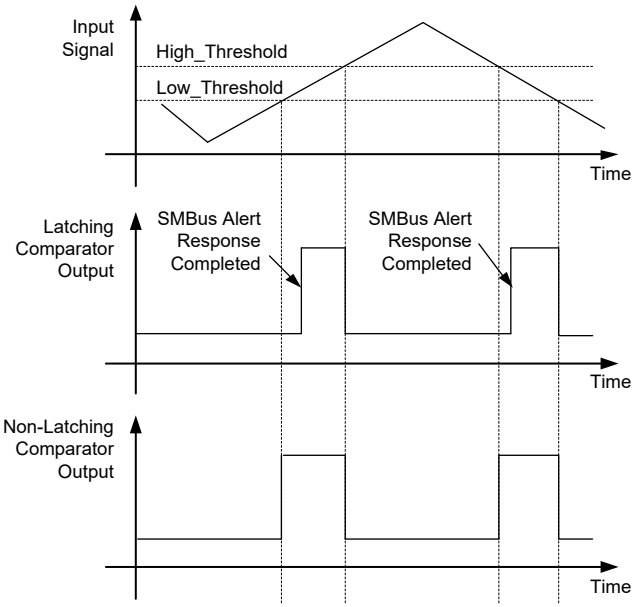



**Figure 9. Alert Pin Timing Diagram when Configured as A Window Comparator**

# DETAILED DESCRIPTION (continued)

## ADC Noise

**Table 6. ADC Noise with Internal Reference (RMS in μV)**

| DR / FS | 800 | 400 | 200 | 100 | 50 | 25 | 12.5 | 6.25 |
|---|---|---|---|---|---|---|---|---|
| 6.144 | 60.7 | 38.9 | 27.4 | 21.0 | 15.2 | 10.7 | 7.8 | 5.4 |
| 4.096 | 40.8 | 26.3 | 18.4 | 13.9 | 10.3 | 7.4 | 5.3 | 3.8 |
| 2.048 | 20.8 | 13.5 | 9.8 | 7.2 | 5.2 | 3.7 | 2.8 | 1.9 |
| 1.024 | 10.6 | 6.9 | 4.9 | 3.8 | 2.6 | 1.9 | 1.4 | 1.0 |
| 0.512 | 6.8 | 4.6 | 3.2 | 2.4 | 1.7 | 1.2 | 0.9 | 0.6 |
| 0.256 | 5.1 | 3.4 | 2.5 | 1.8 | 1.3 | 0.9 | 0.7 | 0.5 |

**Table 7. ADC ENOB (ENOB = (20log (FS/Noise_RMS) - 1.76)/6.02)**

| DR / FS | 800 | 400 | 200 | 100 | 50 | 25 | 12.5 | 6.25 |
|---|---|---|---|---|---|---|---|---|
| 6.144 | 17.3 | 17.9 | 18.5 | 18.9 | 19.3 | 19.8 | 20.3 | 20.8 |
| 4.096 | 17.3 | 17.9 | 18.5 | 18.9 | 19.3 | 19.8 | 20.3 | 20.8 |
| 2.048 | 17.3 | 17.9 | 18.4 | 18.8 | 19.3 | 19.8 | 20.2 | 20.7 |
| 1.024 | 17.3 | 17.9 | 18.4 | 18.8 | 19.3 | 19.7 | 20.2 | 20.7 |
| 0.512 | 16.9 | 17.4 | 18.0 | 18.4 | 18.9 | 19.3 | 19.9 | 20.4 |
| 0.256 | 16.3 | 16.9 | 17.4 | 17.8 | 18.3 | 18.8 | 19.2 | 19.7 |

## Conversion Ready Pin

If ALERT/RDY pin is used as a conversion ready pin, we need the following operations, firstly set the MSB (Most Significant Bit) of the high threshold register to '1', secondly set the MSB of the low threshold register to '0', and select COMP_QUE[1:0] in '00' mode. It should be noted that COMP_QUE[1:0] can disable this pin function. COMP_MODE and COMP_LAT have no affection on this function.

The ALERT/RDY pin is an open-drain output, it needs a pull-up resistor outside.

When the SGM58200 works in continuous mode, the ALERT/RDY pin gives a pulse (~8μs) at the end of every conversion completion.

When the SGM58200 works in single-shot mode, the ALERT/RDY pin goes low (COMP_POL is set to '0') when the conversion data is ready, and keeps low until the next conversion starts. Please see demos in Figure 10 and Figure 11.

## Digital Filter

The devices offer digital filter for filtering the digital data stream coming from the sigma-delta modulator. The implementation of the digital filter is determined by the ADC data rate setting. When data rate is configured as 120, 100, 60, 50, 30, 25, 15, 12.5, 7.5 and 6.25, the device uses a third-order Sinc filter ($Sinc^3$). When data rate is configured as 200, 240, 400, 480, 800 and 960, the device uses a fourth-order Sinc filter ($Sinc^4$).

When ALERT/RDY is used as the conversion completed indication pin, its default logic state is high (pulled up by the external resistor) during the conversion. When the device works in continuous mode, the ALERT/RDY pin will go low and remain low for about 8μs, generating an 8μs logic low pulse at the end of each conversion cycle. When the device works in single-shot mode and the $Sinc^3$ filter is used, the ALERT/RDY pin will go logic low after the third data conversion is finished and remain low until the device begins the next new conversion (OS bit is set to '1' again), and the ALERT/RDY pin goes logic high again during the new conversion. When the device works in single-shot mode and the $Sinc^4$ filter is used, the ALERT/RDY pin will go low after the fourth data conversion is finished and remain low until the device begins the next new conversion (OS bit is set to '1' again), and the ALERT/RDY pin goes logic high again during the new conversion. Please see ALERT/RDY examples in Figure 10 and Figure 11.

# DETAILED DESCRIPTION (continued)

## SMBus Alert Response

The ALERT/RDY pin can output as an SMBus alert. When it's in latch mode, COMP_LAT is set to '1'. If an ADC result is above the upper threshold or below the lower threshold, this pin is set (active low or active high). And the pin output is latched, it can be cleared by reading ADC conversion data, or by issuing an SMBus alert response (reading the alerting device $I^2C$ address).

The ALERT/RDY pin is an open-drain output, it needs a pull-up resistor.

If an alert is output at the ALERT/RDY pin and latched, the master controller accepts the alert, it sent an SMBus alert command (0b00011001) to $I^2C$ bus. Any SGM58200 on the bus will response with their own address, the lowest $I^2C$ address chip will occupy the bus and it will clear itself ALERT/RDY pin, the chip which loses $I^2C$ bus will keep alert on ALERT/RDY pin. The master will repeat SMBus alert command until all salve chips clear their alert.

In a multiple $I^2C$ devices system, two scenarios about clearing an alert on ALERT/RDY pin need to be noted. The first scenario is, when clearing an alert on ALERT/RDY pin of SGM58200 by sending a SMBus alert command (0x19), it must be committed that there is only one SGM58200 device in the system, meanwhile make sure that SGM58200 keeps the lowest address. Another scenario is, when clearing an alert on ALERT/RDY pin of SGM58200 by reading data register (0x00) of SGM58200, it needs to be committed that there are multiple SGM58200 chips in the system (SGM58200s' data registers need to be read one by one) or only one SGM58200 chip in the system.

When ALERT/RDY pin is configured as window comparator mode, if ADC result is higher than upper threshold or ADC result is below the lower threshold, the pin is set (active low or active high).

Timing diagram for SMBus alert response is shown in Figure 12.

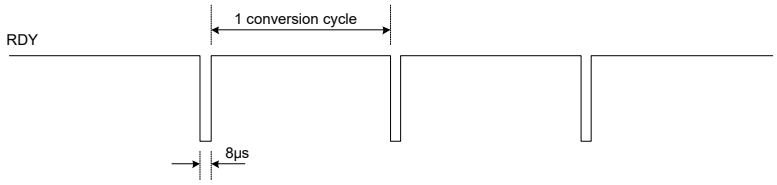



**Figure 10. RDY in Continuous Mode**

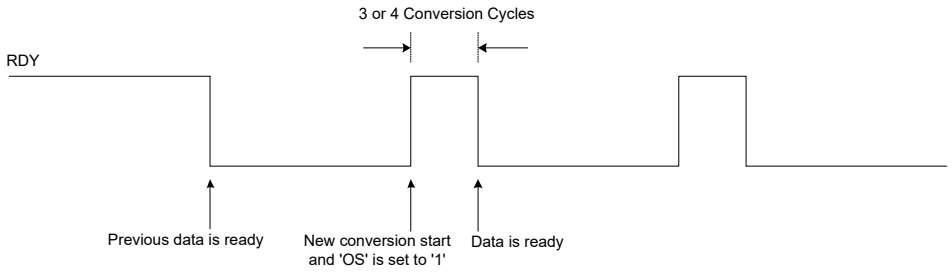
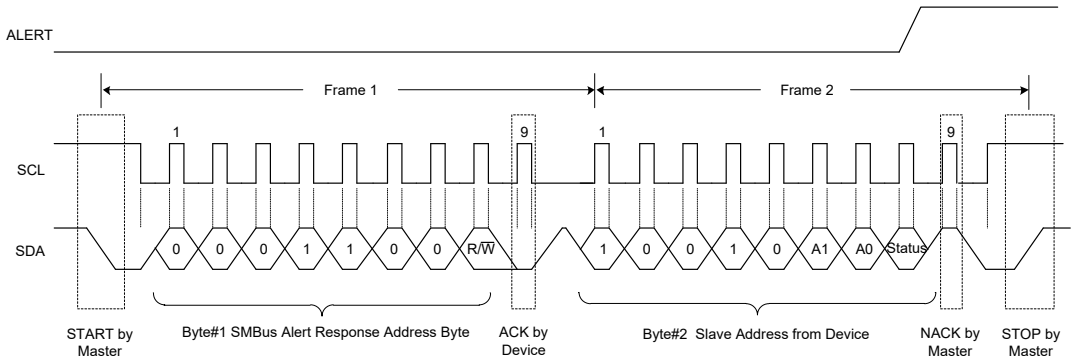



**Figure 11. RDY in Single-Shot Mode**




NOTE: 1. The A0 and A1 values depend on the ADDR pin.

**Figure 12. Timing Diagram for SMBus Alert Response**

# DETAILED DESCRIPTION (continued)

## I²C Interface

The SGM58200 communication interface is an I²C interface. The SGM58200 can only act as slave devices. An I²C timing diagram is shown in Figure 1.

## I²C Address Selection

The SGM58200 has a separate address setting pin ADDR, which can be connected to GND, $V_{DD}$, SDA and SCL. Table 8 shows the four available addresses.

**Table 8. ADDR Pin Connection and Corresponding Slave Address**

| ADDR Pin | Slave Address |
|---|---|
| GND | 1001000 |
| $V_{DD}$ | 1001001 |
| SDA | 1001010 |
| SCL | 1001011 |

## I²C General Call

The SGM58200 supports I²C general call address (0000000) and the eighth bit must be '0'. The device acknowledges the general call address. And if the second byte is 00000110 (06h), the SGM58200 resets all registers and goes to power-down.

## I²C Speed Modes

The I²C bus operation supports three speed modes: Standard mode, fast mode, and high-speed mode. See more details in Electrical Characteristics section.

To enter standard and fast mode, it needs no special operation.

To enter high-speed mode, send a special address byte of 00001XXX following the I²C start condition. The SGM58200 doesn't give an ACK (acknowledge) to this byte, the SGM58200 switches to high-speed mode after receiving this byte. The SGM58200 quits high-speed mode with the next STOP condition.

## Slave Mode Operations

The SGM58200 works in slave mode and doesn't drive the SCL line.

# REGISTER MAPS

## Register Address

The SGM58200 has seven pointer registers. Table 9 and Table 10 shows these register maps. Figure 4 shows how to access this pointer registers.

**Table 9. Register Address**

| Address | Register |
|---|---|
| 0x0 | Conversion Register |
| 0x1 | Config Register |
| 0x2 | Low_Thresh Register |
| 0x3 | High_Thresh Register |
| 0x4 | Config1 Register |
| 0x5 | Chip_ID Register |
| 0x6 | GN_Trim1 Register for EXT_REF |

## Pointer Register

**Table 10. Pointer Register Byte (Write-Only)**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | Register Address | | |

## Conversion Register

The ADC conversion result is 24-bit two's complement format. Table 11 shows the data format. Its reset default value is '0'.

**Table 11. 24-Bit Conversion Register (Read-Only)**

| MSB | | | | | | | | | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

NOTE: Default Value = 000000h.

# REGISTER MAPS (continued)

## Config Register

The configuration register (Config Register) is shown in Table 12.

**Table 12. Config Register Details (Read/Write)**

| BITS | NAME | DESCRIPTION | COMMENT | DEFAULT VALUE |
|---|---|---|---|---|
| D[15] | OS | Working Status/Single-Shot Conversion Start<br>For a write status:<br>0 = No effect<br>1 = Start a single conversion (when in single-shot mode)<br><br>For a read status:<br>0 = The chip is doing a conversion<br>1 = The chip isn't doing a conversion | This bit reports the status of the chip.<br>This bit can only be written when the chip is in power-down. | |
| D[14:12] | MUX[2:0] | Input Multiplexer (MUX) Configuration<br>000 = $AIN_P$ = AIN0 and $AIN_N$ = AIN1 (default)<br>001 = $AIN_P$ = AIN0 and $AIN_N$ = AIN3<br>010 = $AIN_P$ = AIN1 and $AIN_N$ = AIN3<br>011 = $AIN_P$ = AIN2 and $AIN_N$ = AIN3<br>100 = $AIN_P$ = AIN0 and $AIN_N$ = GND<br>101 = $AIN_P$ = AIN1 and $AIN_N$ = GND<br>110 = $AIN_P$ = AIN2 and $AIN_N$ = GND<br>111 = $AIN_P$ = AIN3 and $AIN_N$ = GND | | 000 |
| D[11:9] | PGA[2:0] | Programmable Gain Amplifier (PGA) Configuration<br>000 = FS = ±6.144V (1)<br>001 = FS = ±4.096V (1)<br>010 = FS = ±2.048V (default)<br>011 = FS = ±1.024V<br>100 = FS = ±0.512V<br>101 = FS = ±0.256V<br>110 = FS = ±0.256V<br>111 = FS = ±0.256V | | 010 |
| D[8] | MODE | Device Operating Mode<br>0 = Continuous conversion mode<br>1 = Power-down single-shot mode (default) | | 1 |
| D[7:5] | DR[2:0] | Data Rate | These bits control the data rate setting.<br>See Table 5. | 100 |
| D[4] | COMP_MODE | Comparator Mode<br>0 = A traditional comparator with hysteresis (default)<br>1 = A window comparator | | 0 |
| D[3] | COMP_POL | Comparator Polarity<br>0 = Active low (default)<br>1 = Active high | This bit sets the active polarity of the ALERT/RDY pin. | 0 |
| D[2] | COMP_LAT | Latching Comparator<br>0 = Non-latching comparator (default)<br>1 = Latching comparator | This bit sets whether the ALERT/RDY pin latches once its outputs sets or resets when ADC conversion result is within the upper and lower threshold limitations. | 0 |
| D[1:0] | COMP_QUE[1:0] | Comparator Queue and Disable Function<br>00 = Assert after one conversion<br>01 = Assert after two conversions<br>10 = Assert after four conversions<br>11 = Disable comparator (default) | These bits can disable the comparator.<br>These bits can set the required times of successive ADC conversion beyond the threshold before an alert output on ALERT/RDY pin. | 11 |

NOTES:

1. Default Value = 8583h.
2. This is a theoretical full-scale range of the ADC scaling. The real input must be within the electrical limitation (0V ~ $V_{DD}$ + 0.3V).

# REGISTER MAPS (continued)

## Low_Thresh and High_Thresh Registers

The lower (Low_Thresh) and upper (High_Thresh) threshold registers are in 16-bit two's complement format, and aligned to conversion data D[23:8]. Table 13 shows these two register format.

**Table 13. Low_Thresh and High_Thresh Registers (Read/Write)**

| Low_Thresh Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 15** | **Bit 14** | **Bit 13** | **Bit 12** | **Bit 11** | **Bit 10** | **Bit 9** | **Bit 8** |
| Low_Thresh[15:8] | | | | | | | |
| **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| Low_Thresh[7:0] | | | | | | | |
| | | | | | | | |
| **High_Thresh Register** | | | | | | | |
| **Bit 15** | **Bit 14** | **Bit 13** | **Bit 12** | **Bit 11** | **Bit 10** | **Bit 9** | **Bit 8** |
| High_Thresh[15:8] | | | | | | | |
| **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| High_Thresh[7:0] | | | | | | | |

NOTE: Low_Thresh Default Value = 8000h, High_Thresh Default Value = 7FFFh.

## Config1 Register

**Table 14. 16-Bit Config1 Register Details**

| BITS | NAME | DESCRIPTION | COMMENT | DEFAULT VALUE |
|---|---|---|---|---|
| D[15:9] | N/A | | | |
| D[8] | PD | Writing '1' to PD powers down this part, and this PD bit is automatically cleared internally. Another continuous/single conversion can be carried out again without the need to clear this bit. | | 0 |
| D[7] | DR_SEL | 0 = DR[2:0] = 000 ~ 111 for conversion rate of 6.25Hz, 12.5Hz, 25Hz, 50Hz, 100Hz, 200Hz, 400Hz and 800Hz (default)<br>1 = DR[2:0] = 000 ~ 111 for conversion rate of 7.5Hz, 15Hz, 30Hz, 60Hz, 120Hz, 240Hz, 480Hz and 960Hz | | 0 |
| D[6] | BURNOUT | 0 = No current sourced (default)<br>1 = Source a pair of 2μA current to selected pair of AINs | | 0 |
| D[5] | Reserved | | | 0 |
| D[4] | BUS_FLEX | 0 = Disable leakage blocking circuit for the scenario that $I^2C$ bus voltage is lower than $V_{DD}$ of the part. The $I^2C$ interface is still functional but $V_{DD}$ sees leakage when $V_{BUS} < V_{DD}$ - 0.3V (default)<br>1 = Bus voltage can be lower than $V_{DD}$ without causing leakage. The $V_{DD}$ range is 3V to 5.5V and the $I^2C$ bus voltage should be limited to 3V to 5.5V | | 0 |
| D[3] | EXT_REF | 0 = None (default)<br>1 = Use AIN3 as external reference for ADC | | 0 |
| D[2:0] | N/A | | | |

# REGISTER MAPS (continued)

## Chip_ID Register

**Table 15. 16-Bit Chip_ID Register for Identifying Chip ID and Its Subversions (Read-Only)**

| Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | ID[4:0] | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| VER[2:0] | | | N/A | N/A | N/A | N/A | N/A |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## GN_Trim1 Register (When Using EXT_REF)

ADC gain coefficient for user selecting Config1 register EXT_REF bit as reference. We provide a default value and user is responsible for writing proper value to the register if they want to compensate external reference error. This register does not take effect when EXT_REF = 0 and internal reference is selected.

**Table 16. GN_Trim1 Format**

| Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 |
|---|---|---|---|---|---|---|---|
| N/A | N/A | N/A | N/A | N/A | GN10 | GN9 | GN8 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| GN7 | GN6 | GN5 | GN4 | GN3 | GN2 | GN1 | GN0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |

ADC GN_Trim1 register is an unsigned value. Default value used for final trimming is 1.3333 to compensate default ADC gain of 3/4. The value of GN[10:0] adds a constant to get the final gain trimming value.

GN_Trim1 + CONST = GN_Trim. The binary value of CONST is 1010011010110000, corresponding to a gain factor of 1.30225. After adding the default value of GN_Trim1 register (01111111010), the final default gain trimming value is 1.3333. The MAX final gain trimming value is 1.3547 when trimming register is all '1'; MIN value is 1.30225 when register is all '0'. This gives GN trimming a ±3% range and 32ppmFS step.

# REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| MAY 2023 – REV.A.2 to REV.A.3 | Page |
|---|---|
| Updated Detailed Description section | 15 |

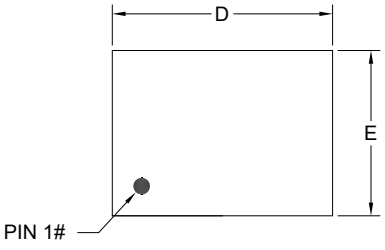
| JUNE 2022 – REV.A.1 to REV.A.2 | Page |
|---|---|
| Updated Detailed Description section | 14 |

| APRIL 2022 – REV.A to REV.A.1 | Page |
|---|---|
| Added UTQFN-2×1.5-10L package | All |

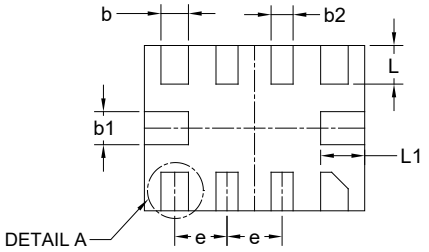
| Changes from Original to REV.A (OCTOBER 2020) | Page |
|---|---|
| Changed from product preview to production data | All |

# PACKAGE OUTLINE DIMENSIONS

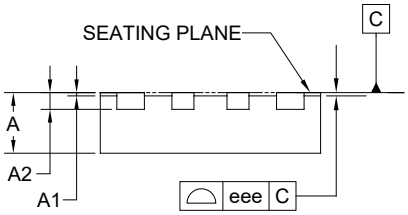
## UTQFN-2×1.5-10L



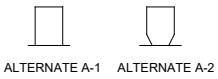

**TOP VIEW**



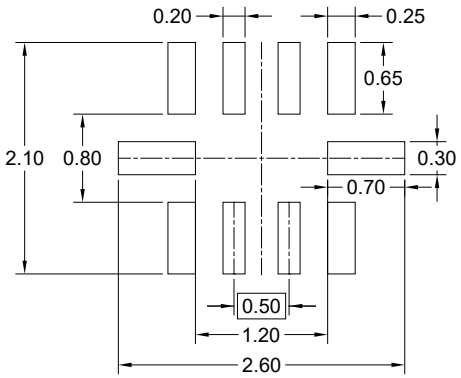

**BOTTOM VIEW**




**SIDE VIEW**




**DETAIL A**
ALTERNATE TERMINAL CONSTRUCTION



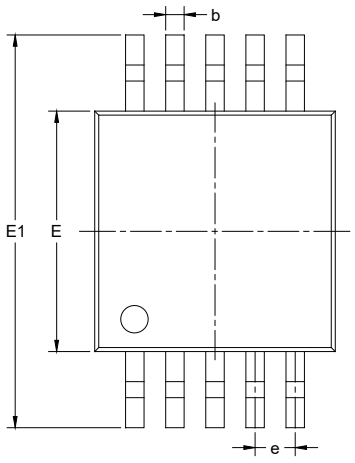

**RECOMMENDED LAND PATTERN** (Unit: mm)

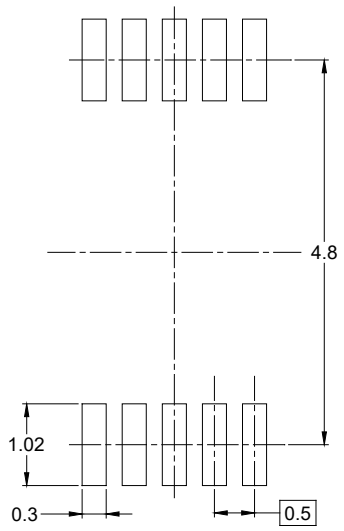
| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.500 | 0.550 | 0.600 |
| A1 | 0.000 | - | 0.050 |
| A2 | 0.152 REF | | |
| b | 0.200 | 0.250 | 0.300 |
| b1 | 0.250 | 0.300 | 0.350 |
| b2 | 0.150 | 0.200 | 0.250 |
| D | 1.900 | 2.000 | 2.100 |
| E | 1.400 | 1.500 | 1.600 |
| L | 0.250 | 0.350 | 0.450 |
| L1 | 0.300 | 0.400 | 0.500 |
| e | 0.500 BSC | | |
| eee | 0.050 | | |

NOTE: This drawing is subject to change without notice.

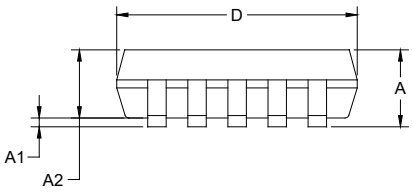
# PACKAGE OUTLINE DIMENSIONS

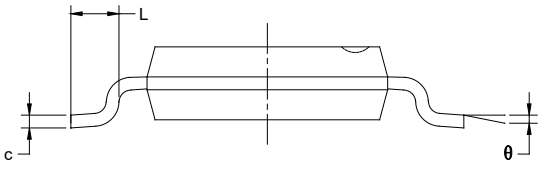
## MSOP-10




**RECOMMENDED LAND PATTERN** (Unit: mm)



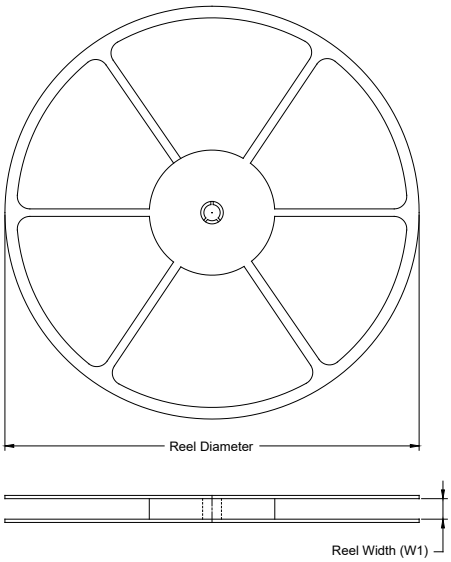




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.820 | 1.100 | 0.032 | 0.043 |
| A1 | 0.020 | 0.150 | 0.001 | 0.006 |
| A2 | 0.750 | 0.950 | 0.030 | 0.037 |
| b | 0.180 | 0.280 | 0.007 | 0.011 |
| c | 0.090 | 0.230 | 0.004 | 0.009 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E1 | 4.750 | 5.050 | 0.187 | 0.199 |
| e | 0.500 BSC | | 0.020 BSC | |
| L | 0.400 | 0.800 | 0.016 | 0.031 |
| θ | 0° | 6° | 0° | 6° |

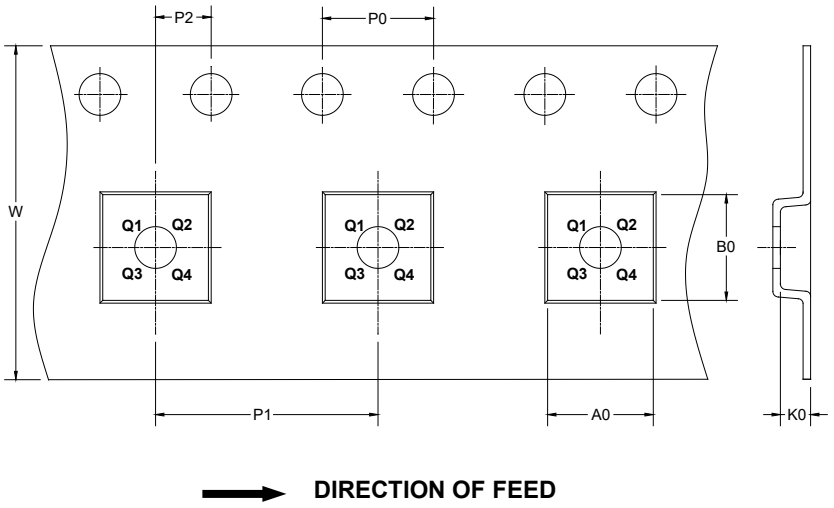
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

## REEL DIMENSIONS




## TAPE DIMENSIONS



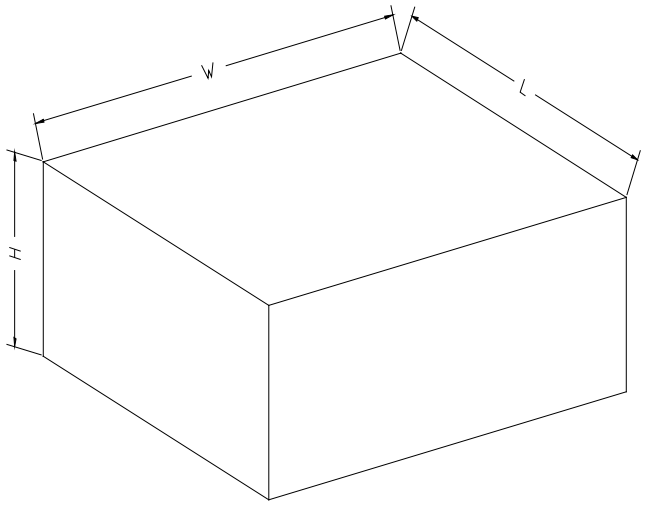

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| UTQFN-2×1.5-10L | 7″ | 9.5 | 1.70 | 2.30 | 0.75 | 4.0 | 4.0 | 2.0 | 8.0 | Q1 |
| MSOP-10 | 13″ | 12.4 | 5.20 | 3.30 | 1.50 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |

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## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 7″ (Option) | 368 | 227 | 224 | 8 |
| 7″ | 442 | 410 | 224 | 18 |
| 13″ | 386 | 280 | 370 | 5 |

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