SGM41611
I²C Controlled High Voltage 4:1 14A Switched-Capacitor Charger

GENERAL DESCRIPTION

The SGM41611 is an efficient 14A switched-capacitor battery charging device with I²C control that can be configured to 6 different operation modes: forward 4:1/2:1/1:1 step-down charging modes and reverse 1:4/1:2/1:1 step-up discharging modes. It can charge single-cell Li-Ion or Li-polymer battery in a wide 3.4V to 21V input voltage range (VBUS) from smart wall adapters or wireless charger. The switched-capacitor architecture is optimized for 50% duty cycle to cut the input current to one-quarter of the battery current and reduce the wiring drops, losses and temperature rise in the application.

A two-channel switched-capacitor topology is used to reduce the required input capacitors and minimize the output ripple. It supports dual input configuration through integrated MUX control and driver for external OVPFETs. It also allows single input with no external OVPFET or single OVPFET.

The SGM41611 is available in a Green WLCSP-4.88× 3.6-108B package.

APPLICATIONS

Smart Phone, Tablet PC

FEATURES

- **6 Different Operation Modes**
  - **Forward 4:1/2:1/1:1 Step-down Charging Modes**
  - **Reverse 1:4/1:2/1:1 Step-up Discharging Modes**
- **Efficiency Optimized Switched-Capacitor Architecture**
  - **Up to 14A Output Current**
  - **3.4V to 21V Input Voltage Range**
  - **400kHz to 1.5MHz Switching Frequency Setting**
  - **Above 96.8% Forward 4:1 Step-down Mode Efficiency (when V_{BAT} = 5V, I_{BAT} = 8A, f_{SW} = 400kHz)**
- **Comprehensive Integrated Protection Feature**
  - **External VUSB/VWPC OVP Control**
  - **Input Over-Voltage Protection (VBUS_OVP)**
  - **Input Under-Voltage Protection (VBUS_UVP)**
  - **Input Over-Current Protection (IBUS_OCP)**
  - **Input Under-Current Protection (IBUS_UCP)**
  - **Input Reverse-Current Protection (IBUS_RCP)**
  - **Output Over-Voltage Protection (VOUT_OVP)**
  - **Battery Over-Voltage Protection (VBAT_OVP)**
  - **IBAT Over-Current Protection (IBAT_OCP)**
  - **C_{FLY} Diagnosis (CFLY_DIAG)**
  - **Switch Peak Over-Current Protection (PEAK_OCP)**
  - **Die Over-Temperature Protection (TDIE_OTP)**
- **9-Channel 12-Bit (Effective) ADC Converter**
  - **VUSB, VWPC, VBUS, IBUS, VOUT, VBAT1, VBAT2, IBAT, TDIE for Monitoring**

TYPICAL APPLICATION

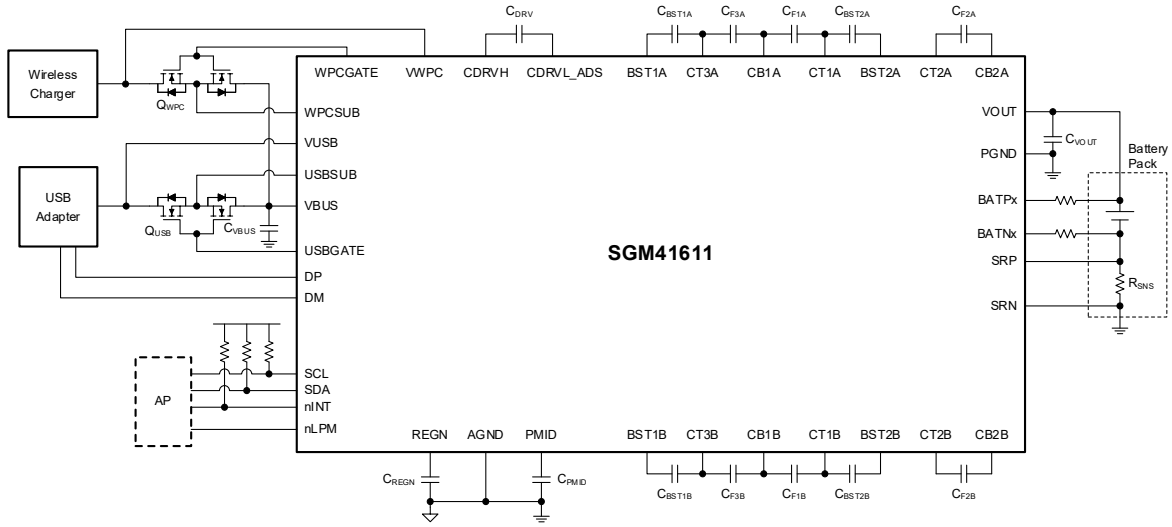


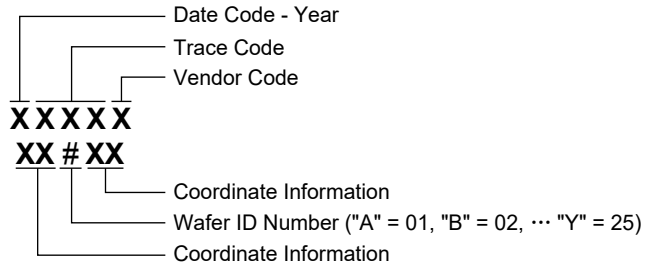
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41611	WLCSP-4.88×3.6-108B	-40℃ to +85℃	SGM41611YG/TR	0FY XXXXX XX#XX	Tape and Reel, 1500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VUSB, VWPC (Converter Not Switching) ..... -0.3V to 35V
USBGATE, WPCGATE..... -0.3V to 33V
USBGATE to USBSUB, WPCGATE to WPCSUB ..... -0.3V to 12V
USBGATE/WPCGATE to VBUS..... -27V to 12V
USBSUB, WPCSUB, VBUS, PMID (Converter Not Switching) ..... -0.3V to 27V
BST1A to CT3A, BST2A to CT1A, BST1B to CT3B, BST2B to CT1B, CDRVH to VOUT ..... -0.3V to 6V
PMID to VBUS ..... -0.3V to 6V
PMID to CT3A/CT3B ..... -0.3V to 24V
CT3A to CT2A, CT3B to CT2B ..... -0.3V to 18V
CT2A to CT1A, CT2B to CT1B ..... -0.3V to 12V
CT1A to VOUT, CT1B to VOUT..... -0.3V to 6V
VOUT, CB1A, CB1B, CB2A, CB2B ..... -0.3V to 6V
SCL, SDA, nINT, nLPM, CDRVL_ADS, REGN, BATP1, BATP2, BATN1, BATN2, SRP, SRN, DP, DM..... -0.3V to 6V
SRP to SRN..... -0.5V to 0.5V
Package Thermal Resistance
WLCSP-4.88×3.6-108B, θ_{JA}..... 20.7℃/W
WLCSP-4.88×3.6-108B, θ_{JB}..... 1.9℃/W
WLCSP-4.88×3.6-108B, θ_{JC}..... 6.3℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (1) (2)
HBM.....±3000V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

VUSB, VWPC.....3.4V to 21V
VBUS (4:1 Mode) .....12V to 21V
VBUS (2:1 Mode) .....6V to 11V
VBUS (Forward 1:1 Mode).....3.4V to 5.5V
VOUT, BATP1, BATP2.....3V to 5.5V
(SRP - SRN).....-0.05V to 0.05V
Junction Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

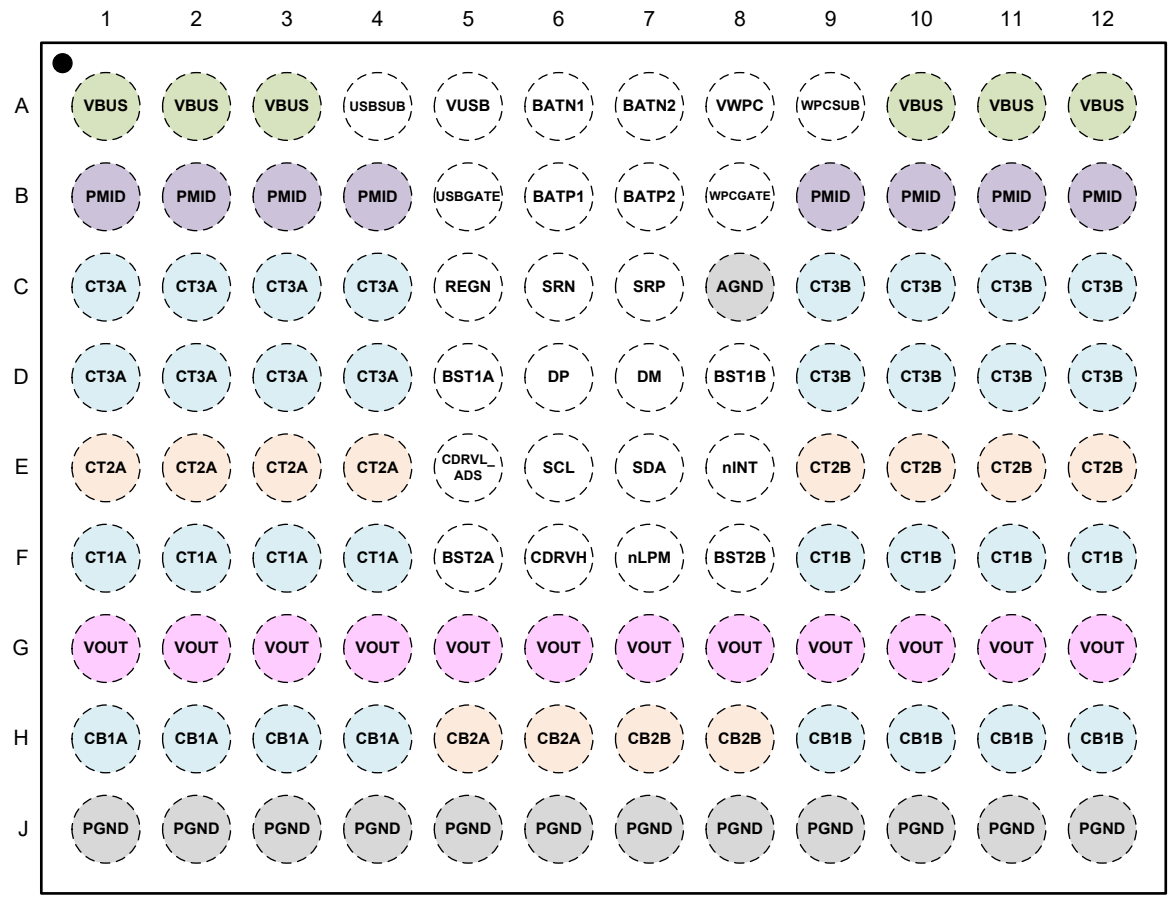
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-4.88×3.6-108B

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
A1, A2, A3, A10, A11, A12	VBUS	P	Device Power Input Pins. Use two 1μF or larger ceramic capacitors between VBUS and PGND pins close to the device.
A4	USBSUB	AI	External Back-to-Back N-MOSFET Common Source Input Pin. Leave it floating if USB charging function is not used.
A5	VUSB	AI	USB Charging DC Voltage Sense Input Pin. Connect it to the drain of the external N-MOSFET, or leave it floating if USBGATE control function is not used.
A6	BATN1	AI	Battery1 Voltage Sensing Negative Input. Connect a 100Ω resistor between BATN1 and negative terminal of the battery pack, or connect it to ground if V_{BAT1} sensing is not used.
A7	BATN2	AI	Battery2 Voltage Sensing Negative Input. Connect a 100Ω resistor between BATN2 and negative terminal of the battery pack, or connect it to ground if V_{BAT2} sensing is not used.
A8	VWPC	AI	Wireless Charging DC Voltage Sense Input Pin. Connect it to the drain of the external N-MOSFET, or leave it floating if wireless charging function is not used.
A9	WPCSUB	AI	External Back-to-Back N-MOSFET Common Source Input Pin. Leave it floating if wireless charging function is not used.
B1, B2, B3, B4, B9, B10, B11, B12	PMID	P	Power Stage Supply Input Pins. Bypass them with at least two 4.7μF ceramic capacitor to PGND.
B5	USBGATE	AO	External Dual N-MOSFET Gate Control Pin. Connect it to the gate of the external back-to-back N-MOSFET in the USB charging path, or leave it floating if USBGATE control function is not used.
B6	BATP1	AI	Battery1 Voltage Sensing Positive Input. Connect a 100Ω resistor between BATP1 and positive terminal of the battery pack, or connect it to ground if V_{BAT1} sensing is not used.
B7	BATP2	AI	Battery2 Voltage Sensing Positive Input. Connect a 100Ω resistor between BATP2 and positive terminal of the battery pack, or connect it to ground if V_{BAT2} sensing is not used.
B8	WPCGATE	AO	External Dual N-MOSFET Gate Control Pin. Connect it to the gate of the external back-to-back N-MOSFET in the wireless charging path, or leave it floating if wireless charging function is not used.
C1, C2, C3, C4, D1, D2, D3, D4	CT3A	P	Channel-A Flying Capacitor C_{F3A} Top Plate Pins. Connect two 22μF or larger parallel capacitors between CT3A and CB1A pins as close as possible to the device.
C5	REGN	AO	Internal 5V LDO Output. Connect a 4.7μF MLCC capacitor between this pin and AGND.
C6	SRN	AI	High-side or Low-side Battery Current Sensing Negative Input. Place a 1mΩ or 2mΩ (R_{SNS}) shunt resistor between SRP and SRN pins. Short SRP and SRN together if not used.
C7	SRP	AI	High-side or Low-side Battery Current Sensing Positive Input. Place a 1mΩ or 2mΩ (R_{SNS}) shunt resistor between SRP and SRN pins. Short SRP and SRN together if not used.
C8	AGND	P	Analog Ground Pin (reference for low current signals).
C9, C10, C11, C12, D9, D10, D11, D12	CT3B	P	Channel-B Flying Capacitor C_{F3B} Top Plate Pins. Connect two 22μF or larger parallel capacitors between CT3B and CB1B pins as close as possible to the device.
D5	BST1A	P	Channel-A Bootstrap Pin. It is the BST pin to supply Q_{8A} gate driver. Use a 0.1μF or larger MLCC capacitor from this pin to CT3A pin.
D6	DP	AIO	USB Communication Interface Positive Line. Connect it to the USB D+ data line.
D7	DM	AIO	USB Communication Interface Negative Line. Connect it to the USB D- data line.
D8	BST1B	P	Channel-B Bootstrap Pin. It is the BST pin to supply Q_{8B} gate driver. Use a 0.1μF or larger MLCC capacitor from this pin to CT3B pin.
E1, E2, E3, E4	CT2A	P	Channel-A Flying Capacitor C_{F2A} Top Plate Pins. Connect two 22μF or larger parallel capacitors between CT2A and CB2A pins as close as possible to the device.
E5	CDRVL_ADS	AIO	Charge Pump for Gate Drive. Connect a 0.22μF MLCC capacitor between CDRVH and CDRVL_ADS. During POR, this pin is also used to assign the I²C address of the device. Pull CDRVL_ADS low by a 75kΩ resistor to AGND to select address 0x67. Pull CDRVL_ADS low by a 249kΩ resistor to AGND or leave it floating to select address 0x68.
E6	SCL	DI	I²C Interface Clock Input Line. The device I²C controller block is forced to reset when receiving 9 clock pulses on the SCL line.
E7	SDA	DIO	I²C Interface Data Line. The SDA line is forced to release when the I²C timeout fault occurs.
E8	nINT	DO	Open-Drain Interrupt Output Pin. Use a pull-up 10kΩ to the logic high rail. The nINT pin is active low and sends a negative 256μs pulse to inform the AP about a new charger status update or a fault.
E9, E10, E11, E12	CT2B	P	Channel-B Flying Capacitor C_{F2B} Top Plate Pins. Connect two 22μF or larger parallel capacitors between CT2B and CB2B pins as close as possible to the device.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE (1)	FUNCTION
F1, F2, F3, F4	CT1A	P	Channel-A Flying Capacitor C_{F1A} Top Plate Pins. Connect two 22μF or larger parallel capacitors between CT1A and CB1A pins as close as possible to the device.
F5	BST2A	P	Channel-A Bootstrap Pin. It is the BST pin to supply Q_{6A} gate driver. Use a 0.1μF or larger MLCC capacitor from this pin to CT1A pin.
F6	CDRVH	AIO	Charge Pump for Gate Drive. Connect a 0.22μF MLCC capacitor between CDRVH and CDRVL_ADS.
F7	nLPM	AI	Low Power Mode Enable Input Pin with an Internal 1.3MΩ Pull-Down Resistor. If battery only, the logic low enables the low power mode with low quiescent current, and the I²C bus does not need to respond. When the VUSB or VWPC is inserted, the state of nLPM pin is ignored and the device exits low power mode. A rising edge on nLPM pin while keeping high for more than 10μs triggers a hard reset of the device. Except for the specified bits, all other register bits are reset to their default values if a hard reset is triggered.
F8	BST2B	P	Channel-B Bootstrap Pin. It is the BST pin to supply Q_{6B} gate driver. Use a 0.1μF or larger MLCC capacitor from this pin to CT1B pin.
F9, F10, F11, F12	CT1B	P	Channel-B Flying Capacitor C_{F1B} Top Plate Pins. Connect two 22μF or larger parallel capacitors between CT1B and CB1B pins as close as possible to the device.
G1, G2, G3, G4, G5, G6, G7, G8, G9, G10, G11, G12	VOUT	P	Output Pins. Connect it to the battery pack positive terminal. Two 10μF capacitors between VOUT and PGND pins are recommended.
H1, H2, H3, H4	CB1A	P	Channel-A Flying Capacitor C_{F1A} and C_{F3A} Bottom Plate Pins. Connect two 22μF or larger parallel capacitors between CT1A and CB1A pins as close as possible to the device, and also connect two 22μF or larger parallel capacitors between CT3A and CB1A pins as close as possible to the device.
H5, H6	CB2A	P	Channel-A Flying Capacitor C_{F2A} Bottom Plate Pins. Connect two 22μF or larger parallel capacitors between CT2A and CB2A pins as close as possible to the device.
H7, H8	CB2B	P	Channel-B Flying Capacitor C_{F2B} Bottom Plate Pins. Connect two 22μF or larger parallel capacitors between CT2B and CB2B pins as close as possible to the device.
H9, H10, H11, H12	CB1B	P	Channel-B Flying Capacitor C_{F1B} and C_{F3B} Bottom Plate Pins. Connect two 22μF or larger parallel capacitors between CT1B and CB1B pins as close as possible to the device, and also connect two 22μF or larger parallel capacitors between CT3B and CB1B pins as close as possible to the device.
J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12	PGND	P	Power Ground Pin.

NOTE:

1. P = power, AI = analog input, AO = analog output, AIO = analog input/output, DI = digital input, DIO = digital input/output.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Currents						
VUSB Quiescent Current	I_{Q_VUSB}	ADC disabled, SCC disabled, Q_{USB} used with driver disabled (USBGATE_EN bit = 0), $V_{USB_OVP_R}$ = 23V (V_{USB}_OVP[2:0] bits = 111), V_{VUSB} = 21V, V_{VWPC} = 0V, V_{VBUS} = 0V, V_{VOUT} = 0V		0.2	0.4	mA
		ADC disabled, SCC disabled, Q_{USB} used with driver enabled (USBGATE_EN bit = 1, USBGATE_MODE bit = 0), $V_{USB_OVP_R}$ = 23V (V_{USB}_OVP[2:0] bits = 111), V_{VUSB} = 21V, V_{VWPC} = 0V, V_{VOUT} = 0V		0.7	1	mA
VWPC Quiescent Current	I_{Q_VWPC}	ADC disabled, SCC disabled, Q_{WPC} used with driver disabled (WPCGATE_EN bit = 0), $V_{WPC_OVP_R}$ = 23V (V_{WPC}_OVP[2:0] bits = 111), V_{VWPC} = 21V, V_{VUSB} = 0V, V_{VBUS} = 0V, V_{VOUT} = 0V		0.2	0.4	mA
		ADC disabled, SCC disabled, Q_{WPC} used with driver enabled (WPCGATE_EN bit = 1, WPCGATE_MODE bit = 0), $V_{WPC_OVP_R}$ = 23V (V_{WPC}_OVP[2:0] bits = 111), V_{VWPC} = 21V, V_{VUSB} = 0V, V_{VOUT} = 0V		0.7	1	mA
VBUS Quiescent Current	I_{Q_VBUS}	SCC enabled (SCC_MODE[2:0] = 010, SCC_EN bit = 1), Q_{USB} & Q_{WPC} used with both drivers disabled, no load, V_{VBUS} = 20V > (4 × V_{VOUT}), f_{SW} = 600kHz		22.9		mA
Battery Only Shutdown Current	I_{SHUT_VOUT}	ADC disabled, SCC disabled, nLPM pin = low, V_{VUSB} = 0V, V_{VWPC} = 0V, V_{VBUS} = 0V, V_{VOUT} = 4.5V		4.5	10	μA
Leakage Current at Pin BATP1, BATP2, BATN1, BATN2	I_{LKG_BAT}	V_{VOUT} < $V_{BAT_INSERT_F}$			1	μA
		ADC enabled			5	
VBAT Insert Rising Threshold	$V_{BAT_INSERT_R}$	VOUT pin, V_{VOUT} rising, for active I²C	2.65	2.8	2.95	V
VBAT Insert Falling Threshold	$V_{BAT_INSERT_F}$	VOUT pin, V_{VOUT} falling		2.7		V
VBAT Insert Hysteresis	$V_{BAT_INSERT_HYS}$			100		mV
External OVPFET Control						
VUSB Insert Rising Threshold	$V_{USB_INSERT_R}$	VUSB pin, V_{VUSB} rising, to turn on USBGATE	3.05	3.25	3.45	V
VUSB Insert Falling Threshold	$V_{USB_INSERT_F}$	VUSB pin, V_{VUSB} falling		3.15		V
VUSB Insert Hysteresis	$V_{USB_INSERT_HYS}$			100		mV
VUSB Insert Rising Threshold Deglitch Time	$t_{USBGATE_ON_DEG}$	Deglitch between V_{VUSB} rising above $V_{USB_INSERT_R}$ and sending an nINT pulse, then to start external Q_{USB} turn-on (USBGATE_EN bit = 1, USBGATE_MODE bit = 0) R_{PDN_VUSB} PoorSRC qualification during $t_{USBGATE_ON_DEG}$		256		ms
VUSB Insert Falling Threshold Deglitch Time	$t_{VUSB_OUT_DEG}$	Deglitch between V_{VUSB} falling below $V_{USB_INSERT_F}$ and sending an nINT pulse		20		ms
VWPC Insert Rising Threshold	$V_{WPC_INSERT_R}$	VWPC pin, V_{VWPC} rising, to turn on WPCGATE	3.05	3.25	3.45	V
VWPC Insert Falling Threshold	$V_{WPC_INSERT_F}$	VWPC pin, V_{VWPC} falling		3.15		V
VWPC Insert Hysteresis	$V_{WPC_INSERT_HYS}$			100		mV
VWPC Insert Rising Threshold Deglitch Time	$t_{WPCGATE_ON_DEG}$	Deglitch between V_{VWPC} rising above $V_{WPC_INSERT_R}$ and sending an nINT pulse, then to start external Q_{WPC} turn-on (WPCGATE_EN bit = 1, WPCGATE_MODE bit = 0) R_{PDN_VWPC} PoorSRC qualification during $t_{WPCGATE_ON_DEG}$		256		ms
VWPC Insert Falling Threshold Deglitch Time	$t_{VWPC_OUT_DEG}$	Deglitch between V_{VWPC} falling below $V_{WPC_INSERT_F}$ and sending an nINT pulse		20		ms
VUSB OVP Rising Threshold Range	$V_{USB_OVP_R}$	I²C programmable, 11V by default	7.5		23	V
VUSB OVP Threshold Accuracy	$V_{USB_OVPR_ACC}$	$V_{USB_OVP_R}$ = 11V	-3		3	%
VUSB OVP Threshold Hysteresis	$V_{USB_OVP_HYS}$	V_{VUSB} falling to turn on Q_{USB} again after VUSB OVP active		1.1		V

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VUSB OVP Rising Deglitch Time	$t_{VUSB_OVP_DEG}$	$V_{USB_OVP_R}$ = 22V, V_{VUSB} = 21V to 23V, by 10V/μs, deglitch between V_{VUSB} rising above $V_{USB_OVP_R}$ and triggering the protection action		200		ns
VUSB OVP Resume Time	$t_{VUSB_OVP_RSM}$	Deglitch between V_{VUSB} falling below $V_{USB_OVP_F}$ and enabling the AP to read to reset the flag bit		128		ms
VUSB2VOUT OVP Rising Threshold Range	$V_{USB2VOUT_OVP}$	Only for forward mode, I²C programmable, 100mV per step, 400mV by default	400		500	mV
VUSB2VOUT OVP Threshold Accuracy	$V_{USB2VOUT_OVP_ACC}$	$V_{USB2VOUT_OVP}$ = 400mV	-120		120	mV
VUSB OVP Alarm Rising Threshold Range	$V_{USBOVP_ALM_R}$	Only for forward mode, I²C programmable, 10V by default	6.5		22	V
VUSB OVP Alarm Threshold Accuracy	$V_{USBOVP_ALM_ACC}$	$V_{USBOVP_ALM_R}$ = 10V	-3		3	%
VUSB Pull-Down Resistor	R_{PDN_VUSB}	V_{VUSB} = 5V, VUSB_PDN_EN = 1		500	1000	Ω
VWPC OVP Rising Threshold Range	$V_{WPC_OVP_R}$	I²C programmable, 22V by default	7.5		23	V
VWPC OVP Threshold Accuracy	$V_{WPC_OVPR_ACC}$	$V_{WPC_OVP_R}$ = 22V	-3		3	%
VWPC OVP Threshold Hysteresis	$V_{WPC_OVP_HYS}$	V_{VWPC} falling to turn on Q_{WPC} again after VWPC OVP active		1.1		V
VWPC OVP Rising Deglitch Time	$t_{VWPC_OVP_DEG}$	$V_{WPC_OVP_R}$ = 22V, V_{VWPC} = 21V to 23V, by 10V/μs, deglitch between V_{VWPC} rising above $V_{WPC_OVP_R}$ and triggering the protection action		200		ns
VWPC OVP Resume Time	$t_{VWPC_OVP_RSM}$	Deglitch between V_{VWPC} falling below $V_{WPC_OVP_F}$ and enabling the AP to read to reset the flag bit		128		ms
VWPC2VOUT OVP Rising Threshold Range	$V_{WPC2VOUT_OVP}$	Only for forward mode, I²C programmable, 100mV per step, 400mV by default	400		500	mV
VWPC2VOUT OVP Threshold Accuracy	$V_{WPC2VOUT_OVP_ACC}$	$V_{WPC2VOUT_OVP}$ = 400mV	-120		120	mV
VWPC OVP Alarm Rising Threshold Range	$V_{WPCOVP_ALM_R}$	Only for forward mode, I²C programmable, 21V by default	6.5		22	V
VWPC OVP Alarm Threshold Accuracy	$V_{WPCOVP_ALM_ACC}$	$V_{WPCOVP_ALM_R}$ = 21V	-3		3	%
VWPC Pull-Down Resistor	R_{PDN_VWPC}	V_{VWPC} = 5V, VWPC_PDN_EN = 1		500	1000	Ω
VBUS Pull-Down Resistor	R_{PDN_VBUS}	VBUS and PMID pins, V_{VBUS} = 5V, VBUS_PDN_EN = 1		5.5		kΩ
REGN LDO						
REGN LDO Output Voltage	V_{REGN}	V_{VBUS} = 8V, I_{REGN} = 5mA	4.8	5	5.2	V
Switched-Cap Converter						
VBUS to VOUT Resistance	$R_{DROPOUT}$	Forward 1:1 mode		23		mΩ
VBUS Present Rising Threshold	$V_{BUS_PRESENT_R}$	V_{VBUS} rising, to enable charging	3.05	3.25	3.45	V
VBUS Present Falling Threshold	$V_{BUS_PRESENT_F}$	V_{VBUS} falling		3.15		V
VBUS Present Hysteresis	$V_{BUS_PRESENT_HYS}$			100		mV
VBAT Brown-In Threshold for Reverse Mode	$V_{BAT_BRN_IN}$	VOUT pin, V_{VOUT} rising, to enable reverse converter mode		3.25	3.4	V
VBAT Brown-Out Threshold for Reverse Mode	$V_{BAT_BRN_OUT}$	VOUT pin, V_{VOUT} falling	2.75	2.95	3.1	V
VBAT Brown-In/Out Threshold Hysteresis	$V_{BAT_BRN_HYS}$	VOUT pin		300		mV
VBAT Brown-Out Threshold Deglitch Time	$t_{VBAT_BRN_OUT_DEG}$	Deglitch between V_{VOUT} falling below $V_{BAT_BRN_OUT}$ and sending an nINT pulse		48		ms
Converter Switching Frequency Range	f_{SW}	I²C programmable, 600kHz by default	400		1500	kHz
Converter Switching Frequency Accuracy	f_{SW_ACC}	f_{SW} = 600kHz, T_J = +25℃	-5		5	%
Protection						
nINT Low Pulse duration when a Protection Occurs	t_{INT}			256		μs

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VBUS OVP Rising Threshold Range	$V_{BUS_OVP_R}$	In forward 4:1 / reverse 1:4 mode	I²C programmable, 21V by default	21		22	V
			Accuracy at 21V $V_{BUS_OVP_R}$	-3		3	%
			V_{BUS_OVP} hysteresis		0.85		V
		In forward 2:1 / reverse 1:2 mode	I²C programmable, 12V by default	12		13	V
			Accuracy at 12V $V_{BUS_OVP_R}$	-3		3	%
			V_{BUS_OVP} hysteresis		0.85		V
		In forward 1:1 / reverse 1:1 mode	I²C programmable, 5.6V by default	5.6		6	V
			Accuracy at 5.6V $V_{BUS_OVP_R}$	-3.5		3.5	%
			V_{BUS_OVP} hysteresis		160		mV
VBUS OVP Rising Deglitch Time	$t_{VBUS_OVPR_DEG}$	Deglitch between V_{VBUS} rising above $V_{BUS_OVP_R}$ and triggering protection action			1		ms
VBUS Peak OVP Rising Threshold	$V_{BUS_PK_OVP}$	In forward 4:1 / reverse 1:4 mode		25.2	26	26.8	V
		In forward 2:1 / reverse 1:2 mode		15.5	16	16.5	
		In forward 1:1 / reverse 1:1 mode		6.75	7	7.25	
VBUS Peak OVP Rising Deglitch Time	$t_{VBUS_PK_DEG}$				100		ns
VBUS UVP Falling Threshold Range for Forward Mode	$V_{BUS_UVP_F}$	In forward 4:1 mode	I²C programmable, 13V by default	12		13	V
			Accuracy at 13V $V_{BUS_UVP_F}$	-3		3	%
			V_{BUS_UVP} hysteresis		0.45		V
		In forward 2:1 mode	I²C programmable, 6.5V by default	6		6.5	V
			Accuracy at 6.5V $V_{BUS_UVP_F}$	-3		3	%
			V_{BUS_UVP} hysteresis		0.45		V
VBUS UVP Falling Deglitch Time	$t_{VBUS_UVPF_DEG}$	Deglitch between V_{VBUS} falling below $V_{BUS_UVP_F}$ and triggering protection action			10		ms
IBUS UCP Rising Threshold	$I_{BUS_UCP_R}$			100	200	300	mA
IBUS UCP Falling Threshold	$I_{BUS_UCP_F}$	Falling, $I_{BUS_UCP_F}$ = 100mA		50	100	150	mA
IBUS OCP Threshold Range	I_{BUS_OCP}	I²C programmable	In forward 4:1 mode	3.75		4	A
			In forward 2:1 / forward 1:1 mode	6		7	
			In reverse 1:4 mode	1.25		1.5	
			In reverse 1:2 mode	2.5		3	
			In reverse 1:1 mode	0.5		6	
IBUS OCP Threshold Accuracy	$I_{BUS_OCP_ACC}$	I_{BUS_OCP} = 3.75A (in forward 4:1 mode), internal accuracy		-4		4	%
IBUS Reverse OCP Threshold Range in Forward Mode	I_{BUS_RCP}	In forward mode			0.7		A
VOUT OVP Rising Threshold Range	$V_{OUT_OVP_R}$	I²C programmable, 200mV per step, 4.8V by default		4.6		5.2	V
VOUT OVP Threshold Accuracy	$V_{OUT_OVP_ACC}$	$V_{OUT_OVP_R}$ = 4.8V		-3		3	%
VOUT OVP Threshold Hysteresis	$V_{OUT_OVP_HYS}$				100		mV
VBATx OVP Rising Threshold Range	$V_{BAT_OVP_R}$	I²C programmable, 100mV per step, 4.6V by default		4.5		5.2	V
VBATx OVP Threshold Accuracy	$V_{BAT_OVP_ACC}$	$V_{BATx_OVP_R}$ = 4.6V, internal accuracy		-0.5		0.5	%
VBATx OVP Threshold Hysteresis	$V_{BAT_OVP_HYS}$				100		mV
IBAT OCP Threshold Range	I_{BAT_OCP}	Bidirectional I_{BAT}, I²C programmable, 8.5A by default		5		15	A
IBAT OCP Threshold Accuracy	$I_{BAT_OCP_ACC}$	I_{BAT} = 8.5A, R_{SNS} = 2mΩ		-2		2	%

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TDIE OTP Rising Threshold Range	$T_{DIE_OTP_R}$	I²C programmable, 20℃ per step, +140℃ by default	80		140	℃
TDIE OTP Threshold Accuracy	$T_{DIE_OTP_ACC}$		-5		5	℃
TDIE OTP Threshold Hysteresis	$T_{DIE_OTP_HYS}$			20		℃
TDIE OTP Alarm Rising Threshold Range	$T_{DIEOTP_ALM_R}$	I²C programmable, 20℃ per step, +120℃ by default	60		120	℃
TDIE OTP Alarm Threshold Accuracy	$T_{DIEOTP_ALM_ACC}$		-5		5	℃
TDIE OTP Alarm Threshold Hysteresis	$T_{DIEOTP_ALM_HYS}$			20		℃
Watchdog Time Out Range	t_{WDT}	I²C programmable, 1s by default	0.5		4	s
ADC Specification						
ADC Resolution	ADC_{RES}			12		bits
ADC VUSB Voltage Readable in REG0x24 and REG0x25	V_{USB_ADC}	Effective range	3		22	V
		LSB		6		mV
VUSB ADC Accuracy	$V_{USB_ADC_ACC}$	V_{VUSB} = 10V, internal accuracy, T_J = +25℃	-1.3		0.3	%
		V_{VUSB} = 10V, internal accuracy, T_J = 0℃ to +125℃	-1.3		0.4	
		V_{VUSB} = 20V, internal accuracy, T_J = +25℃	-0.8		0.8	
		V_{VUSB} = 20V, internal accuracy, T_J = 0℃ to +125℃	-0.8		0.8	
ADC VWPC Voltage Readable in REG0x26 and REG0x27	V_{WPC_ADC}	Effective range	3		22	V
		LSB		6		mV
VWPC ADC Accuracy	$V_{WPC_ADC_ACC}$	V_{VWPC} = 10V, internal accuracy, T_J = +25℃	-1.0		0.8	%
		V_{VWPC} = 10V, internal accuracy, T_J = 0℃ to +125℃	-1.1		0.8	
		V_{VWPC} = 20V, internal accuracy, T_J = +25℃	-0.7		1.2	
		V_{VWPC} = 20V, internal accuracy, T_J = 0℃ to +125℃	-0.7		1.2	
ADC VBUS Voltage Readable in REG0x22 and REG0x23	V_{BUS_ADC}	Effective range	3		22	V
		LSB		6		mV
VBUS ADC Accuracy	$V_{BUS_ADC_ACC}$	V_{VBUS} = 10V, internal accuracy, T_J = +25℃	-1.0		0.5	%
		V_{VBUS} = 10V, internal accuracy, T_J = 0℃ to +125℃	-1.1		0.5	
		V_{VBUS} = 20V, internal accuracy, T_J = +25℃	-0.6		0.9	
		V_{VBUS} = 20V, internal accuracy, T_J = 0℃ to +125℃	-0.6		0.9	
ADC IBUS Current Readable in REG0x28 and REG0x29	I_{BUS_ADC}	Effective range	-6		6	A
		LSB		2		mA
IBUS ADC Accuracy	$I_{BUS_ADC_ACC}$	I_{BUS} = 1A, internal accuracy, T_J = 0℃ to +125℃	-4		6	%
		I_{BUS} = 2A, internal accuracy, T_J = 0℃ to +125℃	-4		5	
		I_{BUS} = 5A, internal accuracy, T_J = 0℃ to +125℃	-4		4	
ADC VBAT1 Voltage Readable in REG0x2E and REG0x2F	V_{BAT1_ADC}	Effective range	3		5	V
		LSB		2		mV
ADC VBAT2 Voltage Readable in REG0x30 and REG0x31	V_{BAT2_ADC}	Effective range	3		5	V
		LSB		2		mV
VBATx ADC Accuracy	$V_{BATx_ADC_ACC}$	Internal accuracy, T_J = 0℃ to +125℃	-0.6		0.6	%

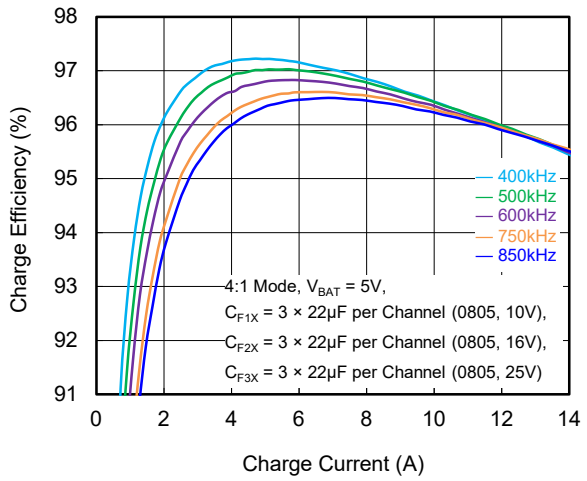
ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise specified.)

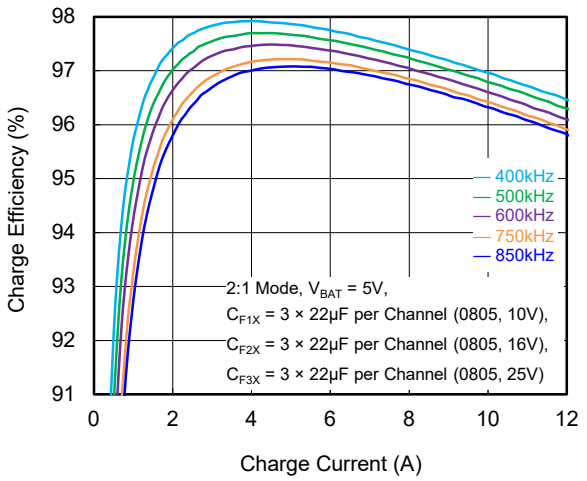
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC IBAT Current Readable in REG0x34 and REG0x35	I_{BAT_ADC}	Effective range	-6		16	A
		LSB		4		mA
IBAT ADC Accuracy	$I_{BAT_ADC_ACC}$	I_{BAT} = 1A, R_{SNS} = 1mΩ, internal accuracy, T_J = 0℃ to +125℃	-4		4	%
		I_{BAT} = 2A, R_{SNS} = 1mΩ, internal accuracy, T_J = 0℃ to +125℃	-3		3	%
		I_{BAT} = 10A, R_{SNS} = 1mΩ, internal accuracy, T_J = 0℃ to +125℃	-2		2	%
ADC VOUT Voltage Readable in REG0x32 and REG0x33	V_{OUT_ADC}	Effective range	3		5	V
		LSB		2		mV
VOUT ADC Accuracy	$V_{OUT_ADC_ACC}$	V_{VOUT} = 3V to 5.1V, internal accuracy, T_J = 0℃ to +125℃	-1		0.4	%
ADC DIE Temperature Readable in REG0x36	T_{DIE_ADC}	Effective range	-40		150	℃
		LSB		1		℃
TDIE ADC Accuracy	$T_{DIE_ADC_ACC}$		-5		5	℃
I²C Interface (SCL and SDA Pins)						
High Level Input Voltage	V_{IH_I2C}	SCL and SDA pins	0.9			V
Low Level Input Voltage	V_{IL_I2C}	SCL and SDA pins			0.4	V
Low Level Output Voltage	V_{OL_SDA}	Sink 2mA, SDA pin			0.4	mV
SCL Clock Frequency	f_{CLK}		100		1000	kHz
Logic I/O Threshold (nLPM and nINT Pins)						
High Level Input Voltage	V_{IH}	nLPM pin	0.9			V
Low Level Input Voltage	V_{IL}	nLPM pin			0.4	V
nLPM Pull-Down Resistance	R_{PDN_nLPM}	Pulled down to AGND		1.3		MΩ
Low Level Output Voltage	V_{OL}	Sink 2mA, nINT pin			0.4	V
BC1.2 Detection (DP and DM Pins)						
Data Contact Detect Current Source	I_{DP_SRC}	DP pin, T_J = +25℃	7	10	13	μA
DM Pull-Down Resistance	R_{DM_DWN}	DM pin	16	18	20	kΩ
Data Contact Detect Logic Low Threshold	V_{LGC_LOW}	DP pin			0.95	V
Data Contact Detect Debounce Time	t_{DCD_DBNC}			15		ms
DP Force Detect Voltage	V_{DP_SRC}	DP pin	0.55	0.6	0.65	V
DM Sink Current	I_{DM_SNK}	DM pin	60	100	140	μA
DP Voltage Source On Time	t_{VDPSRC_ON}	DP pin		60		ms
Pull-Down Detect Threshold	V_{DAT_REF}		0.25	0.325	0.4	V
DM Force Detect Voltage	V_{DM_SRC}	DM pin	0.55	0.6	0.65	V
DP Sink Current	I_{DP_SNK}	DP pin	60	100	140	μA
DM Voltage Source On Time	t_{VDMSRC_ON}	DM pin		60		ms

TYPICAL PERFORMANCE CHARACTERISTICS

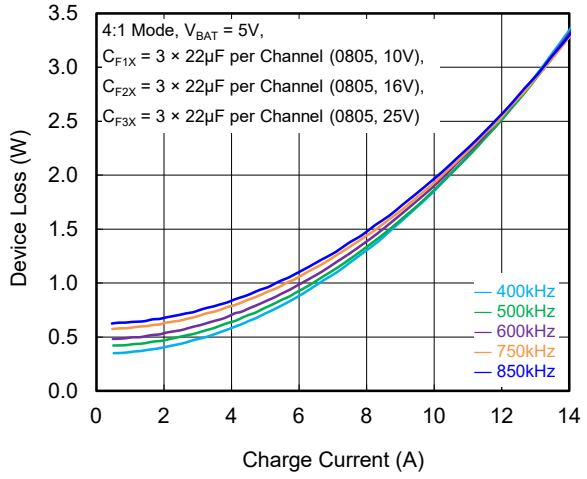
Charge Efficiency vs. Charge Current



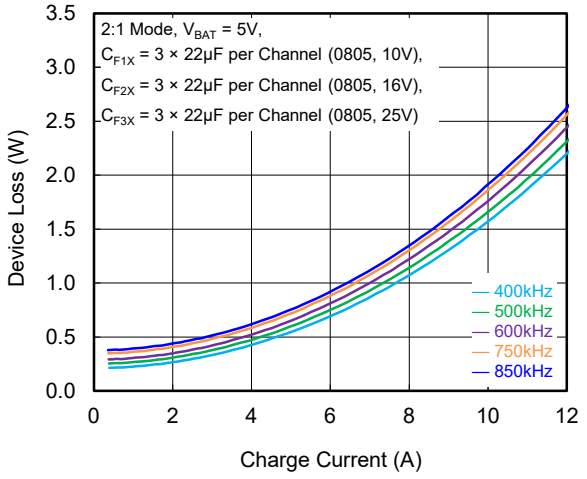
Charge Efficiency vs. Charge Current



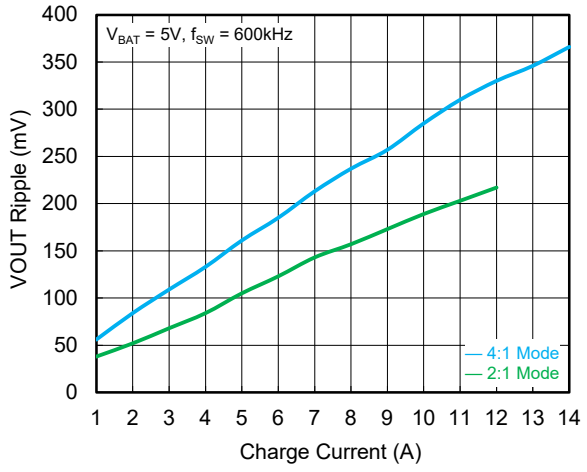
Device Loss vs. Charge Current



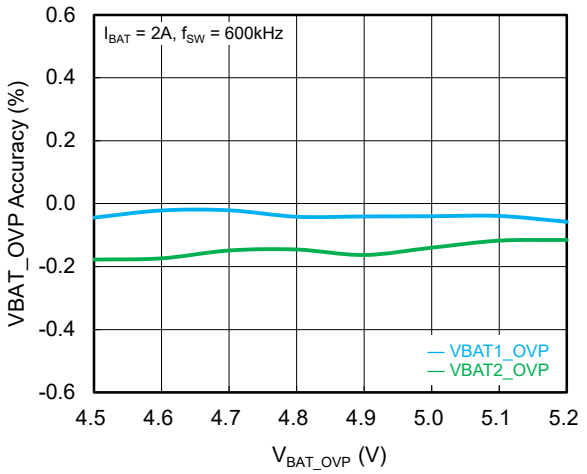
Device Loss vs. Charge Current



VOUT Ripple at 600kHz

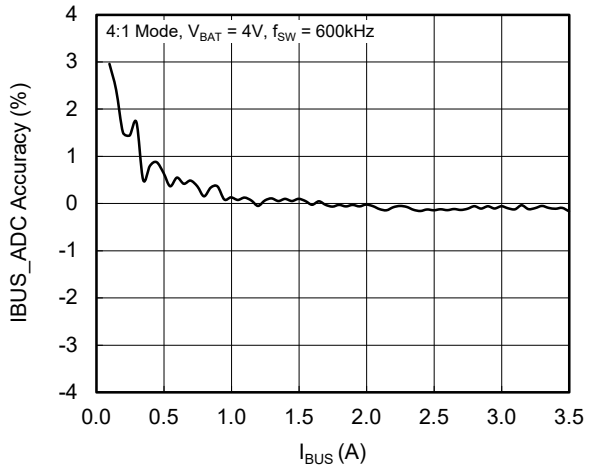


VBAT_OVP Accuracy vs. VBAT_OVP Setting Voltage

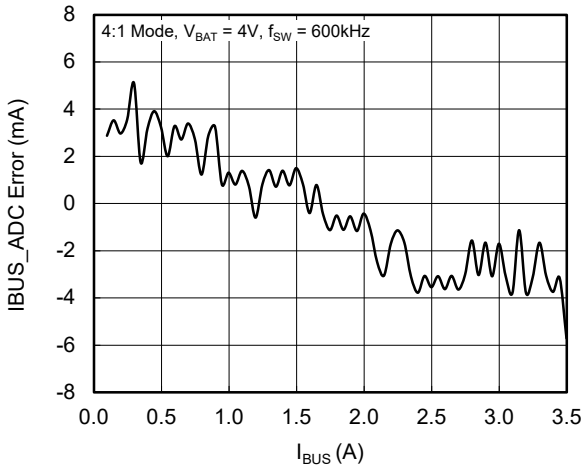


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

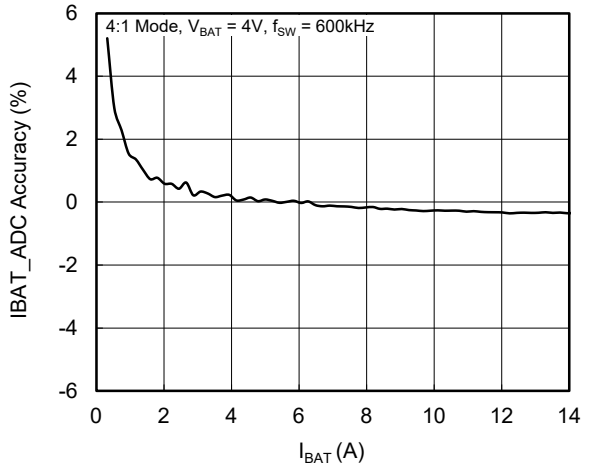
IBUS_ADC Accuracy vs. BUS Current



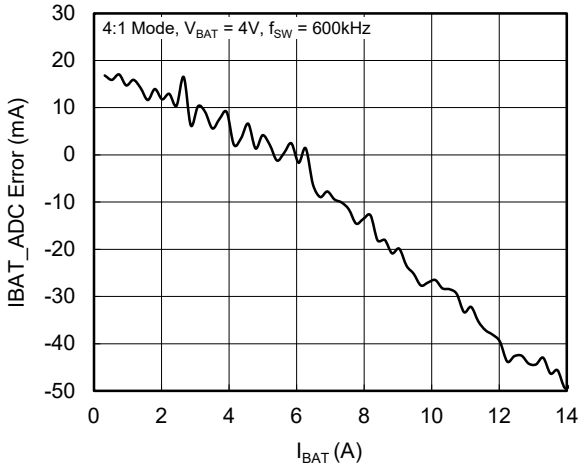
IBUS_ADC Error vs. BUS Current



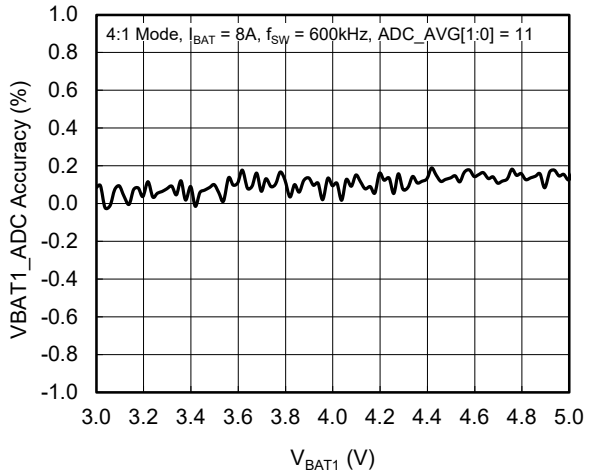
IBAT_ADC Accuracy vs. BAT Current



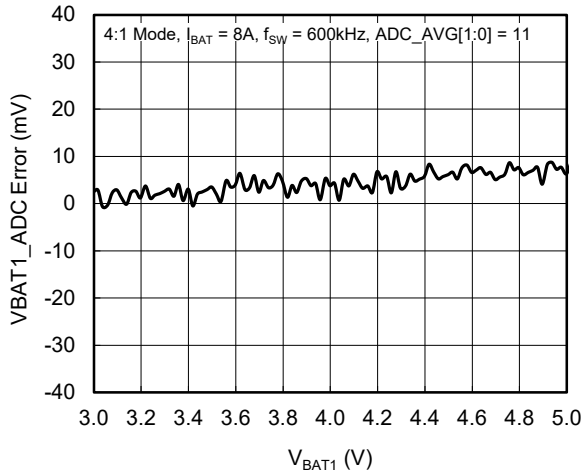
IBAT_ADC Error vs. BAT Current



VBAT1_ADC Accuracy vs. BAT1 Voltage



VBAT1_ADC Error vs. BAT1 Voltage



FUNCTIONAL BLOCK DIAGRAM

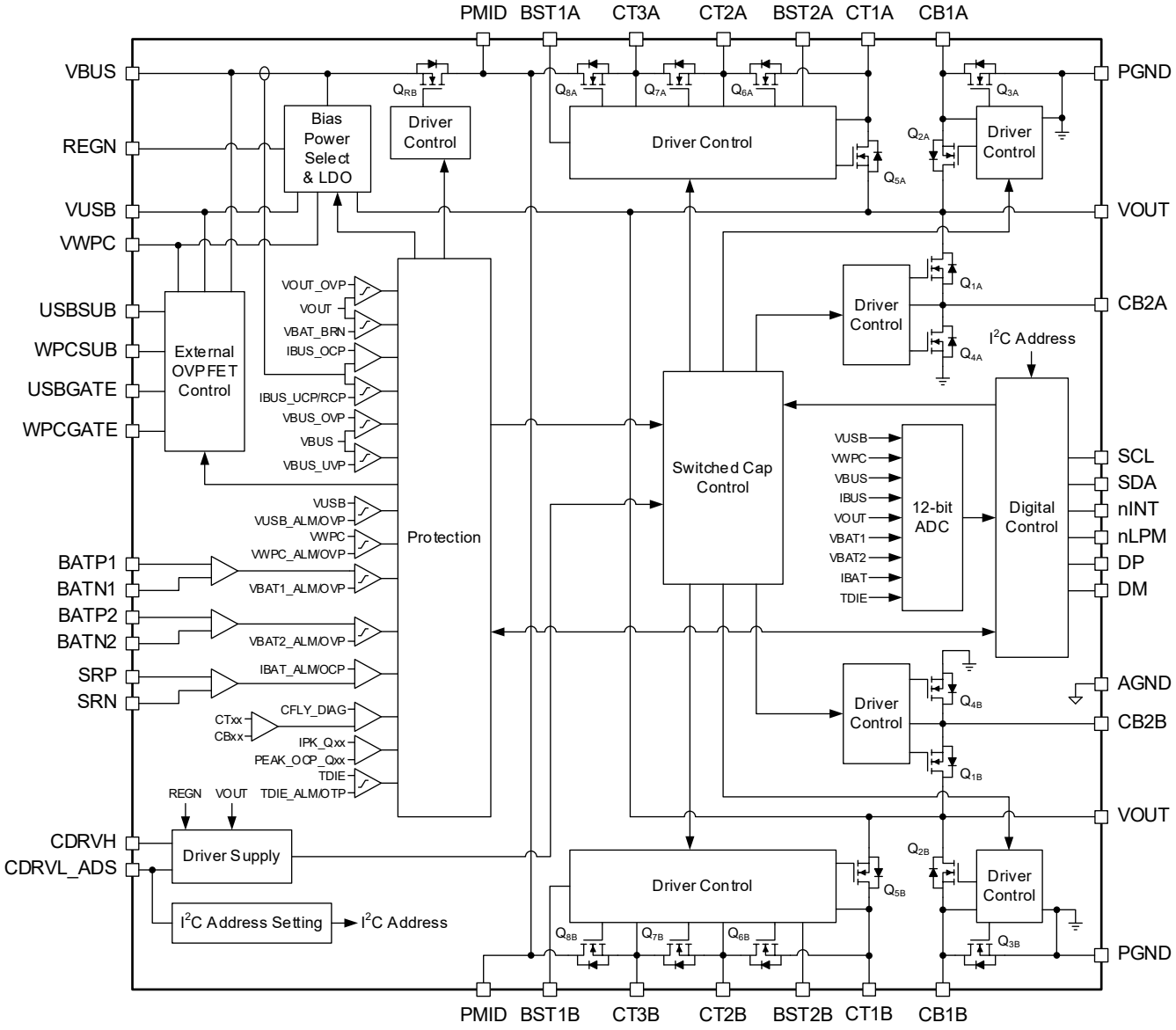


Figure 2. Functional Block Diagram

I²C REGISTER ADDRESS MAP

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

The device I²C Address is determined by the state of CDRVL_ADS pin in the POR sequence, as described in I²C Address Setting section.

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE	DEGLITCH
REG_RST	--	--	--	--	0x03[7]	--
SCC_MODE	0x04[4]	--	--	0x03[6:4]	0x04[7]	--
WATCHDOG	--	0x19[5]	0x1A[5]	0x03[2:0]	0x03[3]	--
FSW_SET	--	--	--	0x07[7:5]	--	--
FSW_SHIFT	--	--	--	0x07[4:3]	0x07[4:3]	--
FSW_DITHER	--	--	--	--	0x07[2]	--
USBGATE	0x0F[1]	--	--	--	0x04[2] & 0x0F[3]	--
VUSB2VOUT_OVP	--	0x13[7]	0x14[7]	0x05[7]	0x37[6]	0x05[6]
VUSB_OVP_ALM	--	0x1B[7]	0x1C[7]	0x05[5:3]	0x39[2]	--
VUSB_OVP	--	0x11[7]	0x12[7]	0x05[2:0]	0x37[5]	--
VUSB_ABSENT	--	0x11[1]	0x12[1]	--	0x37[7]	--
VUSB_INSERT	--	0x17[1]	0x18[1]	--	--	--
VUSB_PDN	--	0x11[6]	0x12[6]	--	0x0F[6]	--
WPCGATE	0x0F[0]	--	--	--	0x04[0] & 0x0F[2]	--
VWPC2VOUT_OVP	--	0x13[6]	0x14[6]	0x06[7]	0x37[3]	0x06[6]
VWPC_OVP_ALM	--	0x1B[6]	0x1C[6]	0x06[5:3]	0x39[1]	--
VWPC_OVP	--	0x11[5]	0x12[5]	0x06[2:0]	0x37[2]	--
VWPC_ABSENT	--	0x11[0]	0x12[0]	--	0x37[4]	--
VWPC_INSERT	--	0x17[0]	0x18[0]	--	--	--
VWPC_PDN	--	0x11[4]	0x12[4]	--	0x0F[5]	--
VBUS_OVP	--	0x11[3]	0x12[3]	F41 & R14: 0x08[7] F21 & R12: 0x08[6] F11 & R11: 0x08[5]	0x37[1]	--
VBUS_PK_OVP				--	0x37[0]	
VBUS_PRESENT	--	0x19[7]	0x1A[7]	--	--	--
VBUS_UVP	--	0x17[3]	0x18[3]	F41: 0x0C[1]	0x39[6]	--
		0x17[2]	0x18[2]	F21: 0x0C[0]		
VBUS_PDN	--	0x11[2]	0x12[2]	--	0x0F[4]	--
VBUS_ABSENT	--	0x19[4]	0x1A[4]	--	0x39[7]	0x0C[3]
VBUS_LO	--	0x1B[4]	0x1C[4]	--	0x3A[5]	--
VBUS_HI	--	0x1B[3]	0x1C[3]	--	0x3A[4]	--
PMID2VOUT_UVP	--	0x13[5]	0x14[5]	0x0A[7:6]	0x38[4]	0x0A[5]
PMID2VOUT_OVP	--	0x13[4]	0x14[4]	0x0A[4:3]	0x38[3]	0x0A[2]
IBUS_OCP	--	0x13[3]	0x14[3]	F41: 0x0B[7]	0x38[2]	0x0B[3]
		0x13[2]	0x14[2]	F21 & F11: 0x0B[6]		
		0x13[1]	0x14[1]	R14: 0x0B[5]		
		0x13[0]	0x14[0]	R12: 0x0B[4] R11: 0x0A[1:0] & 0xD0[2:1]		

I²C REGISTER ADDRESS MAP (continued)

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE	DEGLITCH
IBUS_UCP_FALL	--	0x17[5]	0x18[5]	--	0x38[1]	0x0B[2]
IBUS_UCP_TIMEOUT	--	0x19[3]	0x1A[3]	0x0B[1:0]	0x38[1]	--
IBUS_RCP	--	0x17[4]	0x18[4]	--	0x38[0]	0x0C[2]
VOUT_OVP	--	0x15[0]	0x16[0]	0x08[4:3]	0x38[7]	0x08[2]
VBAT_INSERT	--	0x19[6]	0x1A[6]	--	--	--
VBAT_BRN_OUT	--	0x19[0]	0x1A[0]	--	0x3A[6]	--
VBAT_OVP	--	0x15[7]	0x16[7]	VBAT1: 0x0D[7:5]	0x39[5]	0x0D[4]
		0x15[6]	0x16[6]	VBAT2: 0x0D[3:1]	0x39[4]	0x0D[0]
VBAT_OVP_ALM	--	0x1B[2]	0x1C[2]	VBAT1: 0x1D[7:6]	0x3A[3]	--
		0x1B[1]	0x1C[1]	VBAT2: 0x1D[5:4]	0x3A[2]	--
IBAT_OCP	--	0x15[5]	0x16[5]	0x0E[7:4] & 0x0E[3:2]	0x39[3]	0x0F[7]
IBAT_OCP_ALM	--	0x1B[0]	0x1C[0]	0x1D[3:2]	0x3A[1]	--
PEAK_OCP (Bidirectional)	--	0x17[6]	0x18[6]	Q_{4X}: 0x09[3] Q_{3X}: 0x09[2] Q_{2X}: 0x09[1] Q_{1X}: 0x09[0]	0x38[5]	--
PIN_DIAG	--	0x19[1]	0x1A[1]	--	--	--
TDIE_OTP	--	0x15[1]	0x16[1]	0x0C[7:6]	0x3A[7]	--
TDIE_OTP_ALM	--	0x1B[5]	0x1C[5]	0x0C[5:4]	0x39[0]	--
ADC	--	0x19[2]	0x1A[2]	0x20[6]	0x20[7]	0x21[1:0]

REGISTER AND DATA

Bit Types:

R: Read only

R/W: Read/Write

RC: Read clears the bit

R/WC: Read/Write. Writing a '1' clears the bit. Writing a '0' has no effect.

NOTE: Excepted for the specified bits, all other register bits are reset to their default values if a hard reset is triggered.

REG0x00: DEVICE_INFO0 Register [reset = 0x0A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	DEVICE_VER[3:0]	0000	R	Device Version	N/A
D[3:0]	DEVICE_ID[3:0]	1010	R	Device ID 1010 = SGM41611	N/A

REG0x01: DEVICE_INFO1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	ROM_ID[3:0]	0000	R	ROM ID	N/A
D[3:0]	CNFG_ID[3:0]	0000	R	Configuration ID	N/A

REG0x02: DEVICE_INFO2 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	PE_ID[3:0]	0000	R	PE ID	N/A
D[3:0]	Reserved	0000	R	Reserved	N/A

REGISTER AND DATA (continued)

REG0x03: CONTROL1 Register [reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	REG_RST	0	R/WC	Register Reset Bit 0 = No register reset (default) 1 = Reset registers to their default values. When enabled, the associated register bits are reset to their default values and then this bit is automatically reset to 0.	Hard-reset or REG_RST
D[6:4]	SCC_MODE[2:0]	000	R/W	Switched-Cap Converter Operation Mode Control Bits 000 = Forward 1:1 charger mode (default) 001 = Forward 2:1 charger mode 010 = Forward 4:1 charger mode 011 = Reverse 1:1 converter mode 100 = Reverse 1:2 converter mode 101 = Reverse 1:4 converter mode 110 ~ 111 = Reserved Notes: 1. These bits are not allowed to change during operation. 2. Before forward 2:1 charge mode is enabled, F21_PERFORMANCE bit in REG0x08 should be set to 1.	Hard-reset or REG_RST or WDT
D[3]	WDT_DIS	0	R/W	Watchdog Timer Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[2:0]	WDT_TIMER[2:0]	001	R/W	Watchdog Timer Setting Bits 000 = 0.5s 001 = 1s (default) 010 = 2s 011 = 4s 100 ~ 111 = Reserved When the watchdog timer times out, the device first resets the SCC_EN bit to 0, and then resets SCC_MODE[2:0] bits to 000.	Hard-reset or REG_RST

REG0x04: CONTROL2 Register [reset = 0x05]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	SCC_EN	0	R/W	Switched-Cap Converter Enable Bit 0 = Disabled (default) 1 = Enabled. If any fault has occurred, device returns to standby mode and this bit is automatically cleared to 0.	Hard-reset or REG_RST or WDT
D[6:5]	Reserved	00	R	Reserved	N/A
D[4]	SCC_SW_STAT	0	R	Switched-Cap Converter Switching State Bit 0 = SCC is not in switching mode 1 = SCC is in switching mode	Hard-reset or REG_RST
D[3]	USBGATE_MODE	0	R/W	USBGATE Operation Mode Setting Bit 0 = Auto mode for SCC forward operation (default) 1 = Manual mode	Hard-reset or REG_RST
D[2]	USBGATE_EN	1	R/W	USBGATE Driver Enable Bit 0 = Disable USBGATE output 1 = Enable USBGATE output high (default)	Hard-reset or REG_RST
D[1]	WPCGATE_MODE	0	R/W	WPCGATE Operation Mode Setting Bit 0 = Auto mode for SCC forward operation (default) 1 = Manual mode	Hard-reset or REG_RST
D[0]	WPCGATE_EN	1	R/W	WPCGATE Driver Enable Bit 0 = Disable WPCGATE output 1 = Enable WPCGATE output high (default)	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x05: VUSB_OVP Register [reset = 0x09]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VUSB2VOUT_OVP	0	R/W	VUSB2VOUT OVP Protection Rising Threshold Setting Bit for Forward Mode $V_{USB2VOUT}$ = V_{VUSB}/n - V_{VOUT} (n = 1, 2, or 4, depending on the operation mode) 0 = The $V_{USB2VOUT}$ OVP rising threshold is 0.4V (default) 1 = The $V_{USB2VOUT}$ OVP rising threshold is 0.5V	Hard-reset or REG_RST
D[6]	VUSB2VOUT_OVP_DEG	0	R/W	VUSB2VOUT OVP Protection Deglitch Time ($t_{VUSB2VOUT_OVP_DEG}$) Setting Bit for Forward Mode 0 = 100ns (default) 1 = 128μs	Hard-reset or REG_RST
D[5:3]	VUSB_OVP_ALM[2:0]	001	R/W	VUSB OVP Alarm Rising Threshold Setting Bits for Forward Mode The VUSB OVP alarm rising threshold should be set lower than $V_{USB_OVP_R}$ to ensure proper operation. 000 = 6.5V 001 = 10V (default) 010 = 11V 011 = 12V 100 = 19V 101 = 20V 110 = 21V 111 = 22V	Hard-reset or REG_RST
D[2:0]	VUSB_OVP[2:0]	001	R/W	VUSB OVP Protection Rising Threshold Setting Bits for Forward Mode The VUSB OVP protection rising threshold should be set higher than $V_{USBOVP_ALM_R}$ to ensure proper operation. 000 = 7.5V 001 = 11V (default) 010 = 12V 011 = 13V 100 = 20V 101 = 21V 110 = 22V 111 = 23V	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x06: VWPC_OVP Register [reset = 0x36]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VWPC2VOUT_OVP	0	R/W	VWPC2VOUT OVP Protection Rising Threshold Setting Bit for Forward Mode $V_{WPC2VOUT}$ = V_{VWPC}/n - V_{VOUT} (n = 1, 2, or 4, depending on the operation mode) 0 = The $V_{WPC2VOUT}$ OVP rising threshold is 0.4V (default) 1 = The $V_{WPC2VOUT}$ OVP rising threshold is 0.5V	Hard-reset or REG_RST
D[6]	VWPC2VOUT _OVP_DEG	0	R/W	VWPC2VOUT OVP Protection Deglitch Time ($t_{VWPC2VOUT_OVP_DEG}$) Setting Bit for Forward Mode 0 = 100ns (default) 1 = 128μs	Hard-reset or REG_RST
D[5:3]	VWPC_OVP_ALM[2:0]	110	R/W	VWPC OVP Alarm Rising Threshold Setting Bits for Forward Mode The VWPC OVP alarm rising threshold should be set lower than $V_{WPC_OVP_R}$ to ensure proper operation. 000 = 6.5V 001 = 10V 010 = 11V 011 = 12V 100 = 19V 101 = 20V 110 = 21V (default) 111 = 22V	Hard-reset or REG_RST
D[2:0]	VWPC_OVP[2:0]	110	R/W	VWPC OVP Protection Rising Threshold Setting Bits for Forward Mode The VWPC OVP protection rising threshold should be set higher than $V_{WPCOVP_ALM_R}$ to ensure proper operation. 000 = 7.5V 001 = 11V 010 = 12V 011 = 13V 100 = 20V 101 = 21V 110 = 22V (default) 111 = 23V	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x07: SC_CTRL Register [reset = 0x40]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	FSW_SET[2:0]	010	R/W	Switched-Cap Converter Switching Frequency Setting Bits 000 = 400kHz 001 = 500kHz 010 = 600kHz (default) 011 = 750kHz 100 = 850kHz 101 = 1000kHz 110 = 1250kHz 111 = 1500kHz Note: These bits are allowed to change to the adjacent setting during switching.	Hard-reset or REG_RST
D[4:3]	FSW_SHIFT[1:0]	00	R/W	Bits of Adjusting Switching Frequency for EMI 00/11 = Nominal frequency (default) 01 = Nominal frequency +10% 10 = Nominal frequency -10%	Hard-reset or REG_RST
D[2]	FSW_DITHER_EN	0	R/W	Switching Frequency Dithering Enable Bit 0 = Disabled (default) 1 = Enabled. Dither varies switching frequency ±10%	Hard-reset or REG_RST
D[1]	USBFET_ON_ DIRECTION	0	R/W	Direction Control Bit to turn on external USB FET. 0 = Forward (VUSB present, turn on USB FET) 1 = Reverse (VBUS present, turn on USB FET) Note: When the OVPFET operates in reverse manual mode, set this bit to 1 before turn-on USB FET.	Hard-reset or REG_RST
D[0]	WPCFET_ON_ DIRECTION	0	R/W	Direction Control Bit to turn on external WPC FET. 0 = Forward (VWPC present, turn on WPC FET) 1 = Reverse (VBUS present, turn on WPC FET) Note: When the OVPFET operates in reverse manual mode, set this bit to 1 before turn-on WPC FET.	Hard-reset or REG_RST

REG0x08: VBUS&VOUT_OVP Register [reset = 0x0C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_OVP41	0	R/W	Setting Bit of VBUS OVP Protection Rising Threshold for 4:1 or 1:4 Mode 0 = 21V (default) 1 = 22V	Hard-reset or REG_RST
D[6]	VBUS_OVP21	0	R/W	Setting Bit of VBUS OVP Protection Rising Threshold for 2:1 or 1:2 Mode 0 = 12V (default) 1 = 13V	Hard-reset or REG_RST
D[5]	VBUS_OVP11	0	R/W	Setting Bit of VBUS OVP Protection Rising Threshold for Forward or Reverse 1:1 Mode 0 = 5.6V (default) 1 = 6V	Hard-reset or REG_RST
D[4:3]	VOUT_OVP[1:0]	01	R/W	VOUT OVP Protection Rising Threshold Setting Bits $V_{OUT_OVP_R}$ = 4.6V + VOUT_OVP[1:0] × 200mV 00 = 4.6V 01 = 4.8V (default) 10 = 5V 11 = 5.2V	Hard-reset or REG_RST
D[2]	VOUT_OVP_DEG	1	R/W	VOUT OVP Protection Deglitch Time ($t_{VOUT_OVPR_DEG}$) Setting Bit 0 = 100μs 1 = 1ms (default)	Hard-reset or REG_RST
D[1]	F21_PERFORMANCE	0	R/W	Forward 2:1 Mode Switching Setting Bit Before forward 2:1 charge mode is enabled, this bit should be set to 1.	Hard-reset or REG_RST
D[0]	Reserved	0	R	Reserved	N/A

REGISTER AND DATA (continued)

REG0x09: PEAK_OCP Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3]	PEAK_OCP_Q4x	0	R/W	Q_{4X} Bidirectional Peak OCP Protection Threshold Setting Bit 0 = 9.5A (default) 1 = 11.5A	Hard-reset or REG_RST
D[2]	PEAK_OCP_Q3x	0	R/W	Q_{3X} Bidirectional Peak OCP Protection Threshold Setting Bit 0 = 17.5A (default) 1 = 20A	Hard-reset or REG_RST
D[1]	PEAK_OCP_Q2x	0	R/W	Q_{2X} Bidirectional Peak OCP Protection Threshold Setting Bit 0 = 17.5A (default) 1 = 20A	Hard-reset or REG_RST
D[0]	PEAK_OCP_Q1x	0	R/W	Q_{1X} Bidirectional Peak OCP Protection Threshold Setting Bit 0 = 13A (default) 1 = 16A	Hard-reset or REG_RST

REG0x0A: PMID2VOUT_PROT Register [reset = 0x41]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	PMID2VOUT_UVP[1:0]	01	R/W	PMID2VOUT UVP Protection Falling Threshold Setting Bits $V_{PMID2VOUT}$ = V_{PMID}/n - V_{VOUT} (n = 1, 2, or 4, depending on the operation mode) $V_{PMID2VOUT_UVP}$ = -25mV - PMID2VOUT_UVP[1:0] × 25mV for the forward operation mode $V_{PMID2VOUT_UVP_RVS}$ = -50mV - PMID2VOUT_UVP[1:0] × 50mV for the reverse operation mode 00 = -25mV for forward or -50mV for reverse 01 = -50mV for forward or -100mV for reverse (default) 10 = -75mV for forward or -150mV for reverse 11 = -100mV for forward or -200mV for reverse	Hard-reset or REG_RST
D[5]	PMID2VOUT_UVP_DEG	0	R/W	PMID2VOUT UVP Protection Deglitch Time ($t_{PMID2VOUT_UVP_DEG}$) Setting Bit 0 = 8μs (default) 1 = 1ms	Hard-reset or REG_RST
D[4:3]	PMID2VOUT_OVP[1:0]	00	R/W	PMID2VOUT OVP Protection Rising Threshold Setting Bits $V_{PMID2VOUT}$ = V_{PMID}/n - V_{VOUT} (n = 1, 2, or 4, depending on the operation mode) $V_{PMID2VOUT_OVP}$ = 200mV + PMID2VOUT_OVP[1:0] × 100mV 00 = 200mV (default) 01 = 300mV 10 = 400mV 11 = 500mV	Hard-reset or REG_RST
D[2]	PMID2VOUT_OVP_DEG	0	R/W	PMID2VOUT OVP Protection Deglitch Time ($t_{PMID2VOUT_OVP_DEG}$) Setting Bit 0 = 100ns (default) 1 = 128μs	Hard-reset or REG_RST
D[1:0]	IBUS_OCP_R11[1:0]	01	R/W	Setting Bits of IBUS OCP Protection Threshold for Reverse 1:1 Mode 00 = 0.5A 01 = 1A (default) 10 = 2A 11 = 3A Note: These bits configurations are valid only when IBUS_OCP_R11_E[1:0] = 00 in REG0xD0.	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x0B: IBUS_PROT Register [reset = 0x31]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBUS_OCP41	0	R/W	Setting Bit of IBUS OCP Protection Threshold for Forward 4:1 Mode 0 = 3.75A (default) 1 = 4A	Hard-reset or REG_RST
D[6]	IBUS_OCP21	0	R/W	Setting Bit of IBUS OCP Protection Threshold for Forward 2:1 Mode and Forward 1:1 Mode 0 = 6A (default) 1 = 7A	Hard-reset or REG_RST
D[5]	IBUS_OCP14	1	R/W	Setting Bit of IBUS OCP Protection Threshold for Reverse 1:4 Mode 0 = 1.25A 1 = 1.5A (default)	Hard-reset or REG_RST
D[4]	IBUS_OCP12	1	R/W	Setting Bit of IBUS OCP Protection Threshold for Reverse 1:2 Mode 0 = 2.5A 1 = 3A (default)	Hard-reset or REG_RST
D[3]	IBUS_OCP_DEG	0	R/W	IBUS OCP Protection Deglitch Time ($t_{IBUS_OCP_DEG}$) Setting Bit 0 = 4μs (default) 1 = 64μs	Hard-reset or REG_RST
D[2]	IBUS_UCP_FALL_DEG	0	R/W	IBUS UCP Protection Falling Deglitch Time ($t_{IBUS_UCPF_DEG}$) Setting Bit 0 = 32ms (default) 1 = 256ms	Hard-reset or REG_RST
D[1:0]	IBUS_UCP_BLK[1:0]	01	R/W	IBUS UCP Protection Blanking Time Setting Bits After soft-start, $t_{IBUS_UCP_BLK}$ = 100ms × 2 ^ IBUS_UCP_BLK[1:0] 00 = 100ms 01 = 200ms (default) 10 = 400ms 11 = 800ms	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x0C: VBUS_PROT Register [reset = 0xFB]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	TDIE_OTP[1:0]	11	R/W	TDIE OTP Protection Rising Threshold Setting Bits $T_{DIE_OTP_R}$ = 80℃ + TDIE_OTP[1:0] × 20℃ 00 = +80℃ 01 = +100℃ 10 = +120℃ 11 = +140℃ (default)	Hard-reset or REG_RST
D[5:4]	TDIE_OTP_ALM[1:0]	11	R/W	TDIE OTP Alarm Rising Threshold Setting Bits $T_{DIE_ALM_R}$ = 60℃ + TDIE_OTP[1:0] × 20℃ The TDIE OTP alarm rising threshold should be set lower than $T_{DIE_OTP_R}$ to ensure proper operation. 00 = +60℃ 01 = +80℃ 10 = +100℃ 11 = +120℃ (default)	Hard-reset or REG_RST
D[3]	VBUS_OUT_DEG	1	R/W	VBUS Absent Falling Deglitch Time ($t_{VBUS_OUT_DEG}$) Setting Bit 0 = 10ms 1 = 20ms (default)	Hard-reset or REG_RST
D[2]	IBUS_RCP_DEG	0	R/W	IBUS RCP Protection Deglitch Time ($t_{IBUS_RCP_DEG}$) Setting Bit for Forward Mode 0 = 500ns (default) 1 = 4μs	Hard-reset or REG_RST
D[1]	VBUS_UVP41	1	R/W	Setting Bit of VBUS UVP Protection Falling Threshold for Forward 4:1 Mode 0 = 12V 1 = 13V (default)	Hard-reset or REG_RST
D[0]	VBUS_UVP21	1	R/W	Setting Bit of VBUS UVP Protection Falling Threshold for Forward 2:1 Mode 0 = 6V 1 = 6.5V (default)	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x0D: VBAT_PROT Register [reset = 0x33]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	VBAT1_OVP[2:0]	001	R/W	VBAT1 OVP Protection Rising Threshold Setting Bits $V_{BAT1_OVP_R}$ = 4.5V + VBAT1_OVP[2:0] × 100mV Offset: 4.5V Range: 4.5V (000) – 5.2V (111) Default: 4.6V (001)	Hard-reset or REG_RST
D[4]	VBAT1_OVP_DEG	1	R/W	VBAT1 OVP Protection Deglitch Time ($t_{VBAT1_OVP_DEG}$) Setting Bit 0 = 100ns 1 = 128μs (default)	Hard-reset or REG_RST
D[3:1]	VBAT2_OVP[2:0]	001	R/W	VBAT2 OVP Protection Rising Threshold Setting Bits $V_{BAT2_OVP_R}$ = 4.5V + VBAT2_OVP[2:0] × 100mV Offset: 4.5V Range: 4.5V (000) – 5.2V (111) Default: 4.6V (001)	Hard-reset or REG_RST
D[0]	VBAT2_OVP_DEG	1	R/W	VBAT2 OVP Protection Deglitch Time ($t_{VBAT2_OVP_DEG}$) Setting Bit 0 = 100ns 1 = 128μs (default)	Hard-reset or REG_RST

REG0x0E: IBAT_PROT Register [reset = 0x44]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	IBAT_OCP[3:0]	0100	R/W	IBAT Bidirectional OCP Protection Threshold Setting Bits 0000 = 5A 0001 = 5.5A 0010 = 6A 0011 = 6.5A 0100 = 8.5A (default) 0101 = 9A 0110 = 9.5A 0111 = 10A 1000 = 11A 1001 = 12A 1010 = 12.5A 1011 = 13A 1100 = 13.5A 1101 = 14A 1110 = 14.5A 1111 = 15A	Hard-reset or REG_RST
D[3:2]	IBAT_RSNS[1:0]	01	R/W	External IBAT Current Sense Resistor Setting Bits 00 = 0.5mΩ 01 = 1mΩ (default) 10 = 2mΩ 11 = Reserved	Hard-reset or REG_RST
D[1]	IBAT_RSNS_POS	0	R/W	External IBAT Current Sense Resistor Position Setting Bit 0 = Low-side (default) 1 = High-side	Hard-reset or REG_RST
D[0]	Reserved	0	R	Reserved	N/A

REGISTER AND DATA (continued)

REG0x0F: PULLDOWN_CTRL Register [reset = 0x80]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBAT_OCP_DEG	1	R/W	IBAT Bidirectional OCP Protection Deglitch Time ($t_{IBAT_OCP_DEG}$) Setting Bit 0 = 0.1ms 1 = 1ms (default)	Hard-reset or REG_RST
D[6]	VUSB_PDN_EN	0	R/WC	VUSB Pull-Down Resistor Enable Bit 0 = Pull-down disabled (default) 1 = Pull-down enabled. When enabled, the VUSB is pulled down by 0.5kΩ R_{PDN_VUSB} for 512ms and then this bit is automatically reset to 0.	N/A
D[5]	VWPC_PDN_EN	0	R/WC	VWPC Pull-Down Resistor Enable Bit 0 = Pull-down disabled (default) 1 = Pull-down enabled. When enabled, the VWPC is pulled down by 0.5kΩ R_{PDN_VWPC} for 512ms and then this bit is automatically reset to 0.	N/A
D[4]	VBUS_PDN_EN	0	R/WC	VBUS Pull-Down Resistor Enable Bit 0 = Pull-down disabled (default) 1 = Pull-down enabled. When enabled, the VBUS is pulled down by 5.5kΩ R_{PDN_VBUS} for 512ms and then this bit is automatically reset to 0.	N/A
D[3]	USBGATE_CTRL	0	R/W	USBGATE Control Bit 0 = USBGATE output low (default) 1 = USBGATE output high Only valid when both USBGATE_EN and USBGATE_MODE bits are set to 1. When USBGATE_EN or USBGATE_MODE bit is set to 0, USBGATE_CTRL bit is auto reset to 0.	Hard-reset or REG_RST
D[2]	WPCGATE_CTRL	0	R/W	WPCGATE Control Bit 0 = WPCGATE output low (default) 1 = WPCGATE output high Only valid when both WPCGATE_EN and WPCGATE_MODE bits are set to 1. When WPCGATE_EN or WPCGATE_MODE bit is set to 0, WPCGATE_CTRL bit is auto reset to 0.	Hard-reset or REG_RST
D[1]	USBGATE_STAT	0	R	Status Bit of USBGATE Driver This status bit indicates the real-time ON/OFF status of the USBGATE driver. 0 = USBGATE is turned off. 1 = USBGATE is turned on.	N/A
D[0]	WPCGATE_STAT	0	R	Status Bit of WPCGATE Driver This status bit indicates the real-time ON/OFF status of the WPCGATE driver. 0 = WPCGATE is turned off. 1 = WPCGATE is turned on.	N/A

REGISTER AND DATA (continued)

REG0x11: FLT_FLAG1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VUSB_OVP_FLAG	0	RC	VUSB OVP Fault Flag Bit 0 = No VUSB OVP fault 1 = VUSB OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VUSB OVP fault is cleared, a read on this bit will reset it to 0.	N/A
D[6]	VUSB_PDN_FLAG	0	RC	VUSB Pull-Down Event Flag Bit 0 = No VUSB pull-down event 1 = VUSB pull-down event has occurred. It generates an interrupt on nINT pin if unmasked. After the VUSB pull-down event is complete, a read on this bit will reset it to 0.	Hard-reset
D[5]	VWPC_OVP_FLAG	0	RC	VWPC OVP Fault Flag Bit 0 = No VWPC OVP fault 1 = VWPC OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VWPC OVP fault is cleared, a read on this bit will reset it to 0.	N/A
D[4]	VWPC_PDN_FLAG	0	RC	VWPC Pull-Down Event Flag Bit 0 = No VWPC pull-down event 1 = VWPC pull-down event has occurred. It generates an interrupt on nINT pin if unmasked. After the VWPC pull-down event is complete, a read on this bit will reset it to 0.	Hard-reset
D[3]	VBUS_OVP_FLAG	0	RC	VBUS OVP Fault Flag Bit 0 = No VBUS OVP fault 1 = VBUS OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS OVP fault is cleared, a read on this bit will reset it to 0. Note: Including VBUS_OVP41, VBUS_OVP21 and VBUS_OVP11 protections.	N/A
D[2]	VBUS_PDN_FLAG	0	RC	VBUS Pull-Down Event Flag Bit 0 = No VBUS pull-down event 1 = VBUS pull-down event has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS pull-down event is complete, a read on this bit will reset it to 0.	Hard-reset
D[1]	VUSB_ABSENT_FLAG	0	RC	VUSB Absent Event Flag Bit 0 = No VUSB absent event 1 = VUSB absent event has occurred. It generates an interrupt on nINT pin if unmasked. After the VUSB is present, a read on this bit will reset it to 0.	N/A
D[0]	VWPC_ABSENT_FLAG	0	RC	VWPC Absent Event Flag Bit 0 = No VWPC absent event 1 = VWPC absent event has occurred. It generates an interrupt on nINT pin if unmasked. After the VWPC is present, a read on this bit will reset it to 0.	N/A

REGISTER AND DATA (continued)

REG0x12: FLT_MASK1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VUSB_OVP_MASK	0	R/W	Mask VUSB OVP Fault Interrupt 0 = VUSB OVP fault interrupt can work (default) 1 = Mask VUSB OVP fault interrupt. VUSB_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[6]	VUSB_PDN_MASK	0	R/W	Mask VUSB Pull-Down Event Interrupt 0 = VUSB pull-down event interrupt can work (default) 1 = Mask VUSB pull-down event interrupt. VUSB_PDN_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[5]	VWPC_OVP_MASK	0	R/W	Mask VWPC OVP Fault Interrupt 0 = VWPC OVP fault interrupt can work (default) 1 = Mask VWPC OVP fault interrupt. VWPC_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[4]	VWPC_PDN_MASK	0	R/W	Mask VWPC Pull-Down Event Interrupt 0 = VWPC pull-down event interrupt can work (default) 1 = Mask VWPC pull-down event interrupt. VWPC_PDN_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[3]	VBUS_OVP_MASK	0	R/W	Mask VBUS OVP Fault Interrupt 0 = VBUS OVP fault interrupt can work (default) 1 = Mask VBUS OVP fault interrupt. VBUS_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[2]	VBUS_PDN_MASK	0	R/W	Mask VBUS Pull-Down Event Interrupt 0 = VBUS pull-down event interrupt can work (default) 1 = Mask VBUS pull-down event interrupt. VBUS_PDN_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[1]	VUSB_ABSENT_MASK	0	R/W	Mask VUSB Absent Event Interrupt 0 = VUSB Absent event interrupt can work (default) 1 = Mask VUSB Absent event interrupt. VUSB_ABSENT_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[0]	VWPC_ABSENT_MASK	0	R/W	Mask VWPC Absent Event Interrupt 0 = VWPC Absent event interrupt can work (default) 1 = Mask VWPC Absent event interrupt. VWPC_ABSENT_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x13: FLT_FLAG2 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VUSB2VOUT_OVP_FLAG	0	RC	VUSB2VOUT OVP Fault Flag Bit for Forward Mode 0 = No VUSB2VOUT OVP fault 1 = VUSB2VOUT OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[6]	VWPC2VOUT_OVP_FLAG	0	RC	VWPC2VOUT OVP Fault Flag Bit for Forward Mode 0 = No VWPC2VOUT OVP fault 1 = VWPC2VOUT OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[5]	PMID2VOUT_UVP_FLAG	0	RC	PMID2VOUT UVP Fault Flag Bit 0 = No PMID2VOUT UVP fault 1 = PMID2VOUT UVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[4]	PMID2VOUT_OVP_FLAG	0	RC	PMID2VOUT OVP Fault Flag Bit 0 = No PMID2VOUT OVP fault 1 = PMID2VOUT OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[3]	IBUS_OCP41_FLAG	0	RC	IBUS OCP Fault Flag Bit for Forward 4:1 Mode 0 = No IBUS OCP fault 1 = IBUS OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[2]	IBUS_OCP21_FLAG	0	RC	IBUS OCP Fault Flag Bit for Forward 2:1 Mode and Forward 1:1 Mode 0 = No IBUS OCP fault 1 = IBUS OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[1]	IBUS_OCP14_FLAG	0	RC	IBUS OCP Fault Flag Bit for Reverse 1:4 Mode 0 = No IBUS OCP fault 1 = IBUS OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[0]	IBUS_OCP12_FLAG	0	RC	IBUS OCP Fault Flag Bit for Reverse 1:2 Mode and Reverse 1:1 Mode 0 = No IBUS OCP fault 1 = IBUS OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset

REGISTER AND DATA (continued)

REG0x14: FLT_MASK2 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VUSB2VOUT_OVP_MASK	0	R/W	Mask VUSB2VOUT OVP Fault Interrupt for Forward Mode 0 = VUSB2VOUT OVP fault interrupt can work (default) 1 = Mask VUSB2VOUT OVP fault interrupt. VUSB2VOUT_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[6]	VWPC2VOUT_OVP_MASK	0	R/W	Mask VWPC2VOUT OVP Fault Interrupt for Forward Mode 0 = VWPC2VOUT OVP fault interrupt can work (default) 1 = Mask VWPC2VOUT OVP fault interrupt. VWPC2VOUT_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[5]	PMID2VOUT_UVP_MASK	0	R/W	Mask PMID2VOUT UVP Fault Interrupt 0 = PMID2VOUT UVP fault interrupt can work (default) 1 = Mask PMID2VOUT UVP fault interrupt. PMID2VOUT_UVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[4]	PMID2VOUT_OVP_MASK	0	R/W	Mask PMID2VOUT OVP Fault Interrupt 0 = PMID2VOUT OVP fault interrupt can work (default) 1 = Mask PMID2VOUT OVP fault interrupt. PMID2VOUT_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[3]	IBUS_OCP41_MASK	0	R/W	Mask IBUS OCP Fault Interrupt for Forward 4:1 Mode 0 = IBUS OCP fault interrupt can work (default) 1 = Mask IBUS OCP fault interrupt. IBUS_OCP41_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[2]	IBUS_OCP21_MASK	0	R/W	Mask IBUS OCP Fault Interrupt for Forward 2:1 Mode and 1:1 Mode 0 = IBUS OCP fault interrupt can work (default) 1 = Mask IBUS OCP fault interrupt. IBUS_OCP21_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[1]	IBUS_OCP14_MASK	0	R/W	Mask IBUS OCP Fault Interrupt for Reverse 1:4 Mode 0 = IBUS OCP fault interrupt can work (default) 1 = Mask IBUS OCP fault interrupt. IBUS_OCP14_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[0]	IBUS_OCP12_MASK	0	R/W	Mask IBUS OCP Fault Interrupt for Reverse 1:2 Mode and 1:1 Mode 0 = IBUS OCP fault interrupt can work (default) 1 = Mask IBUS OCP fault interrupt. IBUS_OCP12_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x15: FLT_FLAG3 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBAT1_OVP_FLAG	0	RC	VBAT1 OVP Fault Flag 0 = No VBAT1 OVP fault 1 = VBAT1 OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VBAT1 OVP fault is cleared, reading this bit will reset it to 0.	N/A
D[6]	VBAT2_OVP_FLAG	0	RC	VBAT2 OVP Fault Flag 0 = No VBAT2 OVP fault 1 = VBAT2 OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VBAT2 OVP fault is cleared, reading this bit will reset it to 0.	N/A
D[5]	IBAT_OCP_FLAG	0	RC	IBAT Bidirectional OCP Fault Flag 0 = No IBAT OCP fault 1 = IBAT OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[4]	OVPFET_SS_ TIMEOUT_FLAG	0	RC	External OVPFETs (Q_{USB}/Q_{WPC}) Soft-start Timeout Fault Flag 0 = No OVPFET soft-start timeout fault 1 = OVPFET soft-start timeout fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will be reset it to 0.	N/A
D[3:2]	Reserved	00	R	Reserved	N/A
D[1]	TDIE_OTP_FLAG	0	RC	TDIE Over-Temperature Fault Flag 0 = No TDIE over-temperature fault 1 = TDIE over-temperature fault has occurred. It generates an interrupt on nINT pin if unmasked. After the TDIE over-temperature fault is cleared, reading this bit will reset it to 0.	N/A
D[0]	VOUT_OVP_FLAG	0	RC	VOUT OVP Fault Flag 0 = No VOUT OVP fault 1 = VOUT OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VOUT OVP fault is cleared, reading this bit will reset it to 0.	N/A

REGISTER AND DATA (continued)

REG0x16: FLT_MASK3 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBAT1_OVP_MASK	0	R/W	Mask VBAT1 OVP Fault Interrupt 0 = VBAT1 OVP fault interrupt can work (default) 1 = Mask VBAT1 OVP fault interrupt. VBAT1_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[6]	VBAT2_OVP_MASK	0	R/W	Mask VBAT2 OVP Fault Interrupt 0 = VBAT2 OVP fault interrupt can work (default) 1 = Mask VBAT2 OVP fault interrupt. VBAT2_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[5]	IBAT_OCP_MASK	0	R/W	Mask IBAT Bidirectional OCP Fault Interrupt 0 = IBAT OCP fault interrupt can work (default) 1 = Mask IBAT OCP fault interrupt. IBAT_OCP_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[4]	OVPFET_SS_ TIMEOUT_MASK	0	R/W	Mask OVPFETs (Q_{USB}/Q_{WPC}) Soft-start Timeout Fault Interrupt 0 = OVPFET soft-start timeout fault interrupt can work (default) 1 = Mask OVPFET soft-start timeout fault interrupt. OVPFET_SS_TIMEOUT_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[3:2]	Reserved	00	R	Reserved	N/A
D[1]	TDIE_OTP_MASK	0	R/W	Mask TDIE OTP Fault Interrupt 0 = TDIE OTP fault interrupt can work (default) 1 = Mask TDIE OTP fault interrupt. TDIE_OTP_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[0]	VOUT_OVP_MASK	0	R/W	Mask VOUT OVP Fault Interrupt 0 = VOUT OVP fault interrupt can work (default) 1 = Mask VOUT OVP fault interrupt. VOUT_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x17: FLT_FLAG4 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	PEAK_OCP_QSW_FLAG	0	RC	Switching FETs Bidirectional Peak OCP Fault Flag Bit 0 = No switching FETs peak OCP fault 1 = Switching FETs peak OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[5]	IBUS_UCP_FALL_FLAG	0	RC	IBUS UCP Falling Fault Flag Bit 0 = No IBUS UCP falling fault 1 = IBUS UCP falling fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[4]	IBUS_RCP_FLAG	0	RC	IBUS RCP Fault Flag Bit for Forward Mode 0 = No IBUS RCP fault 1 = IBUS RCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[3]	VBUS_UVP41_FLAG	0	RC	VBUS UVP Fault Flag Bit for Forward 4:1 Mode 0 = No VBUS UVP fault 1 = VBUS UVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS UVP fault is cleared, reading this bit will reset it to 0.	Hard-reset
D[2]	VBUS_UVP21_FLAG	0	RC	VBUS UVP Fault Flag Bit for Forward 2:1 Mode 0 = No VBUS UVP fault 1 = VBUS UVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS UVP fault is cleared, reading this bit will reset it to 0.	Hard-reset
D[1]	VUSB_INSERT_FLAG	0	RC	VUSB Insert Event Flag Bit 0 = No VUSB insert event 1 = VUSB insert event has occurred. It generates an interrupt on nINT pin if unmasked. After the VUSB is removed, reading this bit will reset it to 0.	N/A
D[0]	VWPC_INSERT_FLAG	0	RC	VWPC Insert Event Flag Bit 0 = No VWPC insert event 1 = VWPC insert event has occurred. It generates an interrupt on nINT pin if unmasked. After the VWPC is removed, reading this bit will reset it to 0.	N/A

REGISTER AND DATA (continued)

REG0x18: FLT_MASK4 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	PEAK_OCP_QSW_MASK	0	R/W	Mask Switching FETs Peak OCP Fault Interrupt 0 = Switching FETs peak OCP fault interrupt can work (default) 1 = Mask switching FETs peak OCP fault interrupt. PEAK_OCP_QSW_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[5]	IBUS_UCP_FALL_MASK	0	R/W	Mask IBUS UCP Falling Fault Interrupt 0 = IBUS UCP falling fault interrupt can work (default) 1 = Mask IBUS UCP falling fault interrupt. IBUS_UCP_FALL_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[4]	IBUS_RCP_MASK	0	R/W	Mask IBUS RCP Fault Interrupt for Forward Mode 0 = IBUS RCP fault interrupt can work (default) 1 = Mask IBUS RCP fault interrupt. IBUS_RCP_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[3]	VBUS_UVP41_MASK	0	R/W	Mask VBUS UVP Fault Interrupt for Forward 4:1 Mode 0 = VBUS UVP fault interrupt can work (default) 1 = Mask VBUS UVP fault interrupt. VBUS_UVP41_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[2]	VBUS_UVP21_MASK	0	R/W	Mask VBUS UVP Fault Interrupt for Forward 2:1 Mode 0 = VBUS UVP fault interrupt can work (default) 1 = Mask VBUS UVP fault interrupt. VBUS_UVP21_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[1]	VUSB_INSERT_MASK	0	R/W	Mask VUSB Insert Event Interrupt 0 = VUSB insert event interrupt can work (default) 1 = Mask VUSB insert event interrupt. VUSB_INSERT_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[0]	VWPC_INSERT_MASK	0	R/W	Mask VWPC Insert Event Interrupt 0 = VWPC insert event interrupt can work (default) 1 = Mask VWPC insert event interrupt. VWPC_INSERT_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x19: FLT_FLAG5 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_PRESENT_FLAG	0	RC	VBUS Present Event Flag Bit 0 = No VBUS present event 1 = VBUS present event has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS is absent, reading this bit will reset it to 0.	N/A
D[6]	VBAT_INSERT_FLAG	0	RC	VBAT Insert Event Flag Bit 0 = No VBAT insert event 1 = VBAT insert event has occurred. It generates an interrupt on nINT pin if unmasked. After the battery is absent, reading this bit will reset it to 0.	N/A
D[5]	WD_TIMEOUT_FLAG	0	RC	Watchdog Timeout Fault Flag Bit 0 = No watchdog timeout fault 1 = Watchdog timeout fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[4]	VBUS_ABSENT_FLAG	0	RC	VBUS Absent Event Flag Bit 0 = No VBUS absent event 1 = VBUS absent event has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS is present, a read on this bit will reset it to 0.	N/A
D[3]	IBUS_UCP_TIMEOUT_FLAG	0	RC	IBUS UCP Timeout Fault Flag Bit 0 = No IBUS UCP timeout fault 1 = IBUS UCP timeout fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will be reset it to 0.	Hard-reset
D[2]	ADC_DONE_FLAG	0	RC	ADC Conversion Complete Event Flag Bit In 1-shot conversion mode, this bit is set to 1 after ADC conversion of all enabled channels is complete. 0 = Normal 1 = ADC conversion complete. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	Hard-reset
D[1]	PIN_DIAG_FLAG	0	RC	Pin Diagnosis Fail Fault Flag Bit 0 = Normal 1 = C_{FLY} short/open or VOUT pin short fault has occurred. It generates an interrupt on nINT pin. Reading this bit will reset it to 0.	N/A
D[0]	VBAT_BRN_OUT_FLAG	0	RC	VBAT Brown-Out Fault Flag Bit for Reverse Mode 0 = No VBAT brown-out fault 1 = VBAT brown-out fault has occurred. It generates an interrupt on nINT pin if unmasked. After V_{VOUT} rises above $V_{BAT_BRN_IN}$, a read on this bit will reset it to 0.	N/A

REGISTER AND DATA (continued)

REG0x1A: FLT_MASK5 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_PRESENT_MASK	0	R/W	Mask VBUS Present Event Interrupt 0 = VBUS present event interrupt can work (default) 1 = Mask VBUS present event interrupt. VBUS_PRESENT_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[6]	VBAT_INSERT_MASK	0	R/W	Mask VBAT Insert Event Interrupt 0 = VBAT insert event interrupt can work (default) 1 = Mask VBAT insert event interrupt. VBAT_INSERT_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[5]	WD_TIMEOUT_MASK	0	R/W	Mask Watchdog Timeout Fault Interrupt 0 = Watchdog timeout fault interrupt can work (default) 1 = Mask watchdog timeout fault interrupt. WD_TIMEOUT_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[4]	VBUS_ABSENT_MASK	0	R/W	Mask VBUS Absent Event Interrupt 0 = VBUS Absent event interrupt can work (default) 1 = Mask VBUS Absent event interrupt. VBUS_ABSENT_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[3]	IBUS_UCP_TIMEOUT_MASK	0	R/W	Mask IBUS UCP Timeout Fault Interrupt 0 = IBUS UCP timeout fault interrupt can work (default) 1 = Mask IBUS UCP timeout fault interrupt. IBUS_UCP_TIMEOUT_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[2]	ADC_DONE_MASK	0	R/W	Mask ADC Complete Event Interrupt 0 = ADC_DONE event interrupt can work (default) 1 = Mask ADC_DONE event interrupt. ADC_DONE_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[1]	PIN_DIAG_MASK	0	R/W	Mask Pin Diagnosis Fail Fault Interrupt 0 = Pin diagnosis fail fault interrupt can work (default) 1 = Mask pin diagnosis fail fault interrupt. PIN_DIAG_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[0]	VBAT_BRN_OUT_MASK	0	R/W	Mask VBAT Brown-Out Fault Interrupt for Reverse Mode 0 = VBAT brown-out fault interrupt can work (default) 1 = Mask VBAT brown-out fault interrupt. VBAT_BRN_OUT_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x1B: FLT_FLAG6 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VUSBOVP_ALM_FLAG	0	RC	VUSB OVP Alarm Flag Bit for Forward Mode 0 = No VUSB OVP alarm 1 = VUSB OVP alarm has occurred. It generates an interrupt on nINT pin if unmasked. After the VUSB OVP alarm is cleared, reading this bit will reset it to 0.	Hard-reset
D[6]	VWPCOVP_ALM_FLAG	0	RC	VWPC OVP Alarm Flag for Forward Mode 0 = No VWPC OVP alarm 1 = VWPC OVP alarm has occurred. It generates an interrupt on nINT pin if unmasked. After the VWPC OVP alarm is cleared, reading this bit will reset it to 0.	Hard-reset
D[5]	TDIEOTP_ALM_FLAG	0	RC	TDIE OTP Alarm Flag Bit 0 = No TDIE OTP alarm 1 = TDIE OTP alarm has occurred. It generates an interrupt on nINT pin if unmasked. After the TDIE OTP alarm is cleared, reading this bit will reset it to 0.	Hard-reset
D[4]	VBUS_LO_FLAG	0	RC	VBUS Low Voltage Fault Flag Bit Only valid in forward mode before switching start. It is set to 1 if (V_{VBUS}/n - V_{VOUT}) is below - 0.01V_{VOUT}. (n = 1, 2, or 4, depending on the operation mode) 0 = No VBUS low voltage fault 1 = Device in VBUS low voltage fault has occurred. It generates an interrupt on nINT pin. After the VBUS low voltage fault is cleared, reading this bit will reset it to 0.	Hard-reset or REG_RST
D[3]	VBUS_HI_FLAG	0	RC	VBUS High Voltage Fault Flag Bit Only valid in forward mode before switching start. It is set to 1 if (V_{VBUS}/n - V_{VOUT}) is above 0.15V_{VOUT}. (n = 1, 2, or 4, depending on the operation mode) 0 = No VBUS high voltage fault 1 = Device in VBUS high voltage fault has occurred. It generates an interrupt on nINT pin. After the VBUS high voltage fault is cleared, reading this bit will reset it to 0.	Hard-reset or REG_RST
D[2]	VBAT1OVP_ALM_FLAG	0	RC	VBAT1 OVP Alarm Flag Bit 0 = No VBAT1 OVP alarm 1 = VBAT1 OVP alarm has occurred. It generates an interrupt on nINT pin if unmasked. After the VBAT1 OVP alarm is cleared, reading this bit will reset it to 0.	Hard-reset
D[1]	VBAT2OVP_ALM_FLAG	0	RC	VBAT2 OVP Alarm Flag Bit 0 = No VBAT2 OVP alarm 1 = VBAT2 OVP alarm has occurred. It generates an interrupt on nINT pin if unmasked. After the VBAT2 OVP alarm is cleared, reading this bit will reset it to 0.	Hard-reset
D[0]	IBATOCP_ALM_FLAG	0	RC	IBAT OCP Alarm Flag Bit for Forward Mode 0 = No IBAT OCP alarm 1 = IBAT OCP alarm has occurred. It generates an interrupt on nINT pin if unmasked. After the IBAT OCP alarm is cleared, reading this bit will reset it to 0.	Hard-reset

REGISTER AND DATA (continued)

REG0x1C: FLT_MASK6 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VUSBOVP_ALM_MASK	0	R/W	Mask VUSB OVP Alarm Interrupt 0 = VUSB OVP alarm interrupt can work (default) 1 = Mask VUSB OVP alarm interrupt. VUSBOVP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[6]	VWPCOVP_ALM_MASK	0	R/W	Mask VWPC OVP Alarm Interrupt 0 = VWPC OVP alarm interrupt can work (default) 1 = Mask VWPC OVP alarm interrupt. VWPCOVP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[5]	TDIEOTP_ALM_MASK	0	R/W	Mask TDIE OTP Alarm Interrupt 0 = TDIE OTP alarm interrupt can work (default) 1 = Mask TDIE OTP alarm interrupt. TDIEOTP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[4]	VBUS_LO_MASK	0	R/W	Mask VBUS Low Voltage Fault Interrupt 0 = VBUS low voltage fault interrupt can work (default) 1 = Mask VBUS low voltage fault interrupt. VBUS_LO_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[3]	VBUS_HI_MASK	0	R/W	Mask VBUS High Voltage Fault Interrupt 0 = VBUS high voltage fault interrupt can work (default) 1 = Mask VBUS high voltage fault interrupt. VBUS_HI_FLAG bit is set after the fault, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[2]	VBAT1OVP_ALM_MASK	0	R/W	Mask VBAT1 OVP Alarm Interrupt 0 = VBAT1 OVP alarm interrupt can work (default) 1 = Mask VBAT1 OVP alarm interrupt. VBAT1OVP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[1]	VBAT2OVP_ALM_MASK	0	R/W	Mask VBAT2 OVP Alarm Interrupt 0 = VBAT2 OVP alarm interrupt can work (default) 1 = Mask VBAT2 OVP alarm interrupt. VBAT2OVP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST
D[0]	IBATOCP_ALM_MASK	0	R/W	Mask IBAT OCP Alarm Interrupt for Forward Mode 0 = IBAT OCP alarm interrupt can work (default) 1 = Mask IBAT OCP alarm interrupt. IBATOCP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x1D: VBATOVP_ALM Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	VBAT1OVP_ALM[1:0]	00	R/W	VBAT1 OVP Alarm Rising Threshold Setting Bits $V_{BAT1OVP_ALM_R} = V_{BAT1_OVP_R}$ - (VBAT1OVP_ALM[1:0] + 1) × 50mV 00 = $V_{BAT1_OVP_R}$ - 50mV (default) 01 = $V_{BAT1_OVP_R}$ - 100mV 10 = $V_{BAT1_OVP_R}$ - 150mV 11 = $V_{BAT1_OVP_R}$ - 200mV	Hard-reset or REG_RST
D[5:4]	VBAT2OVP_ALM[1:0]	00	R/W	VBAT2 OVP Alarm Rising Threshold Setting Bits $V_{BAT2OVP_ALM_R} = V_{BAT2_OVP_R}$ - (VBAT2OVP_ALM[1:0] + 1) × 50mV 00 = $V_{BAT2_OVP_R}$ - 50mV (default) 01 = $V_{BAT2_OVP_R}$ - 100mV 10 = $V_{BAT2_OVP_R}$ - 150mV 11 = $V_{BAT2_OVP_R}$ - 200mV	Hard-reset or REG_RST
D[3:2]	IBATOCP_ALM[1:0]	00	R/W	IBAT OCP Alarm Rising Threshold Setting Bits for Forward Mode $I_{BATOCP_ALM_R} = I_{BAT_OCP}$ - 200mA - IBATOCP_ALM[1:0] × 100mA 00 = I_{BAT_OCP} - 200mA (default) 01 = I_{BAT_OCP} - 300mA 10 = I_{BAT_OCP} - 400mA 11 = I_{BAT_OCP} - 500mA	Hard-reset or REG_RST
D[1:0]	Reserved	00	R	Reserved	N/A

REGISTER AND DATA (continued)

REG0x20: ADC_CTRL1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_EN	0	R/W	ADC Conversion Enable Bit 0 = Disabled (default) 1 = Enabled Note: In 1-shot mode when the selected channel conversions are complete, the ADC_EN bit is automatically reset to 0. All channel conversions can be enabled even when the device is not during switching.	Hard-reset or REG_RST or WDT
D[6]	ADC_RATE	0	R/W	ADC Conversion Mode Control Bit 0 = Continuous conversion (default) 1 = 1-shot conversion	Hard-reset or REG_RST
D[5]	VBUS_ADC_DIS	0	R/W	VBUS ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST
D[4]	VUSB_ADC_DIS	0	R/W	VUSB ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST
D[3]	VWPC_ADC_DIS	0	R/W	VWPC ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST
D[2]	IBUS_ADC_DIS	0	R/W	IBUS ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST
D[1:0]	Reserved	00	R	Reserved	N/A

REG0x21: ADC_CTRL2 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBAT1_ADC_DIS	0	R/W	VBAT1 ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST
D[6]	VBAT2_ADC_DIS	0	R/W	VBAT2 ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST
D[5]	VOUT_ADC_DIS	0	R/W	VOUT ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST
D[4]	IBAT_ADC_DIS	0	R/W	IBAT ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST
D[3]	TDIE_ADC_DIS	0	R/W	TDIE ADC Control Bit 0 = Enable conversion (default) 1 = Disable conversion	Hard-reset or REG_RST
D[2]	Reserved	0	R	Reserved	N/A
D[1:0]	ADC_AVG[1:0]	00	R/W	Average Times of ADC Sampling 00 = 1 time (default) 01 = 2 times 10 = 4 times 11 = 8 times	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x22: VBUS_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VBUS_ADC[11:8]	0000	R	Higher 4 bits of the 12-bit ADC VBUS Data (6mV resolution) MSB<3:0>: 12288mV, 6144mV, 3072mV, 1536mV	Hard-reset or REG_RST

REG0x23: VBUS_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBUS_ADC[7:0]	0000 0000	R	Low Byte of the 12-bit ADC VBUS Data (6mV resolution) LSB<7:0>: 768mV, 384mV, 192mV, 96mV, 48mV, 24mV, 12mV, 6mV	Hard-reset or REG_RST

REG0x24: VUSB_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VUSB_ADC[11:8]	0000	R	Higher 4 bits of the 12-bit ADC VUSB Data (6mV resolution) MSB<3:0>: 12288mV, 6144mV, 3072mV, 1536mV	Hard-reset or REG_RST

REG0x25: VUSB_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VUSB_ADC[7:0]	0000 0000	R	Low Byte of the 12-bit ADC VUSB Data (6mV resolution) LSB<7:0>: 768mV, 384mV, 192mV, 96mV, 48mV, 24mV, 12mV, 6mV	Hard-reset or REG_RST

REG0x26: VWPC_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VWPC_ADC[11:8]	0000	R	Higher 4 bits of the 12-bit ADC VWPC Data (6mV resolution) MSB<3:0>: 12288mV, 6144mV, 3072mV, 1536mV	Hard-reset or REG_RST

REG0x27: VWPC_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VWPC_ADC[7:0]	0000 0000	R	Low Byte of the 12-bit ADC VWPC Data (6mV resolution) LSB<7:0>: 768mV, 384mV, 192mV, 96mV, 48mV, 24mV, 12mV, 6mV	Hard-reset or REG_RST

REG0x28: IBUS_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	IBUS_ADC[12] (1)	0	R	Polarity of the 12-bit ADC IBUS Data 0 = Positive (Forward Charging) 1 = Negative (Reverse Discharging)	Hard-reset or REG_RST
D[3:0]	IBUS_ADC[11:8] (1)	0000	R	Higher 4 bits of the 12-bit ADC IBUS Data (2mA resolution) MSB<3:0>: 4096mA, 2048mA, 1024mA, 512mA	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x29: IBUS_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBUS_ADC[7:0] (1)	0000 0000	R	Low Byte of the 12-bit ADC IBUS Data (2mA resolution) LSB<7:0>: 256mA, 128mA, 64mA, 32mA, 16mA, 8mA, 4mA, 2mA	Hard-reset or REG_RST

NOTE: 1. IBUS_ADC[12:0] bits are reported in two's complement.

REG0x2E: VBAT1_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VBAT1_ADC[11:8]	0000	R	Higher 4 bits of the 12-bit ADC VBAT1 Data (2mV resolution) MSB<3:0>: 4096mV, 2048mV, 1024mV, 512mV	Hard-reset or REG_RST

REG0x2F: VBAT1_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBAT1_ADC[7:0]	0000 0000	R	Low Byte of the 12-bit ADC VBAT1 Data (2mV resolution) LSB<7:0>: 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV	Hard-reset or REG_RST

REG0x30: VBAT2_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VBAT2_ADC[11:8]	0000	R	Higher 4 bits of the 12-bit ADC VBAT2 Data (2mV resolution) MSB<3:0>: 4096mV, 2048mV, 1024mV, 512mV	Hard-reset or REG_RST

REG0x31: VBAT2_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBAT2_ADC[7:0]	0000 0000	R	Low Byte of the 12-bit ADC VBAT2 Data (2mV resolution) LSB<7:0>: 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV	Hard-reset or REG_RST

REG0x32: VOUT_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VOUT_ADC[11:8]	0000	R	Higher 4 bits of the 12-bit ADC VOUT Data (2mV resolution) MSB<3:0>: 4096mV, 2048mV, 1024mV, 512mV	Hard-reset or REG_RST

REG0x33: VOUT_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VOUT_ADC[7:0]	0000 0000	R	Low Byte of the 12-bit ADC VOUT Data (2mV resolution) LSB<7:0>: 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x34: IBAT_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	IBAT_ADC[12] (2)	0	R	Polarity of the 12-bit ADC IBAT Data 0 = Positive (Forward Charging) 1 = Negative (Reverse Discharging)	Hard-reset or REG_RST
D[3:0]	IBAT_ADC[11:8] (2)	0000	R	Higher 4 bits of the 12-bit ADC IBAT Data (4mA resolution) MSB<3:0>: 8192mA, 4096mA, 2048mA, 1024mA	Hard-reset or REG_RST

REG0x35: IBAT_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBAT_ADC[7:0] (2)	0000 0000	R	Low Byte of the 12-bit ADC IBAT Data (4mA resolution) LSB<7:0>: 512mA, 256mA, 128mA, 64mA, 32mA, 16mA, 8mA, 4mA	Hard-reset or REG_RST

NOTE: 2. IBAT_ADC[12:0] bits are reported in two's complement.

REG0x36: TDIE_ADC Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TDIE_ADC[7:0]	0000 0000	R	8-bit ADC TDIE Data (1℃ resolution) LSB<7:0>: 128℃, 64℃, 32℃, 16℃, 8℃, 4℃, 2℃, 1℃ TDIE = TDIE_ADC[7:0] × 1℃ - 40℃	Hard-reset or REG_RST

REG0x37: PROT_CTRL1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VUSB_ABSENT_DIS	0	R/W	VUSB Absent Protection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[6]	VUSB2VOUT_OVP_DIS	0	R/W	VUSB2VOUT OVP Protection Disable Bit for Forward Mode 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[5]	VUSB_OVP_DIS	0	R/W	VUSB OVP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[4]	VWPC_ABSENT_DIS	0	R/W	VWPC Absent Protection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[3]	VWPC2VOUT_OVP_DIS	0	R/W	VWPC2VOUT OVP Protection Disable Bit for Forward Mode 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[2]	VWPC_OVP_DIS	0	R/W	VWPC OVP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[1]	VBUS_OVP_DIS	0	R/W	VBUS OVP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[0]	VBUS_PK_OVP_DIS	0	R/W	VBUS Peak OVP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x38: PROT_CTRL2 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VOUT_OVP_DIS	0	R/W	VOUT OVP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5]	PEAK_OCP_QSW_DIS	0	R/W	Switching FETs Bidirectional Peak OCP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[4]	PMID2VOUT_UVP_DIS	0	R/W	PMID2VOUT UVP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[3]	PMID2VOUT_OVP_DIS	0	R/W	PMID2VOUT OVP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[2]	IBUS_OCP_DIS	0	R/W	IBUS OCP Protection Disable Bit 0 = Enabled (default) 1 = Disabled Note: Including IBUS_OCP protections of 6 SCC modes.	Hard-reset or REG_RST
D[1]	IBUS_UCP_DIS	0	R/W	IBUS UCP Protection Disable Bit 0 = Enabled (default) 1 = Disabled Note: Including IBUS_UCP_TIMEOUT and IBUS_UCP_FALL protections.	Hard-reset or REG_RST
D[0]	IBUS_RCP_DIS	0	R/W	IBUS RCP Protection Disable Bit for Forward Mode 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST

REG0x39: PROT_CTRL3 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_ABSENT_DIS	0	R/W	VBUS Absent Protection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[6]	VBUS_UVP_DIS	0	R/W	VUSB UVP Protection Disable Bit 0 = Enabled (default) 1 = Disabled Note: Including VBUS_UVP41 and VBUS_UVP21 protections.	Hard-reset or REG_RST
D[5]	VBAT1_OVP_DIS	0	R/W	VBAT1 OVP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[4]	VBAT2_OVP_DIS	0	R/W	VBAT2 OVP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[3]	IBAT_OCP_DIS	0	R/W	IBAT OCP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[2]	VUSBOVP_ALM_DIS	0	R/W	VUSB OVP Alarm Disable Bit for Forward Mode 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[1]	VWPCOVP_ALM_DIS	0	R/W	VWPC OVP Alarm Disable Bit for Forward Mode 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[0]	TDIEOTP_ALM_DIS	0	R/W	TDIE OTP Alarm Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST

REGISTER AND DATA (continued)

REG0x3A: PROT_CTRL4 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TDIE_OTP_DIS	0	R/W	TDIE OTP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[6]	VBAT_BRN_OUT_DIS	0	R/W	VBAT Brown-Out Protection Disable Bit for Reverse Mode 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[5]	VBUS_LO_DIS	0	R/W	VBUS Low Voltage Detection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[4]	VBUS_HI_DIS	0	R/W	VBUS High Voltage Detection Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[3]	VBAT1OVP_ALM_DIS	0	R/W	VBAT1 OVP Alarm Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[2]	VBAT2OVP_ALM_DIS	0	R/W	VBAT2 OVP Alarm Disable Bit 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[1]	IBATOCP_ALM_DIS	0	R/W	IBAT OCP Alarm Disable Bit for Forward Mode 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST
D[0]	CFLY_SCP_DIS	0	R/W	CFLY Short Protection Disable Bit During Switching 0 = Enabled (default) 1 = Disabled	Hard-reset or REG_RST

REG0xA1: BC1.2_FLAG Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	VUSB_CHG_FLAG	0	RC	Event Flag of VUSB Voltage Change 0 = No VUSB voltage change event 1 = VUSB voltage change event has occurred, namely that VUSB insert or absent event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[4]	USB_DEVICE_CHG_FLAG	0	RC	Event Flag of USB BC1.2 Device Status Bits Change 0 = No USB_DEVICE_STAT bits change event 1 = USB_DEVICE_STAT bits change event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	Hard-reset
D[3:0]	Reserved	0000	R	Reserved	N/A

REG0xA2: BC1.2_MASK Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	VUSB_CHG_MASK	0	R/W	Mask Interrupt of VUSB Voltage Change Event 0 = Interrupt of VUSB voltage change event can work. (default) 1 = Mask interrupt of VUSB voltage change event. VUSB_CHG_FLAG bit sets after the fault, but this bit suppresses the interrupt signal on nINT pin.	Hard-reset
D[4]	USB_DEVICE_CHG_MASK	0	R/W	Mask Interrupt of USB BC1.2 Device Status Bits Change Event 0 = Interrupt of USB_DEVICE_STAT bits change event can work. (default) 1 = Mask interrupt of USB_DEVICE_STAT bits change event. USB_DEVICE_CHG_FLAG bit sets after the fault, but this bit suppresses the interrupt signal on nINT pin.	Hard-reset
D[3:0]	Reserved	0000	R	Reserved	N/A

REGISTER AND DATA (continued)

REG0xA3: DPDM_DETC Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DPDM_DETC_EN	0	R/W	Enable Bit of DP/DM Detection for Debug 0 = Disabled (default) 1 = Enabled. The DP/DM detection results are updated every 8ms.	Hard-reset
D[6:4]	DP_RSLT[2:0]	000	R	DP Pin Voltage Detection Result Bits 000 = 0V. The DP pin voltage is in the range of 0V to 0.05V. 001 = 0.2V. The DP pin voltage is in the range of 0.15V to 0.25V. 010 = 0.6V. The DP pin voltage is in the range of 0.55V to 0.65V. 011 = 1.8V. The DP pin voltage is in the range of 1.65V to 1.95V. 100 = 3.3V. The DP pin voltage is in the range of 3V to 3.6V. 111 = Error. The DP pin voltage is not listed above. Only valid when DPDM_DETC_EN bit is set to 1.	Hard-reset
D[3]	Reserved	0	R	Reserved	N/A
D[2:0]	DM_RSLT[2:0]	000	R	DM Pin Voltage Detection Result Bits 000 = 0V. The DM pin voltage is in the range of 0V to 0.05V. 001 = 0.2V. The DM pin voltage is in the range of 0.15V to 0.25V. 010 = 0.6V. The DM pin voltage is in the range of 0.55V to 0.65V. 011 = 1.8V. The DM pin voltage is in the range of 1.65V to 1.95V. 100 = 3.3V.The DM pin voltage is in the range of 3V to 3.6V. 111 = Error. The DM pin voltage is not in the ranges listed above. Only valid when DPDM_DETC_EN bit is set to 1.	Hard-reset

REG0xA4: BC1.2_CTRL Register [reset = 0x18]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5:4]	DCD_TIMER[1:0]	01	R/W	DCD Timer $t_{DCD_TIMEOUT}$ Setting Bits 00 = The DCD detection is disabled. 01 = 600ms (default) 10 = 900ms 11 = The DCD timer is infinite. The BC1.2 detection cannot step forward until DP voltage is detected below V_{LGC_LOW}.	Hard-reset
D[3]	DCD_DELAY	1	R/W	DCD Detection Delay Time Setting Bit for BC1.2 This is delay time (t_{DCD_DLY}) from when BC1.2 is enabled and VBUS is present to when the DCD detection starts. 0 = 150ms 1 = 300ms (default)	Hard-reset
D[2]	BC_AUTO_EN	0	R/W	BC1.2 Automatic Detection Enable Bit 0 = Disabled (default) 1 = Enabled. When VBUS is present, it will automatically start BC1.2 detection.	Hard-reset
D[1:0]	Reserved	00	R	Reserved	N/A

REGISTER AND DATA (continued)

REG0xA5: DPDM_DAC Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5:4]	DP_DAC[1:0]	00	R/W	DP Pin Output Driver Voltage Setting Bits 00 = HiZ mode (default) 01 = 0V (V_{0P0_VSRC}) 10 = 0.6V (V_{0P6_VSRC}) 11 = 3.3V (V_{3P3_VSRC}) Note: The bit configurations are invalid during BC1.2 detection	Hard-reset
D[3:2]	DM_DAC[1:0]	00	R/W	DM Pin Output Driver Voltage Setting Bits 00 = HiZ mode (default) 01 = 0V (V_{0P0_VSRC}) 10 = 0.6V (V_{0P6_VSRC}) 11 = 3.3V (V_{3P3_VSRC}) Note: The bit configurations are invalid during BC1.2 detection	Hard-reset
D[1]	DPDM_DAC_EN	0	R/W	Enable Bit of DP/DM DAC 0 = Disabled (default) 1 = Enabled	Hard-reset
D[0]	Reserved	0	R	Reserved	N/A

REG0xA8: USB_STAT Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6:4]	USB_DEVICE_STAT[2:0]	000	R	Status Bit of USB BC1.2 Device Detection 000 = No Input (default) 001 = BC1.2 detection in progress 010 = SDP device detected 011 = Non-standard adapter detected 100 = DCP device detected 101 = CDP device detected 110 ~ 111 = Reserved	Hard-reset
D[3:1]	Reserved	000	R	Reserved	N/A
D[0]	DCD_TIMEOUT_FLAG	0	RC	BC1.2 DCD Timeout Fault Flag Bit 0 = No BC1.2 DCD timeout fault (default) 1 = BC1.2 DCD timeout fault has occurred. It generates an interrupt on nINT pin. Read this bit to reset it to 0.	Hard-reset

REG0xD0: MISC_CTRL1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	Reserved	0000 0	R	Reserved	N/A
D[2:1]	IBUS_OCP_R11_E[1:0]	00	R/W	Extra Bits of IBUS OCP Protection Threshold for Reverse 1:1 Mode 00 = Keep IBUS_OCP_R11[1:0] setting in REG0x0A (default) 01 = 4A 10 = 5A 11 = 6A	Hard-reset or REG_RST
D[0]	Reserved	0	R	Reserved	N/A

DETAILED DESCRIPTION

The SGM41611 is an efficient 14A battery charger that can operate in 6 different modes (forward 4:1/2:1/1:1 step-down charging modes and reverse 1:4/1:2/1:1 step-up discharging modes). A two-channel switched-capacitor core is integrated in the device to minimize the ripples and improve efficiency. Two power paths control, a reverse blocking NFET and all other necessary protection features for safe charging are included. A high speed 12-bit ADC converter is also included to provide bus voltage, bus current, battery voltage, battery current, and die temperature information for the charge management host via I²C serial interface.

Forward 4:1 Mode & Reverse 1:4 Mode

In forward 4:1 mode, ignoring small energy loss in each switching period in steady state operation, the SGM41611 generates a VOUT voltage of $V_{PMID}/4$ and is capable of supplying up to 14A output current. In reverse 1:4 operation, it generates a PMID voltage of $4V_{VOUT}$ and is capable of supplying up to 1.5A current. Each channel of the 180° interleaved switched-capacitor charger operates with a fixed 50% duty cycle and reduces the ripple on the output voltage and current. The simplified single channel 4:1/1:4 switched-capacitor charger is shown in Figure 3.

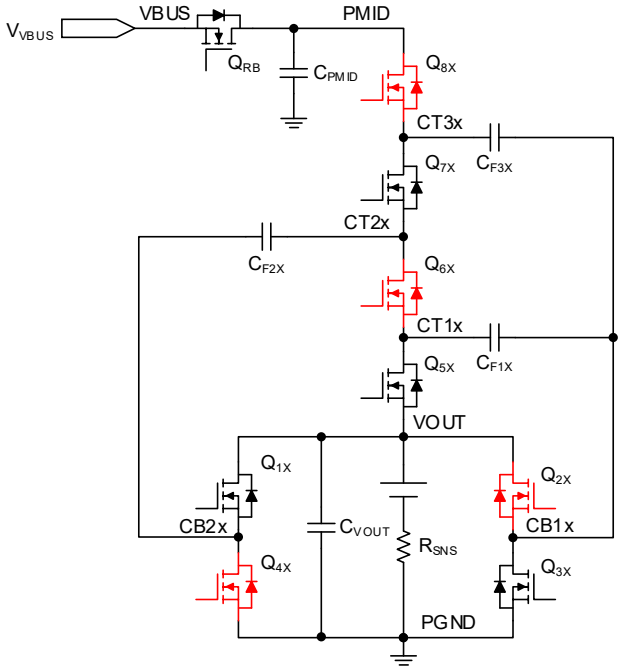


Figure 3. Power Stage of Single Channel 4:1/1:1:4 Switched-Capacitor Charger

Selecting high quality C_{FLY} capacitors and proper switching frequency are the key factors for a well performing capacitor voltage divider. Switching frequency selection is a trade-off between efficiency and capacitor size. An optimum switching frequency can be found for any selected C_{FLY} capacitor to minimize losses.

Forward 2:1 Mode & Reverse 1:2 Mode

The SGM41611 can be configured to operate in forward 2:1 mode or in reverse 1:2 mode, where $Q_{7A}/Q_{7B}/Q_{6A}/Q_{6B}$ are always on. It generates a VOUT voltage of $V_{PMID}/2$ and is capable of supplying up to 12A output current. In reverse 1:2 operation, it generates a PMID voltage of $2V_{VOUT}$ and is capable of supplying up to 3A current. Each channel of the 180° interleaved switched-capacitor charger operates with a fixed 50% duty cycle and reduces the ripple on the output voltage and current. The simplified single channel 2:1/1:2 switched-capacitor charger is shown in Figure 4.

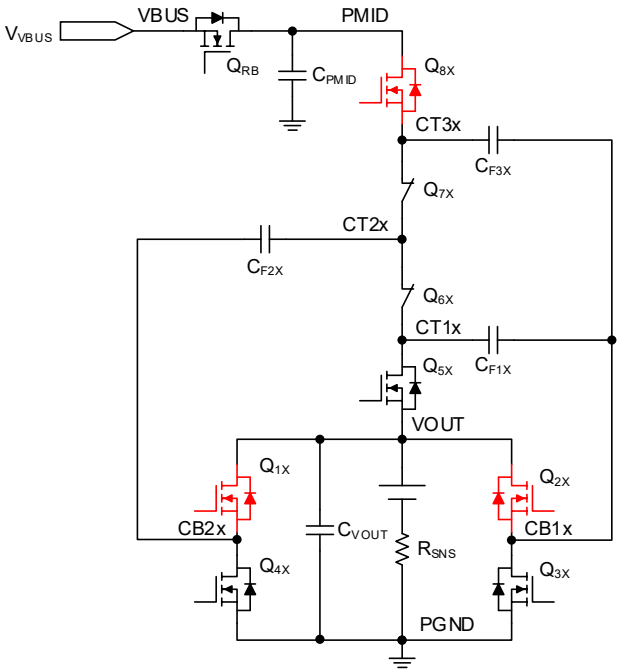


Figure 4. Power Stage of Single Channel 2:1/1:2 Switched-Capacitor Charger

DETAILED DESCRIPTION (continued)

Forward 1:1 Mode & Reverse 1:1 Mode

The SGM41611 is designed to operate in bidirectional bypass mode when V_{VBUS} is close to the V_{VOUT}. With proper settings, the device enters bypass mode, all switches between VBUS and VOUT are fully turned on, and $Q_{3A}/Q_{3B}/Q_{4A}/Q_{4B}$ are also fully turned on to provide bypass filtering, while the other switches remain off. When V_{BUS} is near V_{VOUT}, the bypass mode offers the best efficiency and the device is capable of sourcing up to 6A. The simplified single channel bypass mode switched-capacitor charger is shown in Figure 5.

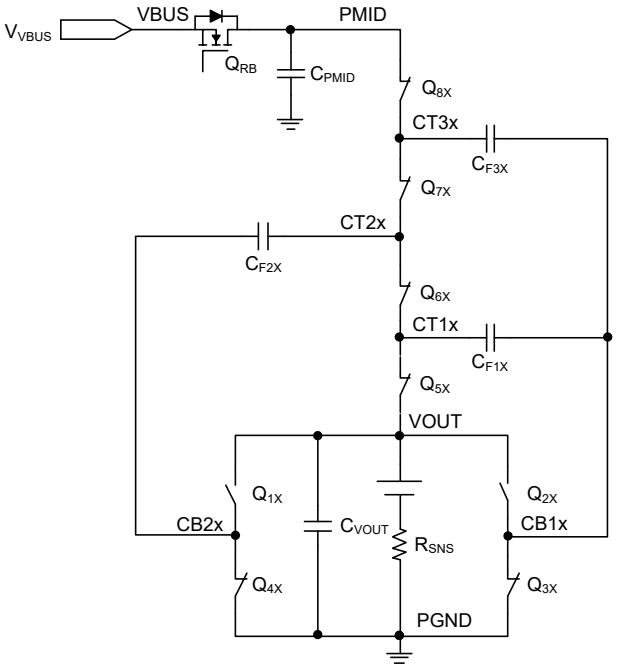


Figure 5. Power Stage of Single Channel 1:1 Switched-Capacitor Charger

The output voltage is close to the input minus a voltage drop caused by the on-resistances of the RBFET plus the four high-side switches of the two channels in parallel:

$$R_{EFF}\ (\text{Bypass mode}) \approx R_{DS_QRB} + (R_{DS_Q8A} + R_{DS_Q7A} + R_{DS_Q6A} + R_{DS_Q5A}) \,||\, (R_{DS_Q8B} + R_{DS_Q7B} + R_{DS_Q6B} + R_{DS_Q5B})$$

where R_{DS_QXX} is the on-resistance of the switch Q_{XX}.

Charge System

The SGM41611 is a slave charger device and needs a host. The host must set up all protection functions and disable the main charger before enabling the SGM41611. The host must monitor the nINT interrupts especially during high current charging. It must also communicate with the wall adapter to control the charge current.

Figure 6 shows the block diagram of a charge system using the SGM41611 along with other devices. In this system, the SGM41611 can be used to detect the adapter by USB BC1.2 and the PD controller is used to communicate with adapter by PD protocol. When the smart wall adapter is detected, the AP unit controls the switching charger (SGM41516) that powers the load system and the switched capacitor charger (SGM41611) that provides high current charging. The communication between those devices is through I²C interface.

DETAILED DESCRIPTION (continued)

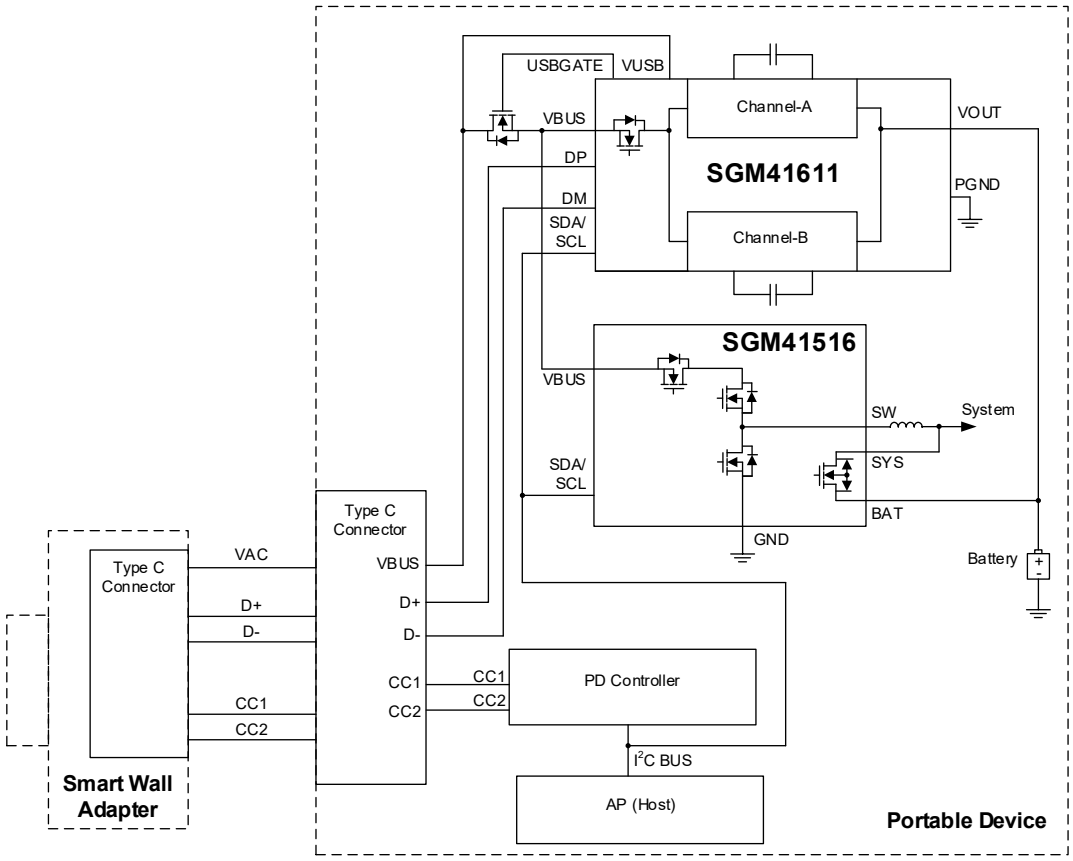


Figure 6. Simplified Charge System

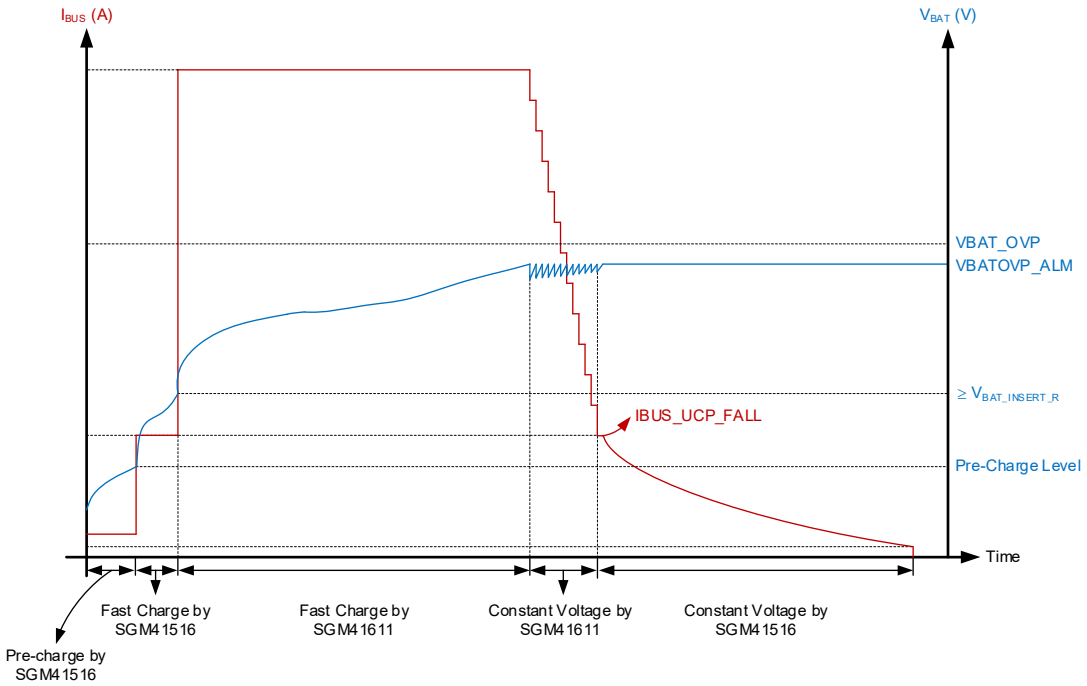


Figure 7. SGM41611 System Charging Profile

DETAILED DESCRIPTION (continued)

A typical charge profile for a high-capacity battery using switching charger and switched capacitor charger together is shown in Figure 7. During the trickle charge and pre-charge, the charging is controlled by the switching charger. Once the battery voltage reaches $V_{BAT_INSERT_R}$, the adapter can negotiate for a higher bus voltage and enable the SGM41611 for charging (4:1, 2:1 or 1:1 mode). Once the battery voltage approaches the $V_{BATxOVP_ALM}$ point, the SGM41611 will notify the AP to reduce the IBUS current, and the AP will negotiate with adapter for a lower bus voltage to effectively taper the current until a point where the IBUS current ramps down below $I_{BUS_UCP_F}$.

Startup Sequence

The SGM41611 is powered from the greater of VUSB, VWPC, VBUS or VOUT (VUSB and VWPC are used as sense input for adapter voltages as well). When V_{VOUT} rises above its UVLO rising threshold and the nLPM pin is connected to high, or V_{VUSB}, V_{VWPC} or V_{VBUS} rises above their respective UVLO rising threshold, the I²C interface is ready for communication and all the registers are reset to default values.

The device does not start charging after power-up, because by default the charger is disabled but the ADC can be enabled and the AP can read the system parameters before enabling charge. The charge can be enabled only if V_{VBUS} > $V_{BUS_PRESENT_R}$ and V_{VOUT} > $V_{BAT_INSERT_R}$.

Device Power-Up from Battery without Input Source

To reduce the quiescent current and maximize the battery run time when it is the only available source, low power mode can be set by pulling low the nLPM pin to achieve very small battery leakage. In low power mode, the REGN LDO and most of the sensing circuits are turned off, except VUSB_INSERT, VWPC_INSERT and VBUS_PRESENT functions. The SGM41611 exits low power mode when nLPM pin is pulled high or V_{VUSB}/V_{VWPC}/V_{VBUS} rises above their respective UVLO rising threshold.

Device Power-Up from Input Source

When an input source is plugged-in and the conditions of V_{VBUS} > $V_{BUS_PRESENT_R}$ and V_{VOUT} > $V_{BAT_INSERT_R}$ are valid, the AP must initialize all protections to the desired thresholds before enabling charge. The protection thresholds that need to be set are VUSB_OVP, VWPC_OVP, VUSB2VOUT_OVP, VWPC2VOUT_OVP, PMID2VOUT_OVP, PMID2VOUT_UVP, VBUS_OVP, VBUS_UVP, IBUS_OCP, IBUS_UCP, IBUS_RCP, VOUT_OVP, VBAT_OVP, IBAT_OCP, PEAK_OCP, and TDIE_OTP. If one of the protection trigger conditions is met, the charger stops switching. It will also be turned off the corresponding external OVPFETs Q_{USB} and Q_{WPC} when VUSB_OVP or VWPC_OVP or VBUS_SC event occurs.

After setting protections, the VBUS voltage is checked to be between V_{BUS_LO} and V_{BUS_HI} to allow forward charge mode operation. Charging is enabled and current flows into the battery when the AP sets forward mode by writing 000/001/010 in the SCC_MODE[2:0] bits and sets SCC_EN = 1. Then raising the VBUS voltage will increase the battery charge current. When the converter is on, any command to change the charge mode is ignored. To do so, the charging must be disabled first, and then the charge mode can be changed by I²C serial interface.

The SGM41611 can run the input source type detection if the relevant bits are set. The SGM41611 follows the USB Battery Charging Specification 1.2 (BC1.2) to detect input source (SDP/DCP/CDP) and non-standard adapter through USB D+/D- lines. When the input source type detection is complete, it will set the USB_DEVICE_CHG_FLAG bit to 1 and generate an INT pulse to notify the host. USB_DEVICE_STAT[2:0] bits will be updated to indicate USB or adaptor input source types at the same time.

REGN Management

REGN provides the power required for the analog section. When V_{VOUT} is higher than 3.3V, it is powered by VOUT instead of PMID. A 4.7μF or lager capacitor is required on the REGN pin.

Dual Input Bi-Directional Power Path Management

The SGM41611 has USBGATE and WPCGATE pins to drive two sets of back-to-back N-channel FETs, which select and manage the input power from two different input sources (such as wired and wireless input sources). If the external Q_{WPC} is not populated in the schematic, then leave VWPC, WPCGATE and WPCSUB pins floating. So is USBGATE.

For forward charging operation, USBGATE and WPCGATE can operate in two modes: auto-mode and manual mode. In reverse mode, both sets of FETs can be turned on/off manually.

DETAILED DESCRIPTION (continued)

Forward Auto-Mode

For the OVPFET forward operation, USBGATE and WPCGATE can operate in auto-mode by setting USBGATE_MODE and WPCGATE_MODE to 0. In auto-mode, USBGATE/WPCGATE is automatically turned on and off according to the VUSB/VWPC voltage. Taking USBGATE as an example, when the VUSB input source is inserted, the VUSB voltage exceeds V_{USB_INSERT} and not higher than V_{USB_OVP} thresholds, the USBGATE will be automatically turned on after $t_{USBGATE_ON_DEG}$ deglitch time. Outside this range, USBGATE will be automatically turned off.

If the two inputs appear on VUSB and VWPC at the same time, the USBGATE will be turned on with a higher priority, and the WPCGATE will be forcibly turned off; if not, USBGATE or WPCGATE will be turned on according to which input source is inserted first, and the other one will remain off even if a valid source is inserted later. When the running input source is plugged out or OVP failure occurs, the corresponding gate driver will be turned off, and the other gate driver will be turned on after 1ms delay if its input source is valid. The USBGATE_STAT and WPCGATE_STAT bits indicate the real-time ON/OFF status of USBGATE/ WPCGATE.

Reverse Manual Mode

When the OVPFET operates in reverse mode, it must be turned on/off manually, depending on which port is desired for the reverse output. It will also turn off the corresponding external OVPFET Q_{USB} or Q_{WPC} when VUSB_OVP or VWPC_OVP fault occurs.

To enter reverse operation mode, the AP should follow the steps below:

1. The AP writes USBGATE_MODE = 1 and USBGATE_EN = 0 and USBFET_ON_DIRECTION = 1, and/or writes WPCGATE_MODE = 1 and WPCGATE_EN = 0 and WPCFET_ON_DIRECTION = 1;
2. The AP writes SCC_MODE[2:0] = 011/100/101;
3. The AP writes SCC_EN = 1, and SGM41611 starts the reverse operation;
4. SGM41611 sets VBUS_PRESENT_FLAG = 1 when V_{VBUS} > $V_{BUS_PRESENT_R}$ and It generates an INT pulse to notify the AP;
5. The AP writes (USBGATE_EN = 1 and USBGATE_CTRL = 1) or (WPCGATE_EN = 1 and WPCGATE_CTRL = 1) depending on which port is desired for the reverse output;
6. If VUSB_OVP or VWPC_OVP fault occurs, SGM41611 will turn off the corresponding external OVPFET Q_{USB} or Q_{WPC} although USBGATE_EN/WPCGATE_EN is still 1. Then it generates an INT pulse to notify the AP, and SCC_EN will not be reset to 0;
7. The AP needs to reset USBGATE_EN = 0 or WPCGATE_EN = 0, and can write 1 to the VUSB/VWPC/VBUS pull-down resistor enable bits as needed to discharge the residual energy.

To exit reverse operation mode, the AP should follow the steps below:

1. The AP writes USBGATE_CTRL = 0 or WPCGATE_CTRL = 0, and SGM41611 turns off the corresponding external OVPFET Q_{USB} or Q_{WPC};
2. The AP writes SCC_EN = 0;
3. SGM41611 stops reverse operation and turns off the Q_{RB};
4. The AP writes USBGATE_MODE = 0 and/or WPCGATE_MODE = 0;
5. The AP can write 1 to the VUSB/VWPC/VBUS pull-down resistor enable bits as needed to discharge the residual energy.

I²C Address Setting

In addition to the SGM41611 requiring a 0.22μF MLCC capacitor between the CDRVH and CDRVL_ADS pins to provide driver supply, the CDRVL_ADS pin is also used to set the default I²C address during the POR procedure. Pull CDRVL_ADS low by a 75kΩ resistor to AGND to select address 0x67. Pull CDRVL_ADS low by a 249kΩ resistor to AGND or leave it floating to select address 0x68. Changes are not allowed after the startup procedure.

ADC

The SGM41611 integrates a fast 9-channel, 12-bit ADC converter to monitor input/output currents and voltages and the temperature of the device. The ADC is controlled by the ADC_CTRLx registers. Setting the ADC_EN bit to 1 enables the ADC. This bit can be used to turn off the ADC and save power when it is not needed. The ADC_RATE bit allows choosing continuous conversion or 1-shot conversion mode. The ADC operates independent of the faults, unless the AP sets the ADC_EN bit to 0.

The ADC can operate if V_{VBUS} > $V_{BUS_PRESENT_R}$ or V_{VOUT} > $V_{BAT_INSERT_R}$ condition is valid. Otherwise the ADC conversion is postponed until one of them is satisfied. The ADC readings are valid only for DC values and not for transients.

DETAILED DESCRIPTION (continued)

By default, all ADC channels are converted in continuous conversion mode except the channels disabled by the ADC_CTRLx registers. If the 1-shot conversion mode is selected, the ADC_DONE_FLAG bit is set to 1 when all channels are converted, then the ADC_EN bit is reset to 0. In the continuous conversion mode, the ADC_DONE_FLAG bit is set to 0.

nINT Pin, Flag and Mask Bits

The nINT pin is an open-drain output and must be pulled up to a logic high rail. It is pulled low with a duration of t_{INT} to notify the AP when it is triggered by an event. See the register map for all event flag and control bits.

When an event occurs, a nINT signal is sent to the AP and the corresponding flag bit is set to 1. The flag bit can be read and some of them can be reset only after the fault is cleared. The nINT signal is not re-sent if an event is still present after the flag bit is read, unless another kind of event occurs. If an event mask bit is set, that event will not send nINT signal, but the flag bit is still updated independent of the mask bit.

The INT pulse generation behavior examples are shown in Figure 8.

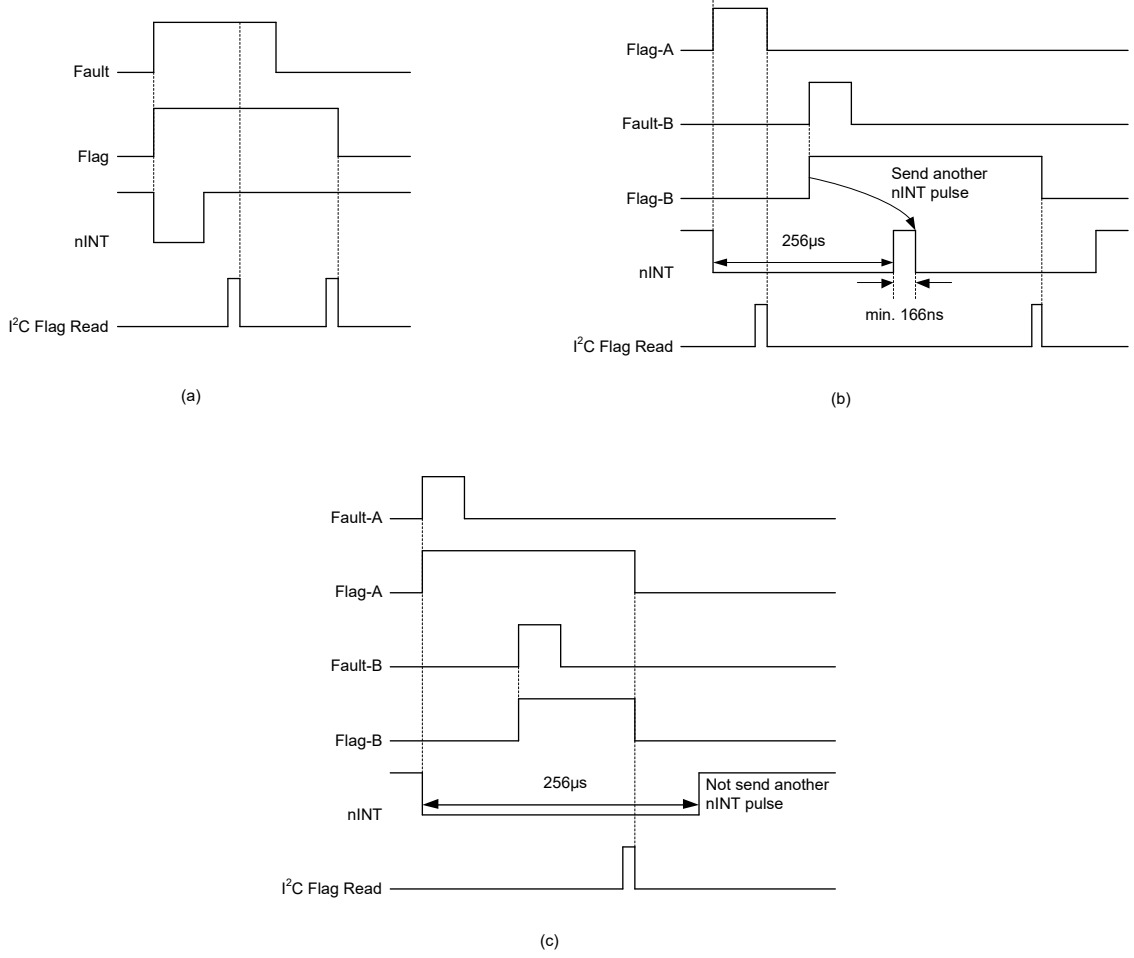


Figure 8. nINT Pulse Generation Behavior Examples

DETAILED DESCRIPTION (continued)

Input Over-Voltage Protection (VUSB_OVP, VWPC_OVP)

The SGM41611 monitors the adapter voltage on the VUSB/VWPC pin to use the USBGATE/WPCGATE output to control the external OVPFETs Q_{USB}/Q_{WPC} respectively. Taking VUSB_OVP as an example, the VUSB over-voltage protection circuit is powered by VUSB and is enabled if V_{VUSB} rises above $V_{USB_INSERT_R}$. If V_{VUSB} is above $V_{USB_INSERT_R}$ for at least $t_{USBGATE_ON_DEG}$ time, when USBGATE_MODE bit is set to forward auto-mode, the USBGATE will output drive signal to turn on the external OVPFET Q_{USB}. If the V_{VUSB} reaches the $V_{USB_OVP_R}$ threshold, the gate voltage starts to drop and eventually the OVPFET Q_{USB} is fully turned off. Figure 9 shows the VUSB_OVP and USBGATE operation timings. The $V_{USB_OVP_R}$ threshold can be set by I²C serial interface. The adapter voltage must never exceed the absolute maximum rating of the VUSB/VWPC pin and the external OVPFETs.

Input Short-Circuit Protection (VBUS_SC)

The VBUS_SC function monitors the VBUS pin for short-circuit. This function is enabled if the external OVPFETs are turned on or if V_{VBUS} rises above $V_{BUS_PRESENT_R}$. If the V_{VBUS} falls below 2.5V, the OVPFETs are turned off, and operation is stopped. SCC_EN bit is reset to 0 (disable). Also, VBUS_ABSENT_FLAG bit is set to 1, and an INT pulse is asserted. The device will wait for 512ms before automatically re-enabling and initiating startup sequence.

VBUS Charge Voltage Range (VBUS_LO & VBUS_HI)

The VBUS_LO and VBUS_HI functions are included to avoid problems due to wrong VBUS setting for forward charging. If V_{VBUS} is beyond the range between V_{BUS_LO} and V_{BUS_HI}, the device remains in charge initiation operation. Once V_{VBUS} is within the charge range, forward charging will start and VBUS_LO and VBUS_HI functions will be disabled.

Input, Output and Battery Over-Voltage Protection (VBUS_OVP, VBUS_PK_OVP, VOUT_OVP and VBATx_OVP)

The VBUS_OVP, VBUS_PK_OVP, VOUT_OVP and VBAT_OVP functions detect input and output voltage conditions. If either input or output voltage is higher than the protection threshold, the operation is stopped and the SCC_EN bit is reset to 0 (disable). The VBUS_OVP and VBUS_PK_OVP functions monitor VBUS pin voltage. The VOUT_OVP function monitors VOUT pin voltage. The VBATx_OVP uses BATPx and BATNx remote sense pins to monitor differential voltage between the battery terminals. To minimize the risk of battery terminal short in the manufacturing process, a 100Ω resistor needs to be connected in series to the BATPx and BATNx pin respectively. The VBUS_OVP, VOUT_OVP and VBATx_OVP thresholds can be set by I²C serial interface.

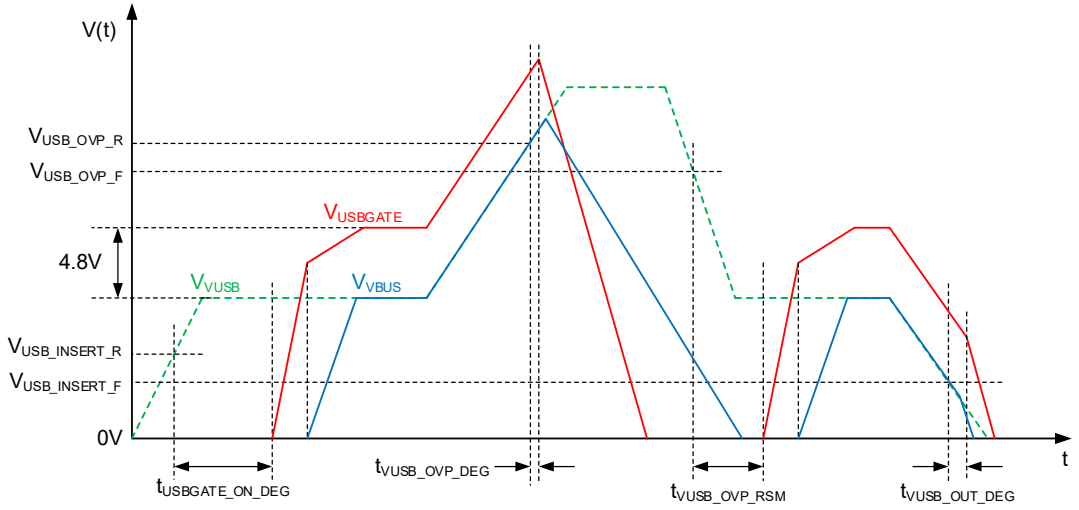


Figure 9. OVPGATE Operation Timing

DETAILED DESCRIPTION (continued)

Bidirectional Bus and Battery Over-Current Protection (IBUS_OCPxx and IBAT_OCP)

The IBUS_OCP function monitors the bidirectional current via Q_{RB}. If SCC_EN bit is set to enable forward/reverse operation, the Q_{RB} is turned on and the IBUS_OCP function starts detecting the current. If the I_{BUS} reaches I_{BUS_OCPXX} threshold, the device stops operation and resets SCC_EN bit to 0 (disable). The bidirectional battery current is monitored by the voltage across an external series shunt resistor. This differential voltage is measured between SRP and SRN pins. If I_{BAT_OCP} threshold is reached, the device stops operation and resets SCC_EN bit to 0 (disable). The I_{BUS_OCPxx} and I_{BAT_OCP} thresholds can be set by I²C serial interface.

Input Under-Current Protection (IBUS_UCP)

The IBUS_UCP function detects the input current via Q_{RB} during forward charging. After charging is started, the $t_{IBUS_UCP_BLK}$ timer is enabled and I_{BUS} current is compared with $I_{BUS_UCP_R}$. If I_{BUS} cannot exceed $I_{BUS_UCP_R}$ within $t_{IBUS_UCP_BLK}$, the charging will be stopped and SCC_EN bit is reset to 0 (disable). If I_{BUS} exceeds $I_{BUS_UCP_R}$ when $t_{IBUS_UCP_BLK}$ times out, from then on, if I_{BUS} falls below the $I_{BUS_UCP_F}$ threshold, the charging will be stopped and SCC_EN bit is reset to 0 (disable). The $t_{IBUS_UCP_BLK}$ timer can be set by I²C serial interface.

Input Reverse-Current Protection (IBUS_RCP)

The IBUS_RCP function detects the input reverse current via Q_{RB} during forward charging. If the reverse current flowing from the battery to the input source reaches IBUS_RCP threshold, the IBUS_RCP_FLAG bit is set to 1 and an INT pulse is generated, the charging will be stopped and SCC_EN bit is reset to 0 (disable).

PMID Charge Voltage Range (PMID2VOUT_UVP & PMID2VOUT_OVP)

The PMID2VOUT_UVP and PMID2VOUT_OVP functions are included to avoid problems caused by abnormal input or output transients during forward or reverse operation. If (V_{PMID}/n - V_{VOUT}) is beyond the range between $V_{PMID2VOUT_UVP}$ and $V_{PMID2VOUT_OVP}$, where n = 1, 2 or 4, depending on the operation mode, the operation will be stopped and SCC_EN bit is reset to 0 (disable). The $V_{PMID2VOUT_UVP}$ and $V_{PMID2VOUT_OVP}$ thresholds can be set by I²C serial interface.

CFLY Diagnosis (PIN_DIAG)

The CFLY diagnosis function identifies the health of flying capacitors before and during forward or reverse operation. The device initialization process is started after SCC_EN bit is set to 1. When V_{VBUS} and/or V_{BAT} are/is in the charge range, the flying capacitors in both channels are pre-charged. A CFLY open/short-circuit is detected if they cannot be charged. If so, the initialization process is stopped and SCC_EN bit is reset to 0 (disable). Even if CFLY capacitors pass the open/short-circuit test in the initialization process, the CFLY diagnosis function remains active and whenever a V_{CFxx} voltage falls, the operation is stopped and SCC_EN bit is reset to 0 (disable). The PIN_DIAG_FLAG bit is set to 1 and an INT pulse is generated as well. During a CFLY short-circuit event, other protection events such as IBUS_OCP, VBAT_OVP or PEAK_OCP may occur.

A CFLY discharge circuit is activated before the internal RBFET (Q_{RB}) is turned on if V_{VBUS} > $V_{BUS_PRESENT_R}$ to prevent over-current stress at the start of charging.

VOUT Short-Circuit Protection (VOUT_SC)

The VOUT_SC function monitors the VOUT pin for short-circuit. This function is enabled during forward or reverse operation. If V_{VOUT} falls below V_{OUT_SC} (2.7V) threshold, the operation is stopped and SCC_EN bit is reset to 0 (disable). Also, the PIN_DIAG_FLAG bit is set to 1, and an INT pulse is generated.

Bidirectional Converter Peak Over-Current Protection (PEAK_OCP)

The PEAK_OCP function monitors the converter switch operating currents. If the switch current reach peak OCP threshold during forward or reverse operation, the PEAK_OCP_FLAG bit is set to 1 and an INT pulse is generated, the operation is stopped and SCC_EN bit is reset to 0 (disable). The switch peak OCP thresholds can be set by I²C serial interface.

TDIE Over-Temperature Protection (TDIE_OTP)

The TDIE_OTP function prevents operation in over-temperature condition. The die temperature is monitored and if the $T_{DIE_OTP_R}$ threshold is reached, the operation is stopped and SCC_EN bit is reset to 0 (disable). The startup sequence cannot be initiated again until the die temperature falls down with a 20℃ hysteresis. The TDIE_OTP threshold can be set by I²C serial interface.

APPLICATION INFORMATION

Input Capacitors (C_{VUSB}, C_{VWPC}, C_{VBUS} and C_{PMID})

Input capacitors are selected by considering two main factors:

1. Adequate voltage margin above maximum surge voltage;
2. Not too large voltage margin in order to limit the peak currents drawn from the source and reduce the input noise.

For C_{VUSB}, C_{VWPC} and C_{VBUS}, use low ESR bypass ceramic capacitors placed close to the VUSB/VWPC/VBUS and PGND pins respectively. The C_{PMID} are determined by the minimum capacitance needed for stable operation and the required ESR to minimize the voltage ripple and load step transients. Typically, two 4.7μF or larger X5R ceramic capacitors are sufficient to meet the C_{PMID} requirements of two channels. Consider the DC bias derating of the ceramic capacitors. The X5R and X7R capacitors are relatively stable against DC bias and high temperature. Note that the bias effect is more severe with smaller package sizes, so choose the largest affordable package size. Also consider a large margin for the voltage rating for the worst-case transient input voltages.

External OVPFETs (Q_{USB} and Q_{WPC})

The maximum recommended input range is 21V. If the supplied VUSB or VWPC voltage is above 21V, two sets of back-to-back N-channel OVPFETs are recommended between the adapter inputs and the SGM41611. Choose a low R_{DSON} MOSFET for the OVPFET to minimize power losses.

Flying Capacitors (C_{FLY})

For selection of the C_{FLY} capacitors, the current rating, ESR and the bias voltage derating are critical parameters. The C_{FLY} capacitors are biased to different DC voltages according to the operation mode. To trade-off between efficiency and power density, set the C_{FLY} voltage ripple to the 2% of its DC bias voltage as a good starting point. The C_{FLY} for each phase can be calculated by Equation 1:

$$C_{FLY} = \frac{I_{BAT}}{8 f_{SW} V_{CFLY_RPP}} = \frac{I_{BAT}}{16\% f_{SW} V_{DC_CFLY}} \quad (1)$$

where I_{BAT} is the charging current and V_{CFLY_RPP} is the peak-to-peak voltage ripple of the C_{FLY}.

Choosing a too small capacitor for C_{FLY} results in lower efficiency and high output voltage/current ripples. However, choosing a too large C_{FLY} only provides minor efficiency and output ripple improvements.

The default switching frequency is f_{SW} = 600kHz. It can be adjusted by FSW_SET[2:0] bits in REG0x07. Lower frequency increases efficiency by reducing switching losses but requires larger capacitance to maintain low output ripple and low output impedance. An optimum switching frequency can be found for any selected C_{FLY} capacitor to minimize losses.

Output Capacitor (C_{VOUT})

C_{VOUT} selection criteria are similar to the C_{FLY} capacitor. Larger C_{VOUT} value results in less output voltage ripple, but due to the dual-phase operation, the C_{VOUT} RMS current is much smaller than C_{FLY}, so smaller capacitance value can be chosen for C_{VOUT} as given in Equation 2:

$$C_{VOUT} = \frac{I_{BAT} \times t_{DEAD}}{0.5 \times V_{VOUT_RPP}} \quad (2)$$

where t_{DEAD} is the dead time between the two phases and V_{VOUT_RPP} is the peak-to-peak output voltage ripple and is typically set to the 2% of V_{OUT}.

C_{VOUT} is biased to the battery voltage and its nominal value should be derated for battery voltage DC bias. Typically two 10μF, X5R or better grade ceramic capacitors placed close to the VOUT and PGND pins provide stable performance of two channels.

External Bootstrap Capacitor (C_{BST1} and C_{BST2})

The bootstrap capacitors provide the gate driver supply voltage for the internal switches. Respectively place a 100nF low ESR ceramic capacitor between BST1A and CT3A pins, between BST2A and CT1A pins, between BST1B and CT3B pins and between BST2B and CT1B pins.

PCB Layout Guidelines

A good PCB layout is critical for stable operation of the SGM41611. Follow these guidelines for the best results:

1. Use short and wide traces for VBUS as it carries high current.
2. Minimize connectors wherever possible. Connector losses are significant especially at high currents.
3. Use solid thermal vias for better thermal relief.
4. Bypass VBUS, PMID and VOUT pins to PGND with ceramic capacitors as close to the device pins as possible.
5. Place C_{FLY} capacitors as close as possible to the device with small pad areas to reduce switching noise and EMI.
6. Connect or reference all quiet signals to the AGND pin.
7. Connect and reference all power signals to the PGND pins (preferably the nearest ones).
8. Try not to interrupt or break the power planes by signal traces.

TYPICAL APPLICATION CIRCUIT

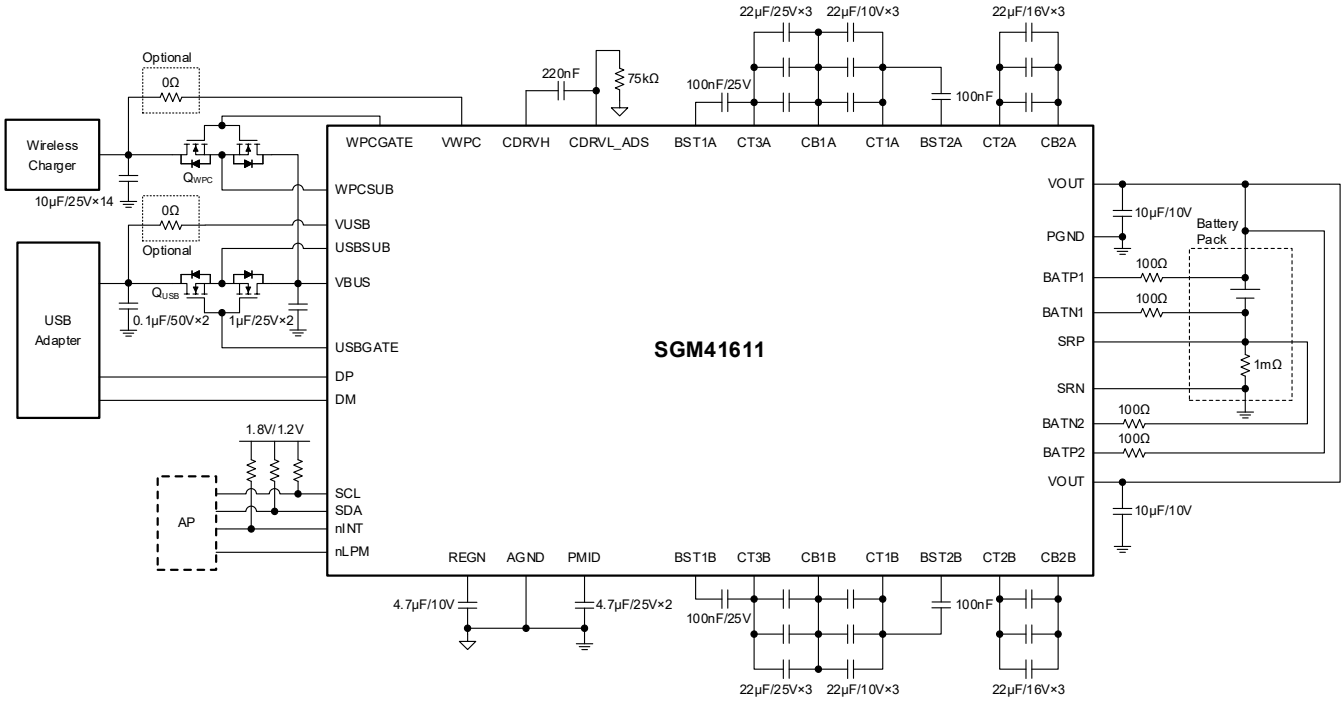


Figure 10. Typical Application Circuit of SGM41611

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

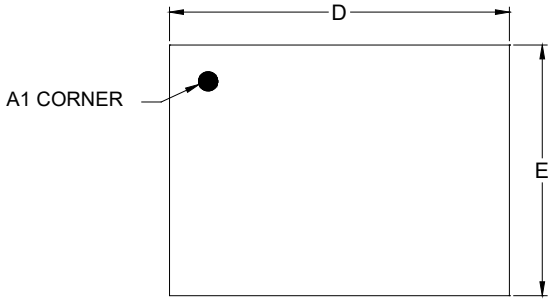
JULY 2026 – REV.A.1 to REV.A.2	Page
Changed Detailed Description section	52

SEPTEMBER 2025 – REV.A to REV.A.1	Page
Corrected CDRVL_ADS pin name in Figure 1	1
Added Electrical Characteristics conditions	7 ~ 9
Modified 0xA1[5] and 0xA2[5] bit names	45
Updated Application Information section	56
Corrected CDRVL_ADS pin name in Figure 10	57

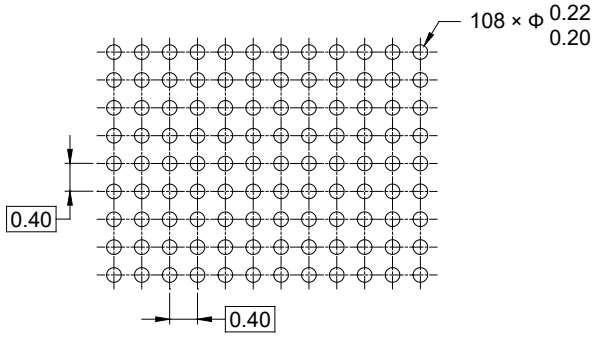
Changes from Original to REV.A (SEPTEMBER 2024)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

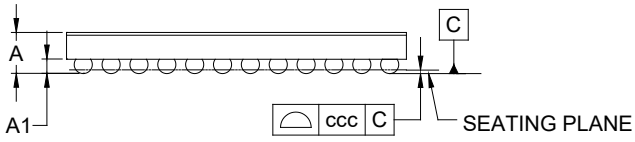
WLCSP-4.88×3.6-108B



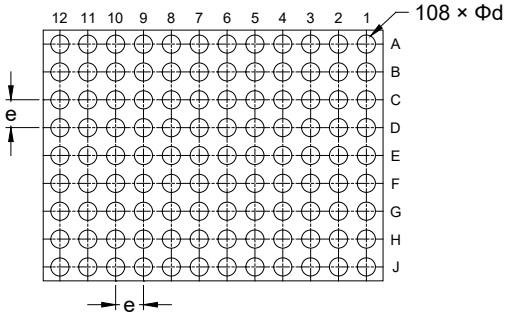
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



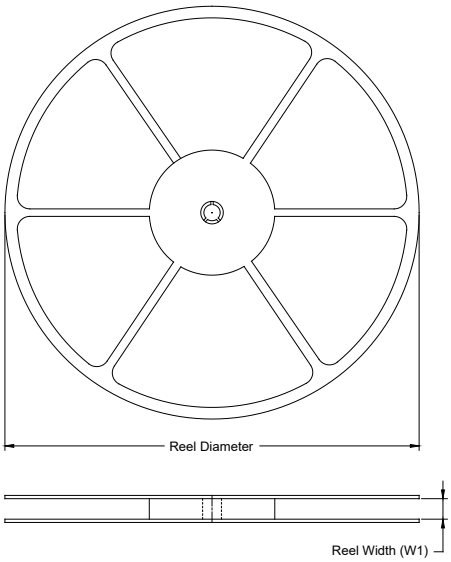
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.625
A1	0.186	-	0.226
D	4.850	-	4.910
E	3.570	-	3.630
d	0.230	-	0.290
e	0.400 BSC		
ccc	0.050		

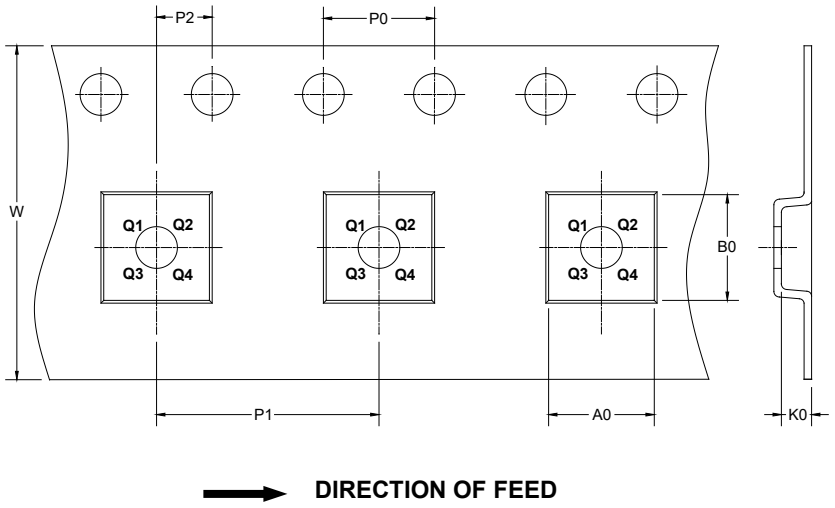
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



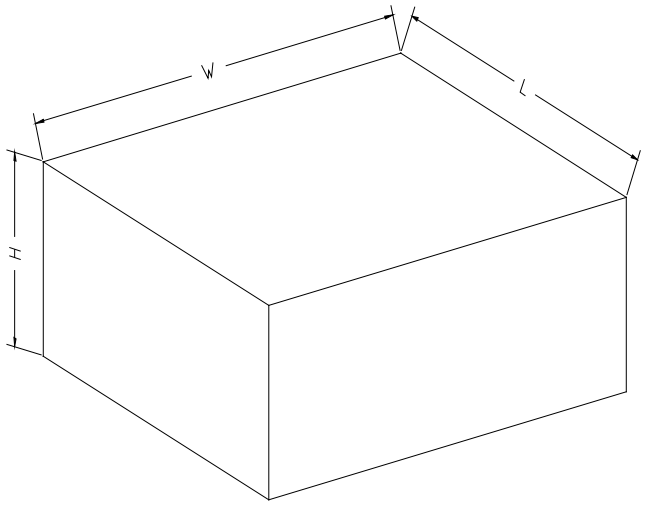
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-4.88×3.6-108B	7"	12.4	3.80	5.37	0.69	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002