SGM41574

I²C Controlled, 1- to 4-Cell, 5A Fully Integrated Buck-Boost Battery Charger with Narrow VDC Power Path Management

FEATURES

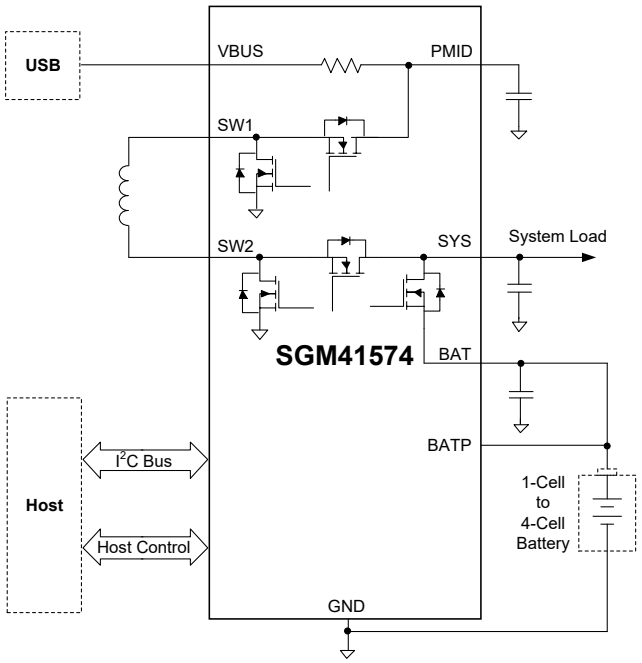
- 3.6V to 24V Wide Operating Input Voltage Range
- Up to 30V Sustainable Voltage
- Dual-Input Power Mux Controller for Source Selection
- Ship Mode, Shutdown Mode and System Power Reset Capability by External SFET Control
- USB BC1.2, Non-Standard, and HVDCP Input Source Adaptors Auto Detection
- 22μA (TYP) Quiescent Current at Battery Only Operation
- 0.4μA (TYP) Shutdown Current in Shutdown Mode
- 4 Switching MOSFETs Buck-Boost Charger for 1-4 Cells Battery
- Up to 95.5% Efficiency for 2-Cell 8V Battery and 2A Charge Current from 12V Input
- Programmable Fast Charge Current from 50mA to 5A with 10mA Step
- USB OTG with 2.8V to 22V Adjustable Output to Support USB-PD PPS
- Up to 3.32A Programmable OTG Output Current Limit
- Fully Integrated All MOSFETs, Current Sense and Compensation
- 750kHz and 1.5MHz Programmable Frequency
- Selectable PFM Mode and Out-of-Audio (OOA) Mode at Light Load Operations
- Narrow Voltage DC (NVDC) Power Path Management
- I²C Port for Flexible System Parameter Setting and Status Reporting
- Integrated ADC for Monitoring Input Voltage, Input Current, Battery Voltage, Charge Current, System Voltage, Battery Temperature and Die Temperature
- Input Current Optimizer (ICO) to Maximize Adaptor Output Current without Overloading
- Programmable Input Current Limit (IINDPM) and Dynamic Power Management to Support USB Standard Adaptors
- Maximum Power Tracking by Programmable Input Voltage Limit (VINDPM)
- Safety Features including Configurable JEITA for Battery Temperature Protection
- Battery Charging Safety Timer
- Thermal Regulation and Thermal Shutdown
- Watchdog Monitoring I²C Operation
- VBUS/System/Battery Over-Voltage Protection
- Output Over-Current Protection for Both Forward Charge Mode and OTG Mode

APPLICATIONS

Smartphone, EPOS

Portable Internet Devices and Accessory

SIMPLIFIED SCHEMATIC



GENERAL DESCRIPTION

The SGM41574 is an integrated 4 switching MOSFETs Buck-Boost battery charger and system power path management device for 1-4 cells Li-Ion or Li-polymer batteries. Its low-impedance power path optimizes efficiency, reduces battery charging time, and extends battery life. I^2C programming makes it a flexible powering and charger design solution.

The SGM41574 can detect the input source types which include SDP/CDP/DCP and non-standard adaptor through the D+/D- pins following USB BC1.2 specification. It provides D+/D- handshake to support fast charging with the adjustable high voltage adaptor (HVDCP). The wide full input voltage range and the input current range can also support USB-PD applications.

To support 1-4 cells Li-Ion battery charging, the SGM41574 automatically works at Buck, Boost or Buck-Boost configurations according to the adaptor voltage and the battery voltage. The SGM41574 supports two different input sources with its dual input source selector management.

The SGM41574 employs narrow VDC architecture (NVDC) with BATFET separating system from the battery. Even without battery or with a fully depleted battery, the system is regulated to above the minimum system voltage. The SGM41574 features a dynamic power management (DPM) to avoid input adaptor overloading or to meet the maximum current limit. It keeps the system voltage regulated to its minimum setting in DPM mode by reducing the charge current. The SGM41574 also provides supplement mode to further support system output in case that charge current decreased to zero and the input is still overload. The SGM41574 can provide the maximum power point with an algorithm called input current optimizer (ICO) to avoid the input source overload.

The SGM41574 supports the default mode (standalone) without the host control. It automatically detects the battery voltage and starts charging. A charge cycle automatically terminates when a full charge is detected if the device is not in thermal regulation or DPM mode. The charger automatically initiates a new charging cycle if battery voltage falls below the recharge threshold.

The SGM41574 supports USB On-The-Go (OTG) operation by supplying default 5V on the VBUS with an output current limit up to 3.32A. To support the programmable power supply (PPS) feature defined by the USB-PD 3.0 Specifications, the OTG voltage is programmable from 2.8V to 22V with 10mV resolution.

To save the power from battery to system, the SGM41574 provides an SDRV pin to control an external N-channel ship FET. Host can set charger to ship mode or shutdown mode to reduce the leakage current from battery by I^2C.

The SGM41574 provides full protections for safety of battery charging and system operation, including battery temperature monitoring, charging safety timer, over-current and over-voltage protections. When any fault occurs, the SGM41574 asserts an nINT pulse to notify the host.

The SGM41574 provides the integrated 16-bit ADC for monitoring input voltage, input current, battery voltage, charge current, system voltage, battery temperature and die temperature.

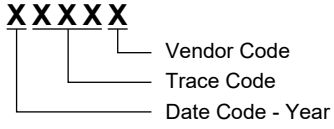
The SGM41574 is available in a Green TQFN-4×4-29L package.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41574	TQFN-4×4-29L	-40℃ to +85℃	SGM41574YTWM29G/TR	SGM41574 YTWM29 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)
- VAC1, VAC2 ..... -2V to 30V
- VBUS (Converter Not Switching) ..... -2V to 30V
- PMID (Converter Not Switching) ..... -0.3V to 30V
- ACDRV1, ACDRV2, BTST1 ..... -0.3V to 32V
- SYS (Converter Not Switching) ..... -0.3V to 23V
- BATP, BAT ..... -0.3V to 20V
- BTST2 ..... -0.3V to 29V
- SDRV ..... -0.3V to 26V
- SW1 ..... -2V (50ns) to 30V
- SW2 ..... -2V (50ns) to 23V
- nQON, D+, D-, nCE, STAT, SCL, SDA, nINT, ILIM_HIZ, PROG, TS, REGN ..... -0.3V to 6V

Output Sink Current
- STAT, nINT 6mA

Differential Voltage Range
- BTST1-SW1, BTST2-SW2 ..... -0.3V to 6V
- SYS-BAT ..... -0.3V to 16V
- SDRV-BAT ..... -0.3V to 6V

Package Thermal Resistance
- TQFN-4×4-29L, θ_{JA} ..... 38.9℃/W
- TQFN-4×4-29L, θ_{JB} ..... 4.8℃/W
- TQFN-4×4-29L, θ_{JC} ..... 15.4℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±3000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{VBUS} ..... 3.6V to 24V
Input Current, I_{VBUS} ..... 3.3A (MAX)
Battery Voltage, V_{BAT} ..... 18.8V (MAX)
Output Current (SW), I_{SW} ..... 5A (MAX)
Fast Charging Current, I_{BAT} ..... 5A (MAX)
RMS Discharge Current (Continuously), I_{BAT} ..... 6A (MAX)
Peak Discharge Current (Up to 1s), I_{BAT} ..... 10A (MAX)
Operating Ambient Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

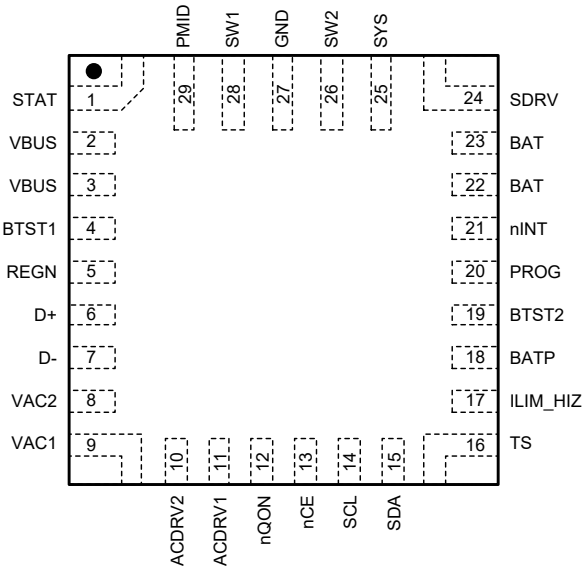
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-4×4-29L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	STAT	DO	Open-Drain Charge Status Output. Connect this pin to logic high rail through a 2.2kΩ resistor and LED series for charge status indication. The STAT pin acts as follows: During charge: low (LED ON). Charge completed or charge disabled: high (LED OFF). Charge suspended (in response to a fault): 1Hz pulses with 50% duty cycle (LED BLINKS). The function can be disabled by setting the STAT_DIS bit to 1.
2, 3	VBUS	P	Charger Input. The power input terminal of the charger. VBUS and PMID pins are internally connected by current sensing capability. Place 3 × 10μF ceramic capacitors from VBUS pin to GND close to the device.
4	BTST1	P	Input High-side Power MOSFET (Q1) Gate Driver Power Supply. A 47nF bootstrap capacitor between SW1 and BTST1 pins is recommended.
5	REGN	P	Charger Internal Linear Regulator Output. Power supply for internal MOSFET drivers and IC. Connect a 4.7μF ceramic capacitor from REGN pin to GND.
6	D+	AIO	Positive USB Data Line. D+/D- based USB device protocol detection.
7	D-	AIO	Negative USB Data Line. D+/D- based USB device protocol detection.
8	VAC2	P	VAC2 Input Detection. A valid VAC2 voltage is detected when the voltage is between 3.6V and 24V. Connect this pin to VBUS if the ACFET2-RBFET2 is uninstalled.
9	VAC1	P	VAC1 Input Detection. A valid VAC1 voltage is detected when the voltage is between 3.6V and 24V. Connect this pin to VBUS if the ACFET1-RBFET1 is uninstalled.
10	ACDRV2	P	Input FETs Driver Pin 2. The ACDRV2 provides driver voltage (typical 5V above VBUS voltage) for the input 2 (VAC2) back-to-back MOSFETs (ACFET2 and RBFET2) between VAC2 and VBUS pins. Connect this pin to GND if the ACFET2-RBFET2 is uninstalled.
11	ACDRV1	P	Input FETs Driver Pin 1. The ACDRV1 provides driver voltage (typical 5V above VBUS voltage) for the input 1 (VAC1) back-to-back MOSFETs (ACFET1 and RBFET1) between VAC1 and VBUS pins. Connect this pin to GND if the ACFET1-RBFET1 is uninstalled.
12	nQON	DI	Ship FET Enable or System Power Reset Control Input. In ship mode, a logic low on this pin with t_{SM_EXIT} duration turns on the ship FET and the SGM41574 exits the ship mode. In normal operation mode, a logic low on this pin with 10s duration turns off the ship FET for 350ms and then turns it on to reset the system power. During 350ms of the ship FET shutdown, if the VBUS is high, the charger is set to HIZ mode, and there is a 30mA current on SYS to discharge the system voltage. After the ship FET turns on again, the HIZ mode is disabled. This pin is internal pulled up to high logic by default.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
13	nCE	DI	Charge Enable Input Pin (Active Low). When nCE pin is low and EN_CHG = 1, the charge is enabled. Do not leave nCE pin floating.
14	SCL	DI	I^2C Clock Signal. Use a 10kΩ pull-up to the logic high rail.
15	SDA	DIO	I^2C Data Signal. Use a 10kΩ pull-up to the logic high rail.
16	TS	AI	Temperature Sense Input Pin. Connect to the battery NTC thermistor that is grounded on the other side. To program operating temperature window, it can be biased by a resistor divider between REGN and GND. Charge suspends if TS voltage goes out of the programmed range. It is recommended to use a 103AT-2 type thermistor.
17	ILIM_HIZ	AI	Input Current Limit Setting and HIZ Mode Control Pin. A resistor between ILIM_HIZ and GND can clamp the input current limit as I_{INMAX} = (V_{ILIM_HIZ} - 1V)/800mΩ. When EN_EXTILIM = 1, the lower limit between IINDPM[8:0] registers and ILIM_HIZ pin resistor setting set the actual input current limit. The ILIM_HIZ pin can supply higher than 100mA current limit only. For both forward charging mode and OTG mode, the device stops switching with REGN on when ILIM_HIZ pin is pulled lower than 0.7V, and it resumes switching if ILIM_HIZ recovers higher than 1.1V. Do not leave this pin floating.
18	BATP	P	Positive Battery Sense Terminal. Kelvin connects this pin to positive battery terminal (BAT pin) with 100Ω series resistor. This pin cannot be floating.
19	BTST2	P	Output High-side Power MOSFET (Q4) Gate Driver Power Supply. A 47nF bootstrap capacitor between SW2 and BTST2 pins is recommended.
20	PROG	DI	Charger POR Default Settings Program. At POR, the charger detects the pull-down resistance of the PROG pin, and then sets the charger default POR switching frequency and the battery cell count. The ICHG[8:0], VSYSMIN[5:0] and VREG[10:0] registers are updated to associate with the battery cell count. Tolerance of the pull-down resistance is recommended to be ±1% or ±2%.
21	nINT	DO	Open-Drain Interrupt Output Pin. Use a 10kΩ pull-up to the logic high rail. The nINT pin is active low and sends a negative 256μs pulse to inform host about a new charger status update or a fault.
22, 23	BAT	P	Battery Positive Terminal Pin. Connect 2 × 10μF ceramic capacitors between BAT and GND pins close to the device. SYS and BAT pins are internally connected by BATFET with current sensing capability.
24	SDRV	P	External N-Channel Ship FET (SFET) Gate Driver Output. It is the driver pin of the external ship FET. To enter ship mode or shutdown mode, this pin is pulled low to turn off the ship FET. In normal operation, this pin keeps high (typical 5V above BAT voltage) to turn on the ship FET. The SFET_PRESENT bit should be configured to 1 before using the features associated with the ship FET. A 1nF ceramic capacitor from SDRV pin to GND is recommended when the ship FET is not populated.
25	SYS	P	System Connection. The SYS pin is connected to the BAT pin with an internal BATFET. Connect 5 × 10μF and one 0.1μF ceramic capacitors from SYS pin to GND close to the device.
26	SW2	P	Boost Side Half Bridge Switching Node.
27	GND	P	Ground Pin of the Device.
28	SW1	P	Buck Side Half Bridge Switching Node.
29	PMID	P	Q1 MOSFET Drain Connection. An internal N-channel high-side MOSFET (Q1) is connected between PMID and SW1 pins with the drain on PMID pin and the source on SW1 pin. The capacitor placed at PMID pin cannot be too large, see details in Application Information section. It is recommended to connect only one 10μF/25V/0805 ceramic capacitor and one 0.1μF ceramic capacitor from PMID pin to GND close to the device.

NOTE: AI = analog input, AO = analog output, AIO = analog input and output, DI = digital input, DO = digital output, DIO = digital input and output, P = power.

ELECTRICAL CHARACTERISTICS

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Currents							
Quiescent Battery Current (BATP, BAT, SYS) in Battery Only Mode	$I_{Q_BAT_ON}$	V_{BAT} = 8V, No VBUS, BATFET is enabled, I²C enabled, ADC disabled, system is powered by battery, T_J = +25℃			22	28	μA
Quiescent Battery Current (BATP) in Ship Mode	$I_{Q_BAT_OFF}$	V_{BAT} = 8V, No VBUS, I²C enabled, ADC disabled, in ship mode, T_J = +25℃			8	10	μA
Shutdown Battery Current (BATP) in Shutdown Mode	I_{SD_BAT}	V_{BAT} = 8V, No VBUS, I²C disabled, ADC disabled, in shutdown mode			0.4	1	μA
Quiescent Input Current (VBUS)	I_{Q_VBUS}	V_{VBUS} = 15V, V_{BAT} = 8V, charge disabled, converter switching, I_{SYS} = 0A, PFM enabled	OOA disabled		2.8		mA
			OOA enabled		12		
Shutdown Input Current (VBUS) in HIZ Mode	I_{SD_VBUS}	V_{VBUS} = 5V, HIZ mode, no battery, ADC disabled, ACDRV disabled			280		μA
Quiescent Battery Current (BATP, BAT, SYS) in OTG Mode	I_{Q_OTG}	V_{BAT} = 8V, V_{VBUS} = 5V, OTG mode enabled, converter switching, I_{VBUS} = 0A, PFM enabled	OOA disabled		3.3		mA
			OOA enabled		10		
VBUS Pin and VBAT Pin Power-Up							
VAC Present Rising Threshold to Turn-On the ACFET-RBFET	$V_{VAC_PRESENT}$	For both VAC1 and VAC2			3.45	3.6	V
VAC Present Falling Threshold to Turn-Off the ACFET-RBFET				3.1	3.25		V
VAC Over-Voltage Rising Threshold	V_{VAC_OVP}	For both VAC1 and VAC2	VAC_OVP[1:0] = 00	25.2	25.8	26.4	V
			VAC_OVP[1:0] = 01	21.1	21.6	22.1	
			VAC_OVP[1:0] = 10	11.7	12	12.3	
			VAC_OVP[1:0] = 11	6.7	7	7.3	
VAC Over-Voltage Falling Threshold	V_{VAC_OVP}	For both VAC1 and VAC2	VAC_OVP[1:0] = 00	24.4	25	25.6	V
			VAC_OVP[1:0] = 01	20.6	21.1	21.6	
			VAC_OVP[1:0] = 10	11.3	11.6	11.9	
			VAC_OVP[1:0] = 11	6.5	6.8	7.1	
VBUS Operating Range	V_{VBUS_OP}			3.6		24	V
VBUS Rising for Active I²C (with No Battery)	V_{VBUS_UVLOZ}	V_{VBUS} rising		3.1	3.3	3.5	V
VBUS Falling to Turn-Off I²C (with No Battery)	V_{VBUS_UVLO}	V_{VBUS} falling		2.85	3.05	3.25	V
VBUS Rising for REGN On	$V_{VBUS_PRESENT}$	V_{VBUS} rising		3.3	3.45	3.6	V
VBUS Falling for REGN Off	$V_{VBUS_PRESENTZ}$	V_{VBUS} falling		3.1	3.25	3.4	V
VBUS Over-Voltage Rising Threshold	V_{VBUS_OVP}	V_{VBUS} rising		25.1	25.5	26.1	V
VBUS Over-Voltage Falling Threshold	V_{VBUS_OVPZ}	V_{VBUS} falling		23.8	24.2	24.8	V
IBUS Over-Current Rising Threshold	I_{BUS_OCP}				8		A
BAT Voltage to Have Active I²C (No Source on VBUS and VAC)	V_{BAT_UVLOZ}	V_{BAT} rising, when the charger is in normal mode (without SFET)		2.3	2.5	2.7	V
	V_{BAT_UVLO}	V_{BAT} falling, when the charger is in normal mode (without SFET or SFET on)		2.1	2.3	2.5	
BATP Voltage to Have Active I²C (No Source on VBUS and VAC)	V_{BATP_UVLOZ}	V_{BATP} rising, when the charger is in ship mode (with SFET and SFET off)		3.1	3.3	3.5	V
	V_{BATP_UVLO}	V_{BATP} falling, when the charger is in ship mode (with SFET and SFET off)		2.85	3.05	3.25	

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VBUS Pin and VBAT Pin Power-Up							
BAT Voltage Rising Threshold to Enable OTG Mode	V_{BAT_OTG}	V_{BAT} rising		2.65	2.8	2.95	V
BAT Voltage Falling Threshold to Disable OTG Mode	V_{BAT_OTGZ}	V_{BAT} falling		2.35	2.5	2.65	V
Bad Adaptor Detection Threshold	V_{BAD_SRC}	V_{VBUS} falling		3.2	3.35	3.5	V
Bad Adaptor Detection Threshold Hysteresis		V_{VBUS} rising above V_{BAD_SRC}		200	250	300	mV
Bad Adaptor Detection Current	I_{BAD_SRC}				35		mA
Power Path Management							
System Voltage Regulation	V_{SYS_REG}	V_{BAT} > V_{SYSMIN}, charging disabled, offset above V_{BAT}			150		mV
		V_{BAT} < V_{SYSMIN}, offset above V_{SYSMIN}			200		
VSYS Over-Voltage Rising Threshold	V_{SYS_OVP}	As a percentage of the system regulation voltage, to turn off the converter	1-cell default	106.5	110	114.5	%
			2-4 cells default	107.5	110	112.5	
VSYS Over-Voltage Falling Threshold		As a percentage of the system regulation voltage, to re-enable the converter	1-cell default	96.5	100	104.5	%
			2-4 cells default	97.5	100	102.5	
VSYS Short Voltage Falling Threshold	V_{SYS_SHORT}			2.05	2.2	2.35	V
Battery Charger							
Charge Voltage Program Range	$V_{BAT_REG_RANGE}$			3		18.8	V
Charge Voltage Step	$V_{BAT_REG_STEP}$				10		mV
Charge Voltage Setting Accuracy	$V_{BAT_REG_ACC}$	Initial accuracy, T_J = -40℃ to +85℃	V_{REG} = 16.8V	-0.7		0.3	%
			V_{REG} = 12.6V	-0.25		0.25	
			V_{REG} = 8.4V	-0.4		0.6	
			V_{REG} = 4.2V	-0.5		1.1	
Charge Current Regulation Range	$I_{CHG_REG_RANGE}$			0.05		5	A
Charge Current Regulation Step	$I_{CHG_REG_STEP}$				10		mA
Charge Current Accuracy	I_{CHG_ACC}	V_{BAT} = 8V, initial accuracy, T_J = -40℃ to +85℃	I_{CHG} = 4A	-3		2	%
			I_{CHG} = 2A	-2.5		2.5	
			I_{CHG} = 1A	-2.5		5.5	
			I_{CHG} = 0.5A	-3		12	
Pre-Charge Current Regulation Setting	I_{PRECHG}			40		2000	mA
Pre-Charge Current Regulation Step	I_{PRECHG_STEP}				40		mA
LDO Mode Charge Current Accuracy when V_{BATP} below V_{SYSMIN}	I_{PRECHG_ACC}	V_{BAT} = 6.5V, initial accuracy, T_J = -40℃ to +85℃	I_{PRECHG} = 1000mA	920		1100	mA
			I_{PRECHG} = 480mA	450		500	
			I_{PRECHG} = 200mA	140		220	
			I_{PRECHG} = 120mA	55		135	

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Battery Charger							
Termination Current Regulation Setting	I_{TERM}			40		1000	mA
Termination Current Regulation Step	I_{TERM_STEP}				40		mA
Termination Current Accuracy	I_{TERM_ACC}	T_J = -40℃ to +85℃	I_{TERM} = 120mA	-25		15	%
			I_{TERM} = 480mA	-10		10	
Battery Short Voltage Rising Threshold to Start Pre-Charge	V_{BAT_SHORTZ}	V_{BAT} rising			2.3		V
Battery Short Voltage Falling Threshold to Stop Pre-Charge	V_{BAT_SHORT}	V_{BAT} falling			2.2		V
Battery Short Voltage Trickle Charging Current	I_{SHORT}	V_{BAT} < V_{BAT_SHORTZ}			80		mA
Battery Voltage Rising Threshold to Start Fast-Charge	$V_{BAT_LOWV_RISE}$	As percentage of V_{REG}, V_{BAT_LOWV} = 15.3%V_{REG}, VBAT_LOWV[1:0] = 00		14.6	15.3	16	%
		As percentage of V_{REG}, V_{BAT_LOWV} = 64%V_{REG}, VBAT_LOWV[1:0] = 01		62	64	66	
		As percentage of V_{REG}, V_{BAT_LOWV} = 68.7%V_{REG}, VBAT_LOWV[1:0] = 10		66.7	68.7	70.7	
		As percentage of V_{REG}, V_{BAT_LOWV} = 73.3%V_{REG}, VBAT_LOWV[1:0] = 11		71.3	73.3	75.3	
Battery Voltage Threshold to Stop Fast-Charge Hysteresis	$V_{BAT_LOWV_HYS}$	V_{BAT} falling, as percentage of V_{REG}, VBAT_LOWV[1:0] = 11			1.5		%
Battery Recharge Threshold	V_{RECHG}	V_{BAT} falling, VRECHG[3:0] = 0011, V_{REG} = 8.4V			200		mV
		V_{BAT} falling, VRECHG[3:0] = 0111, V_{REG} = 16.8V			400		
BATFET MOSFET On-Resistance from SYS to BAT	R_{ON_BATFET}	T_J = -40℃ to +85℃			11		mΩ
Battery Protections							
Battery Over-Voltage Threshold, When Battery Connected	V_{BAT_OVP}	V_{BAT} rising, as percentage of V_{REG}	1-cell default	102.5	104.5	106.5	%
			2-4 cells default	102.5	104	105.5	
		V_{BAT} falling, as percentage of V_{REG}	1-cell default	100.5	102.5	104.5	
			2-4 cells default	100.5	102	103.5	
Battery Short Voltage	V_{BAT_SHORT}	V_{BAT} falling, to clamp the charging current as trickle charging current			2.2		V
		V_{BAT} rising, to release the trickle charging current clamp			2.3		
Battery Discharging Over-Current Rising Threshold	I_{BAT_OCP}	With SFET configuration and EN_BATOC = 1			12		A
Input Voltage and Current Regulation (DPM: Dynamic Power Management)							
Input Voltage Regulation Limit	V_{INDPM}			3.6		22	V
Input Voltage Regulation Step	V_{INDPM_STEP}				100		mV
Input Voltage Regulation Accuracy	V_{INDPM_ACC}	V_{INDPM} = 18.6V		-2		2	%
		V_{INDPM} = 10.6V		-2		2	
		V_{INDPM} = 4.3V		-3		3	
Input Current Regulation Limit	I_{INDPM}			0.1		3.3	A
Input Current Regulation Step	I_{INDPM_STEP}				10		mA
Input Current Regulation Accuracy	I_{INDPM_ACC}	V_{VBUS} = 9V, initial accuracy	I_{INDPM} = 500mA	385	515	640	mA
			I_{INDPM} = 1000mA	850	980	1100	
			I_{INDPM} = 2000mA	1830	1920	2000	
			I_{INDPM} = 3000mA	2750	2850	2950	

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage and Current Regulation (DPM: Dynamic Power Management)						
Voltage Range for Input Current Regulation at ILIM_HIZ Pin	$V_{ILIM_REG_RNG}$		1		4	V
ILIM_HIZ Pin Leakage Current	I_{LEAK_ILIM}	V_{ILIM_HIZ} = 5.5V	-1		1	μA
D+/D- Detection						
D+ Voltage Source (600mV)	$V_{D+_600MVSRC}$		500	600	700	mV
D- Voltage Source (600mV)	$V_{D-_600MVSRC}$		500	600	700	mV
D+ Current Source (10μA)	$I_{D+_10UASRC}$	V_{D+} = 200mV	7	10	13	μA
D+ Current Sink (100μA)	$I_{D+_100UASNK}$	V_{D+} = 500mV	75	100	125	μA
D- Current Sink (100μA)	$I_{D-_100UASNK}$	V_{D-} = 500mV	75	100	125	μA
D+ Comparator Threshold for Secondary Detection	V_{D+_0P325}	D+ pin rising	250		400	mV
D- Comparator Threshold for Primary Detection	V_{D-_0P325}	D- pin rising	250		400	mV
D+ Comparator Threshold for Data Contact Detection	V_{D+_0P8}	D+ pin rising	850	900	950	mV
D+ Leakage Current	I_{D+_LKG}	HIZ mode	-1		1	μA
D- Leakage Current	I_{D-_LKG}	HIZ mode	-1		1	μA
D+ Comparator Threshold for Non-Standard Adaptor	V_{D+_2P8}	Combined $V_{D+_2P8_HI}$ and $V_{D+_2P8_LO}$	2.6		2.9	V
	V_{D+_2P0}	Combined $V_{D+_2P0_HI}$ and $V_{D+_2P0_LO}$	1.9		2.1	
	V_{D+_1P2}	Combined $V_{D+_1P2_HI}$ and $V_{D+_1P2_LO}$	1.1		1.4	
D- Comparator Threshold for Non-Standard Adaptor	V_{D-_2P8}	Combined $V_{D-_2P8_HI}$ and $V_{D-_2P8_LO}$	2.6		2.9	V
	V_{D-_2P0}	Combined $V_{D-_2P0_HI}$ and $V_{D-_2P0_LO}$	1.9		2.1	
	V_{D-_1P2}	Combined $V_{D-_1P2_HI}$ and $V_{D-_1P2_LO}$	1.1		1.4	
Thermal Regulation and Thermal Shutdown						
Junction Temperature Regulation Threshold	$T_{JUNCTION_REG}$	TREG[1:0] = 11 (120℃)		120		℃
		TREG[1:0] = 10 (100℃)		100		
		TREG[1:0] = 01 (80℃)		80		
		TREG[1:0] = 00 (60℃)		60		
Thermal Shutdown Rising Threshold	T_{SHUT}	Temperature increasing, TSHUT[1:0] = 00		150		℃
		Temperature increasing, TSHUT[1:0] = 01		130		
		Temperature increasing, TSHUT[1:0] = 10		120		
		Temperature increasing, TSHUT[1:0] = 11		85		
Thermal Shutdown Falling Hysteresis	T_{SHUT_HYS}	Temperature decreasing by T_{SHUT_HYS}		30		℃
JEITA Thermistor Comparator (Charge Mode)						
T1 Comparator Rising Threshold	V_{T1_RISE}	As percentage to V_{REGN} (0℃ w/ 103AT), charge suspended above this voltage	72.9	73.9	74.9	%
T1 Comparator Falling Threshold	V_{T1_FALL}	As percentage to V_{REGN} (3℃ w/ 103AT), charge re-enabled below this voltage	70.6	71.4	72.3	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
JEITA Thermistor Comparator (Charge Mode)							
T2 Comparator Rising Threshold	V_{T2_RISE}	As percentage to V_{REGN}	JEITA_T2 = 5℃ w/ 103AT	70.7	71.7	72.8	%
			JEITA_T2 = 10℃ w/ 103AT	67.9	69.1	70.4	
			JEITA_T2 = 15℃ w/ 103AT	64.9	66.1	67.4	
			JEITA_T2 = 20℃ w/ 103AT	61.8	63	64.2	
T2 Comparator Falling Threshold	V_{T2_FALL}	As percentage to V_{REGN}	JEITA_T2 = 5℃ w/ 103AT	68.6	69.4	70.3	%
			JEITA_T2 = 10℃ w/ 103AT	65.8	66.7	67.6	
			JEITA_T2 = 15℃ w/ 103AT	62.9	63.8	64.7	
			JEITA_T2 = 20℃ w/ 103AT	59.9	60.8	61.7	
T3 Comparator Rising Threshold	V_{T3_RISE}	As percentage to V_{REGN}	JEITA_T3 = 40℃ w/ 103AT	49.4	50.2	51.1	%
			JEITA_T3 = 45℃ w/ 103AT	45.9	46.6	47.5	
			JEITA_T3 = 50℃ w/ 103AT	42.2	42.9	43.7	
			JEITA_T3 = 55℃ w/ 103AT	38.7	39.5	40.3	
T3 Comparator Falling Threshold	V_{T3_FALL}	As percentage to V_{REGN}	JEITA_T3 = 40℃ w/ 103AT	47.6	48.3	49.1	%
			JEITA_T3 = 45℃ w/ 103AT	43.9	44.7	45.6	
			JEITA_T3 = 50℃ w/ 103AT	40.3	41.1	42	
			JEITA_T3 = 55℃ w/ 103AT	36.8	37.6	38.5	
T4 Comparator Falling Threshold	V_{T4_FALL}	As percentage to V_{REGN} (60℃ w/ 103AT), charge suspended below this voltage		33.4	34	34.7	%
T4 Comparator Rising Threshold	V_{T4_RISE}	As percentage to V_{REGN} (58℃ w/ 103AT), charge is re-enabled above this voltage		35.2	35.8	36.5	%
Cold or Hot Thermistor Comparator (OTG Mode)							
T_{COLD} Comparator Rising Threshold	V_{BCOLD_RISE}	As percentage to V_{REGN} (-20℃ w/ 103AT)		79.5	80.4	81.3	%
		As percentage to V_{REGN} (-10℃ w/ 103AT)		76.5	77.5	78.3	
T_{COLD} Comparator Falling Threshold	V_{BCOLD_FALL}	As percentage to V_{REGN} (-20℃ w/ 103AT)		77.6	78.4	79.1	%
		As percentage to V_{REGN} (-10℃ w/ 103AT)		74.7	75.4	76.2	
T_{HOT} Comparator Falling Threshold	V_{BHOT_FALL}	As percentage to V_{REGN} (55℃ w/ 103AT)		37.1	37.6	38.1	%
		As percentage to V_{REGN} (60℃ w/ 103AT)		33.8	34.3	34.8	
		As percentage to V_{REGN} (65℃ w/ 103AT)		30.7	31.2	31.7	
T_{HOT} Comparator Rising Threshold	V_{BHOT_RISE}	As percentage to V_{REGN} (55℃ w/ 103AT)		39.1	39.6	40.1	%
		As percentage to V_{REGN} (60℃ w/ 103AT)		35.5	36	36.5	
		As percentage to V_{REGN} (65℃ w/ 103AT)		32.2	32.8	33.5	
Switching Converter							
PWM Switching Frequency	f_{SW}	PWM_FREQ = 0		1.3	1.5	1.7	MHz
		PWM_FREQ = 1		650	750	850	kHz
Sense Resistance and MOSFET R_{DSON}							
VBUS to PMID Input Sensing Resistance	R_{SNS}	T_J = -40℃ to +85℃			11		mΩ
Buck High-side Switching MOSFET On-Resistance between PMID and SW1 - Q1	R_{Q1_ON}	T_J = -40℃ to +85℃			21		mΩ
Buck Low-side Switching MOSFET On-Resistance between SW1 and GND - Q2	R_{Q2_ON}	T_J = -40℃ to +85℃			33		mΩ
Boost Low-side Switching MOSFET On-Resistance between SW2 and GND - Q3	R_{Q3_ON}	T_J = -40℃ to +85℃			25		mΩ
Boost High-side Switching MOSFET On-Resistance between SW2 and SYS - Q4	R_{Q4_ON}	T_J = -40℃ to +85℃			17		mΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OTG Mode Converter							
Typical OTG Mode Voltage Regulation Range	V_{OTG_RANGE}			2.8		22	V
Typical OTG Mode Voltage Regulation Step	V_{OTG_STEP}				10		mV
OTG Mode Voltage Regulation Accuracy	V_{OTG_ACC}	I_{VBUS} = 0A	V_{OTG} = 5V	-2		3	%
			V_{OTG} = 12V	-2		2.5	
			V_{OTG} = 20V	-2.5		2	
Typical OTG Mode Current Regulation Range	I_{OTG_RANGE}			0.12		3.32	A
Typical OTG Mode Current Regulation Step	I_{OTG_STEP}				40		mA
OTG Mode Current Regulation Accuracy	I_{OTG_ACC}	I_{OTG} = 3A		2700		3300	mA
		I_{OTG} = 1.52A		1320		1770	
		I_{OTG} = 0.52A		340		730	
OTG Mode Under-Voltage Falling Threshold	V_{OTG_UVP}			2.05	2.2	2.35	V
OTG Mode Over-Voltage Rising Threshold	V_{OTG_OVP}	As percentage of V_{OTG} regulation, OTG mode, OOA disabled		109	113	117	%
OTG Mode Over-Voltage Falling Threshold		As percentage of V_{OTG} regulation		94	98	102	%
Battery Current Regulation in OTG Mode	I_{OTG_BAT}	V_{BAT} = 8V, V_{OTG} = 9V	IBAT_REG[1:0] = 00	2.85	3	3.15	A
			IBAT_REG[1:0] = 01	3.8	4	4.2	
			IBAT_REG[1:0] = 10	4.75	5	5.2	
REGN LDO							
REGN LDO Output Voltage	V_{REGN}	V_{VBUS} = 5V, I_{REGN} = 20mA		4.45	4.7	4.85	V
		V_{VBUS} = 15V, I_{REGN} = 20mA		4.65	5	5.35	
REGN LDO Current Limit	I_{REGN}	V_{VBUS} = 5V, V_{REGN} = 4.5V		25			mA
I²C Interface Characteristics (SCL, SDA)							
Input High Threshold Level (SDA)	V_{IH_SDA}			1.3			V
Input Low Threshold Level (SDA)	V_{IL_SDA}					0.4	V
Output Low Threshold Level (SDA)	V_{OL_SDA}	Sink current = 5mA				0.4	V
High-Level Leakage Current (SDA)	I_{BIAS_SDA}	Pull up rail 1.8V				1	μA
Input High Threshold Level (SCL)	V_{IH_SCL}			1.3			V
Input Low Threshold Level (SCL)	V_{IL_SCL}					0.4	V
High-Level Leakage Current (SCL)	I_{BIAS_SCL}	Pull up rail 1.8V				1	μA
Logic Input Pin Characteristics (nCE, ILIM_HIZ, nQON)							
Input High Threshold (nCE)	V_{IH_CE}			1.3			V
Input Low Threshold (nCE)	V_{IL_CE}					0.4	V
High-Level Leakage Current (nCE)	$I_{IN_BIAS_CE}$	Pull up rail 1.8V				1	μA
Input High Threshold (nQON)	V_{IH_QON}			1.3			V
Input Low Threshold (nQON)	V_{IL_QON}					0.4	V
Internal nQON Pull-Up	V_{QON}	nQON is pulled up internally			4		V
Internal nQON Pull-Up Resistance	R_{QON}				250		kΩ
Input High Threshold (ILIM_HIZ)	$V_{IH_ILIM_HIZ}$			1.1			V
Input Low Threshold (ILIM_HIZ)	$V_{IL_ILIM_HIZ}$					0.7	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Output Pin Characteristics (nINT, STAT)						
Output Low Threshold (nINT)	V_{OL_INT}	Sink current = 5mA			0.4	V
High-Level Leakage Current (nINT)	$I_{OUT_BIAS_INT}$	Pull up rail 1.8V			1	μA
Output Low Threshold (STAT)	V_{OL_STAT}	Sink current = 5mA			0.4	V
High-Level Leakage Current (STAT)	$I_{OUT_BIAS_STAT}$	Pull up rail 1.8V			1	μA
ADC Measurement Accuracy and Performance						
Conversion-Time, Each Measurement	t_{ADC_CONV}	ADC_SAMPLE[1:0] = 00		8		ms
		ADC_SAMPLE[1:0] = 01		4		
		ADC_SAMPLE[1:0] = 10		2		
		ADC_SAMPLE[1:0] = 11		1		
Effective Resolution	ADC_{RES}	ADC_SAMPLE[1:0] = 00	14	15		bits
		ADC_SAMPLE[1:0] = 01	13	14		
		ADC_SAMPLE[1:0] = 10	12	13		
		ADC_SAMPLE[1:0] = 11	10	11		
ADC Measurement Range and LSB						
ADC BUS Current Reading (Both Forward and OTG)	IBUS_ADC	Range	0		5	A
		LSB		1		mA
ADC BUS Voltage Reading	VBUS_ADC	Range	0		30	V
		LSB		1		mV
ADC VAC Voltage Reading	VAC_ADC	Range	0		30	V
		LSB		1		mV
ADC BAT Voltage Reading	VBAT_ADC	Range	0		20	V
		LSB		1		mV
ADC SYS Voltage Reading	VSYS_ADC	Range	0		24	V
		LSB		1		mV
ADC BAT Current Reading	IBAT_ADC	Range	0		8	A
		LSB		1		mA
ADC TS Voltage Reading	TS_ADC	Range	0		99.9	%
		LSB		0.098		%
ADC Die Temperature Reading	TDIE_ADC	Range	-40		150	℃
		LSB		0.5		℃

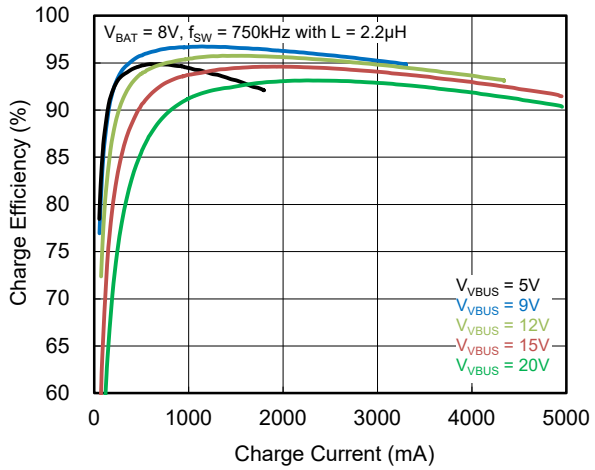
TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Battery Charger						
Typical Top-Off Timer Accuracy	t_{TOP_OFF}	TOPOFF_TMR[1:0] = 01	12	15	18	min
		TOPOFF_TMR[1:0] = 10	24	30	36	
		TOPOFF_TMR[1:0] = 11	36	45	54	
Charge Safety Timer in Trickle Charge	t_{SAFETY_TRKCHG}		0.9	1	1.1	h
Charge Safety Timer in Pre-Charge	t_{SAFETY_PRECHG}	PRECHG_TMR = 0 (2h)	1.8	2	2.2	h
Charge Safety Timer Accuracy	t_{SAFETY}	CHG_TMR[1:0] = 00 (5h)	4.5	5	5.5	h
		CHG_TMR[1:0] = 01 (8h)	7.2	8	8.8	
		CHG_TMR[1:0] = 10 (12h)	10.8	12	13.2	
		CHG_TMR[1:0] = 11 (24h)	21.3	24	26.4	
I²C Interface						
SCL Clock Frequency	f_{SCL}				1000	kHz
Watchdog Timer						
Watchdog Reset Time	t_{LP_WDT}	EN_HIZ = 1, WATCHDOG[2:0] = 111 (160s)	100	160		s
	t_{WDT}	EN_HIZ = 0, WATCHDOG[2:0] = 111 (160s)	136	160		

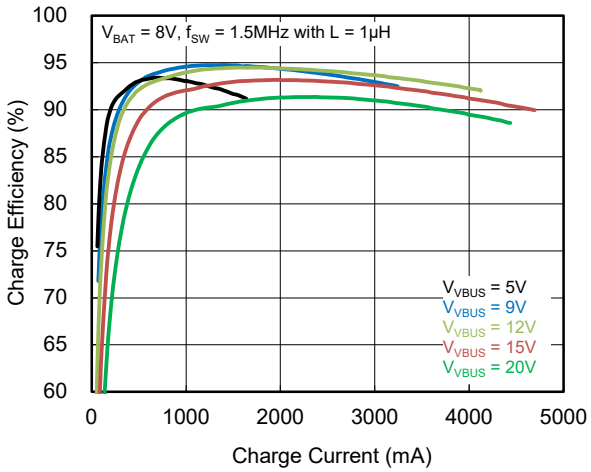
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, C_{VBUS} = 3 × 10μF, C_{PMID} = 10μF, C_{SYS} = 5 × 10μF, C_{BAT} = 2 × 10μF, L = 1μH when f_{SW} = 1.5MHz and L = 2.2μH when f_{SW} = 750kHz, unless otherwise noted.

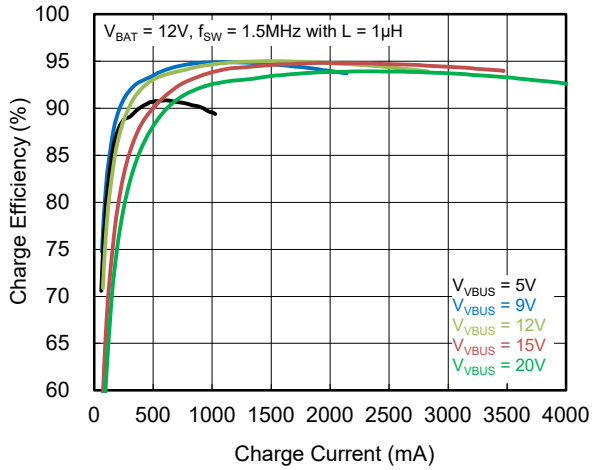
2-Cell Battery Charge Efficiency vs. Charge Current



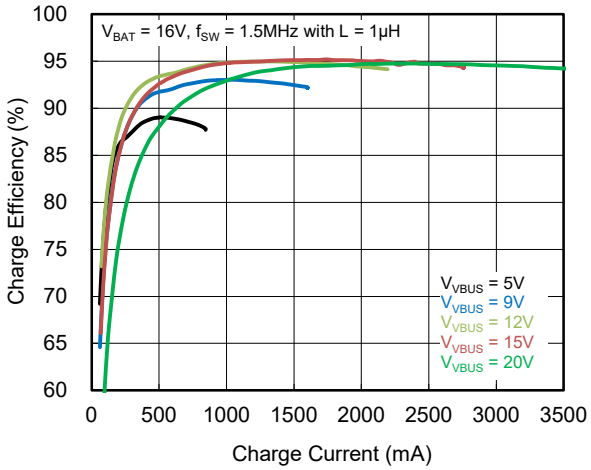
2-Cell Battery Charge Efficiency vs. Charge Current



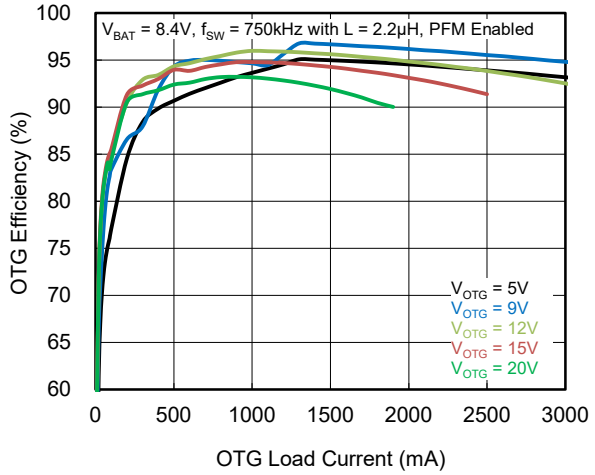
3-Cell Battery Charge Efficiency vs. Charge Current



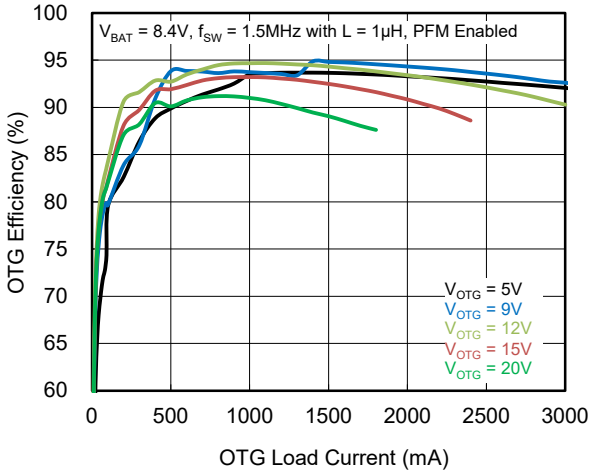
4-Cell Battery Charge Efficiency vs. Charge Current



2-Cell Battery OTG Efficiency vs. OTG Load Current



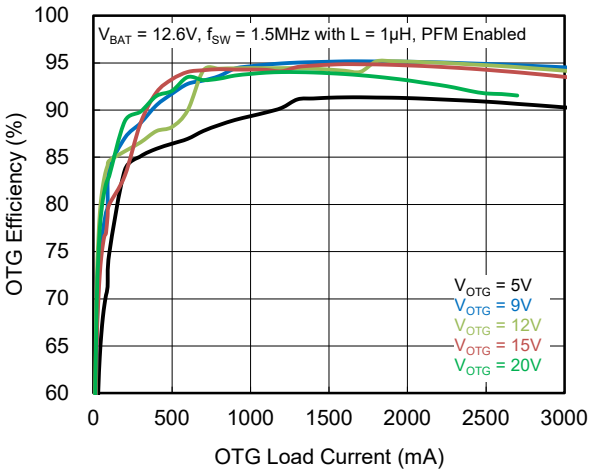
2-Cell Battery OTG Efficiency vs. OTG Load Current



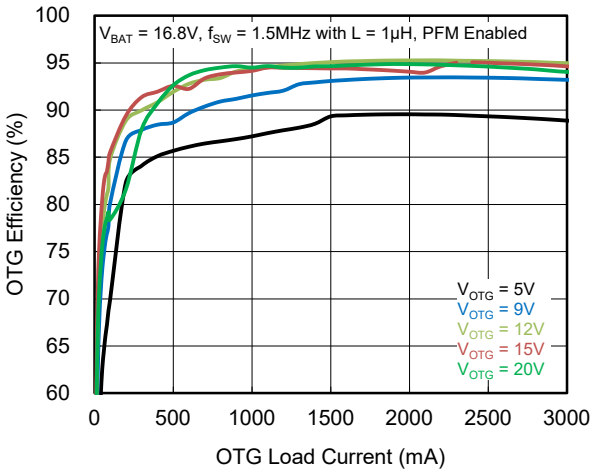
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, C_{VBUS} = 3 × 10μF, C_{PMID} = 10μF, C_{SYS} = 5 × 10μF, C_{BAT} = 2 × 10μF, L = 1μH when f_{SW} = 1.5MHz and L = 2.2μH when f_{SW} = 750kHz, unless otherwise noted.

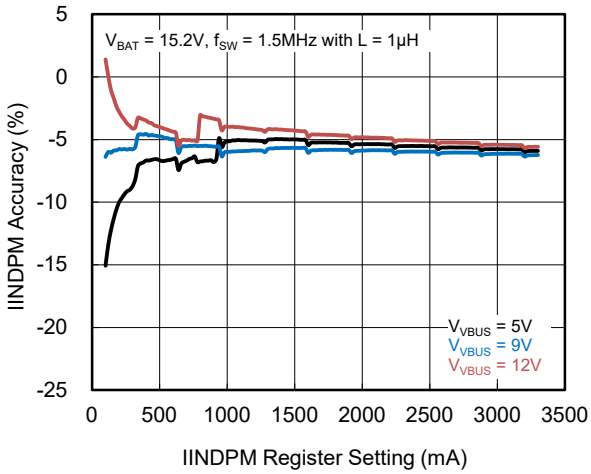
3-Cell Battery OTG Efficiency vs. OTG Load Current



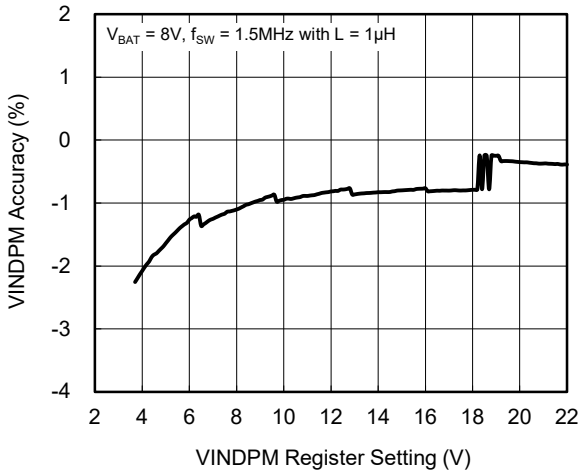
4-Cell Battery OTG Efficiency vs. OTG Load Current



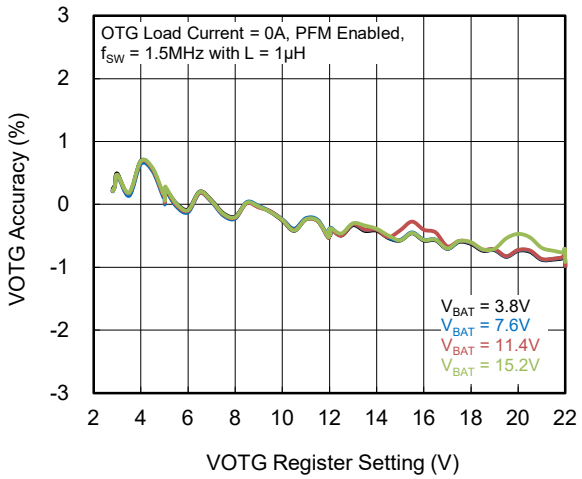
IINDPM Setting Accuracy



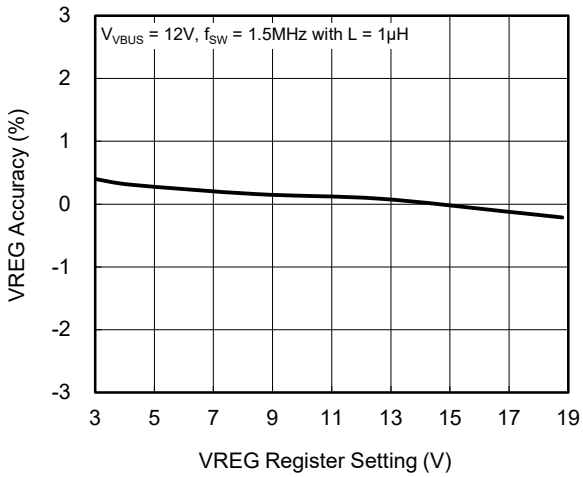
VINDPM Setting Accuracy



OTG Voltage Regulation (VOTG) Accuracy



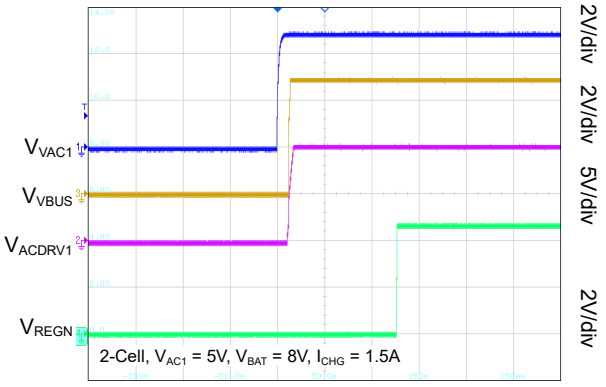
Charge Voltage Setting Accuracy



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

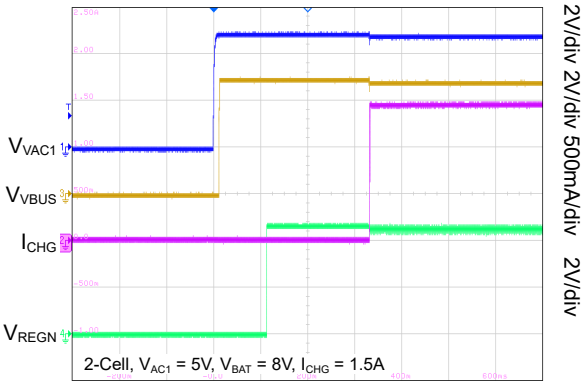
T_J = +25℃, C_{VBUS} = 3 × 10μF, C_{PMID} = 10μF, C_{SYS} = 5 × 10μF, C_{BAT} = 2 × 10μF, L = 1μH when f_{SW} = 1.5MHz and L = 2.2μH when f_{SW} = 750kHz, unless otherwise noted.

VAC1 Power-Up with ACFET1-RBFET1



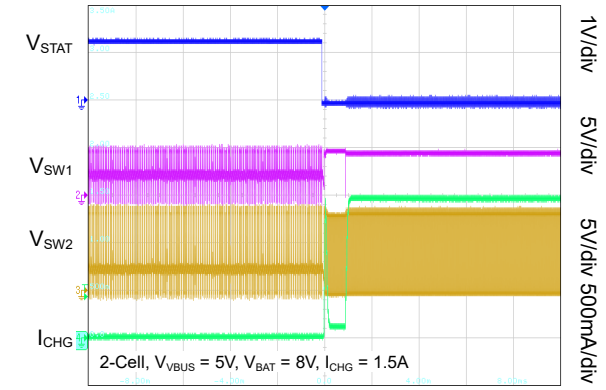
Time (50ms/div)

VAC1 Power-Up with Charge Enabled



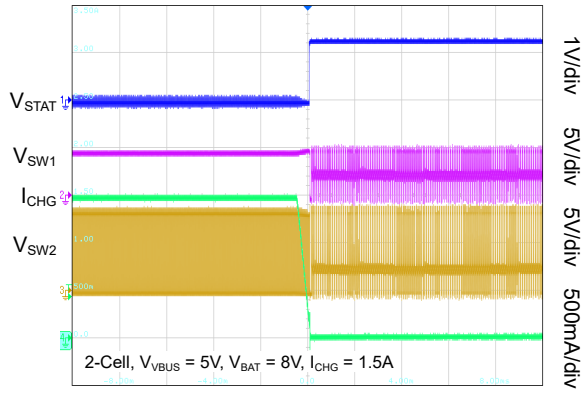
Time (100ms/div)

Charge Enabled



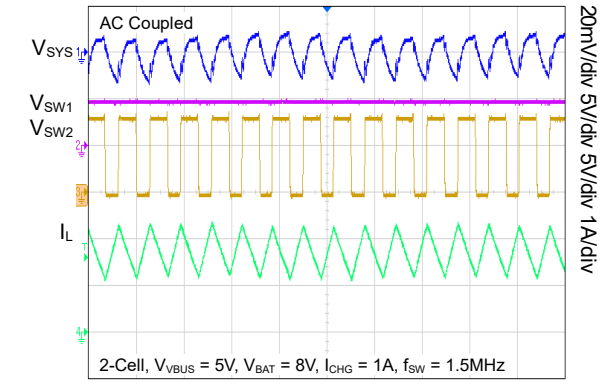
Time (2ms/div)

Charge Disabled



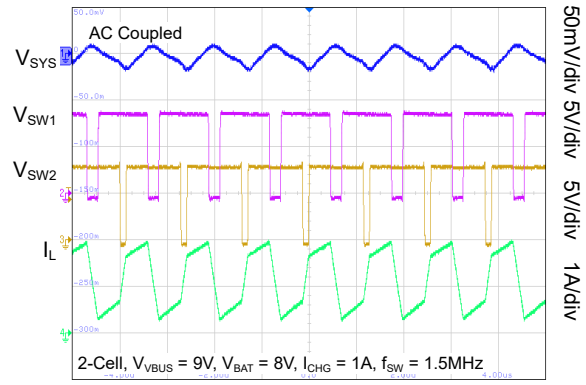
Time (2ms/div)

Boost Charging Mode PWM Operation



Time (1μs/div)

Buck-Boost Charging Mode PWM Operation

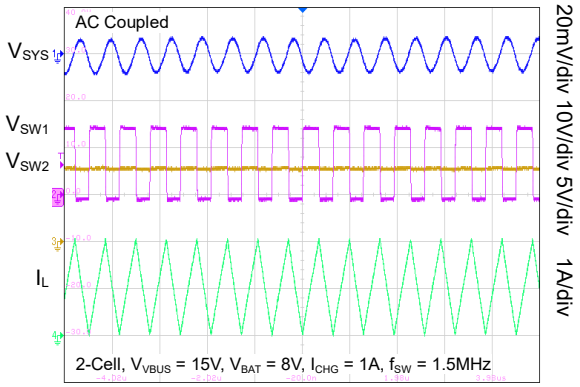


Time (1μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

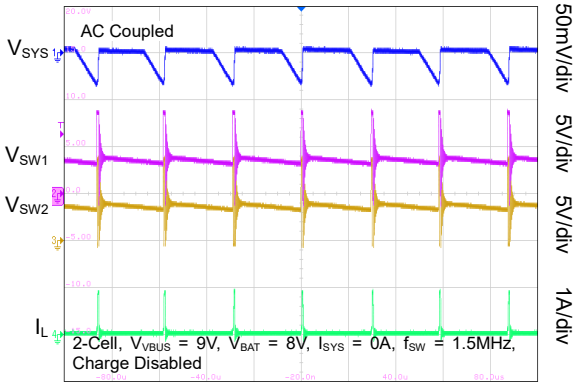
T_J = +25℃, C_{VBUS} = 3 × 10μF, C_{PMID} = 10μF, C_{SYS} = 5 × 10μF, C_{BAT} = 2 × 10μF, L = 1μH when f_{SW} = 1.5MHz and L = 2.2μH when f_{SW} = 750kHz, unless otherwise noted.

Buck Charging Mode PWM Operation



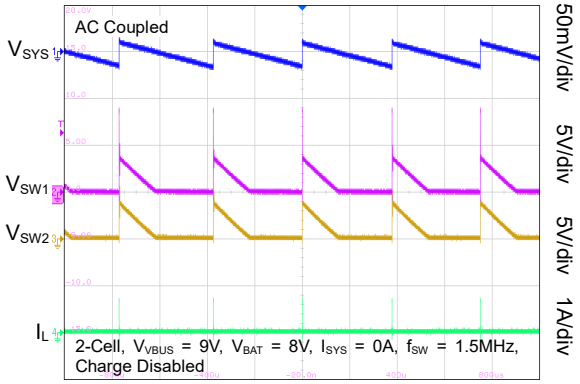
Time (1μs/div)

Buck-Boost PFM Operation with OOA



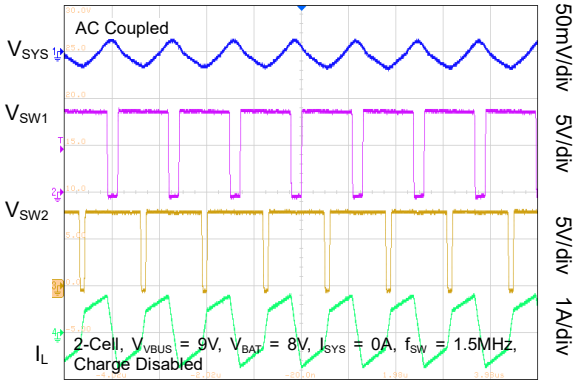
Time (20μs/div)

Buck-Boost PFM Operation without OOA



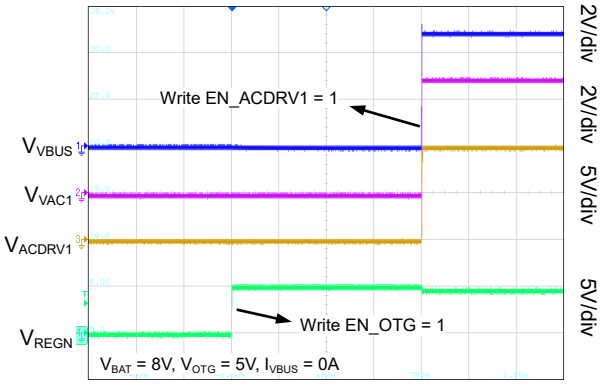
Time (200μs/div)

Buck-Boost Operation with PFM Disabled



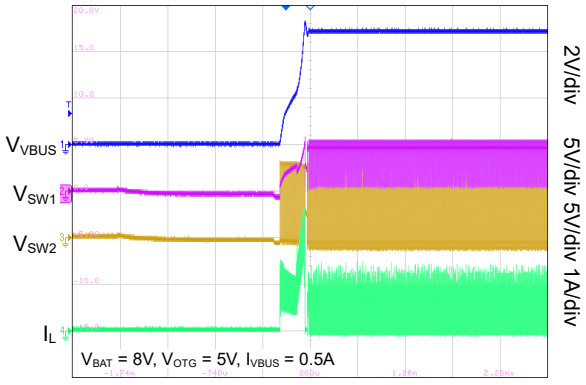
Time (1μs/div)

OTG Startup with ACFET1-RBFET1



Time (200ms/div)

OTG Startup with 500mA Load

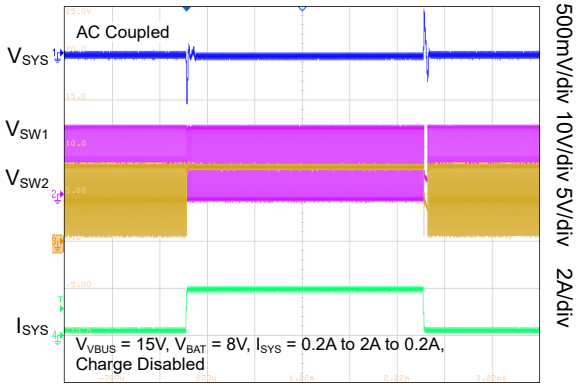


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

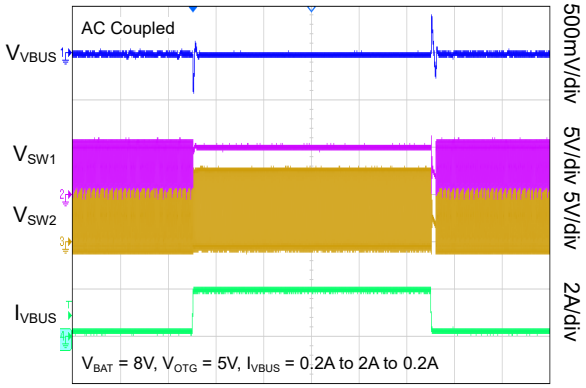
T_J = +25℃, C_{VBUS} = 3 × 10μF, C_{PMID} = 10μF, C_{SYS} = 5 × 10μF, C_{BAT} = 2 × 10μF, L = 1μH when f_{SW} = 1.5MHz and L = 2.2μH when f_{SW} = 750kHz, unless otherwise noted.

System Load Transient Response



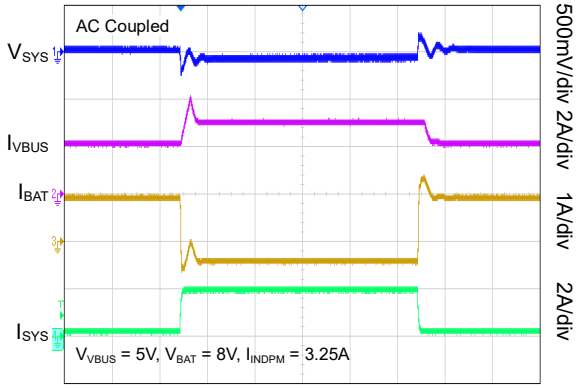
Time (500μs/div)

OTG Load Transient Response



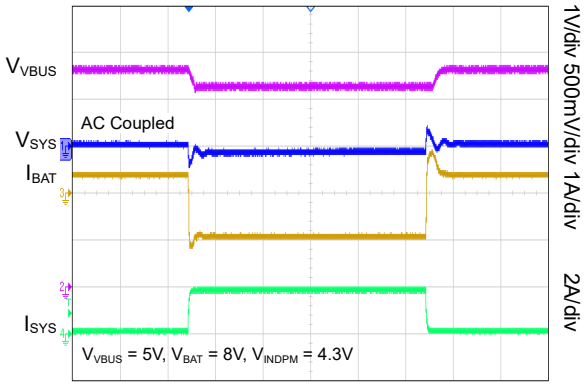
Time (500μs/div)

IINDPM Transient Response



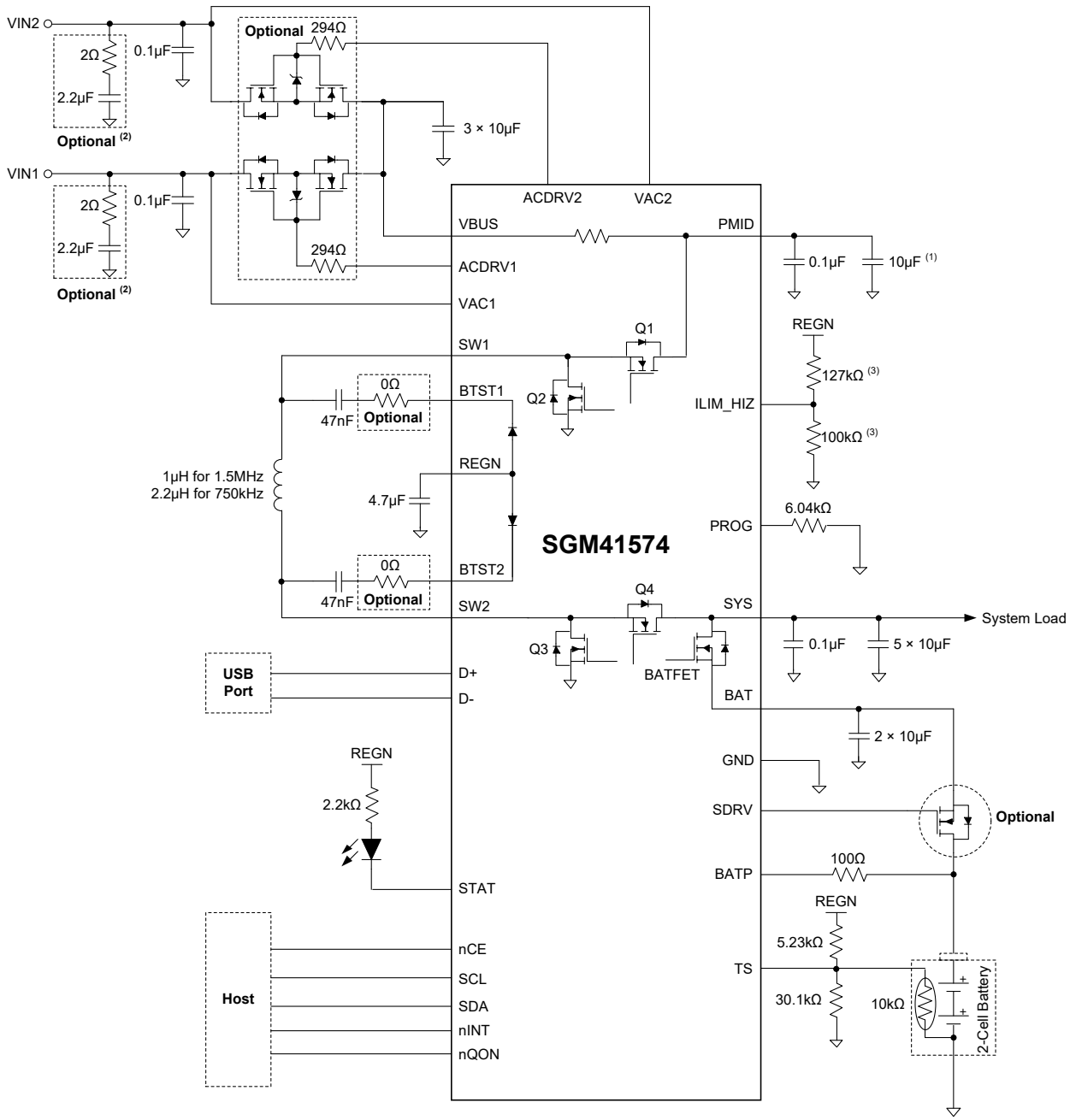
Time (500μs/div)

VINDPM Transient Response



Time (500μs/div)

TYPICAL APPLICATION CIRCUITS



NOTES:

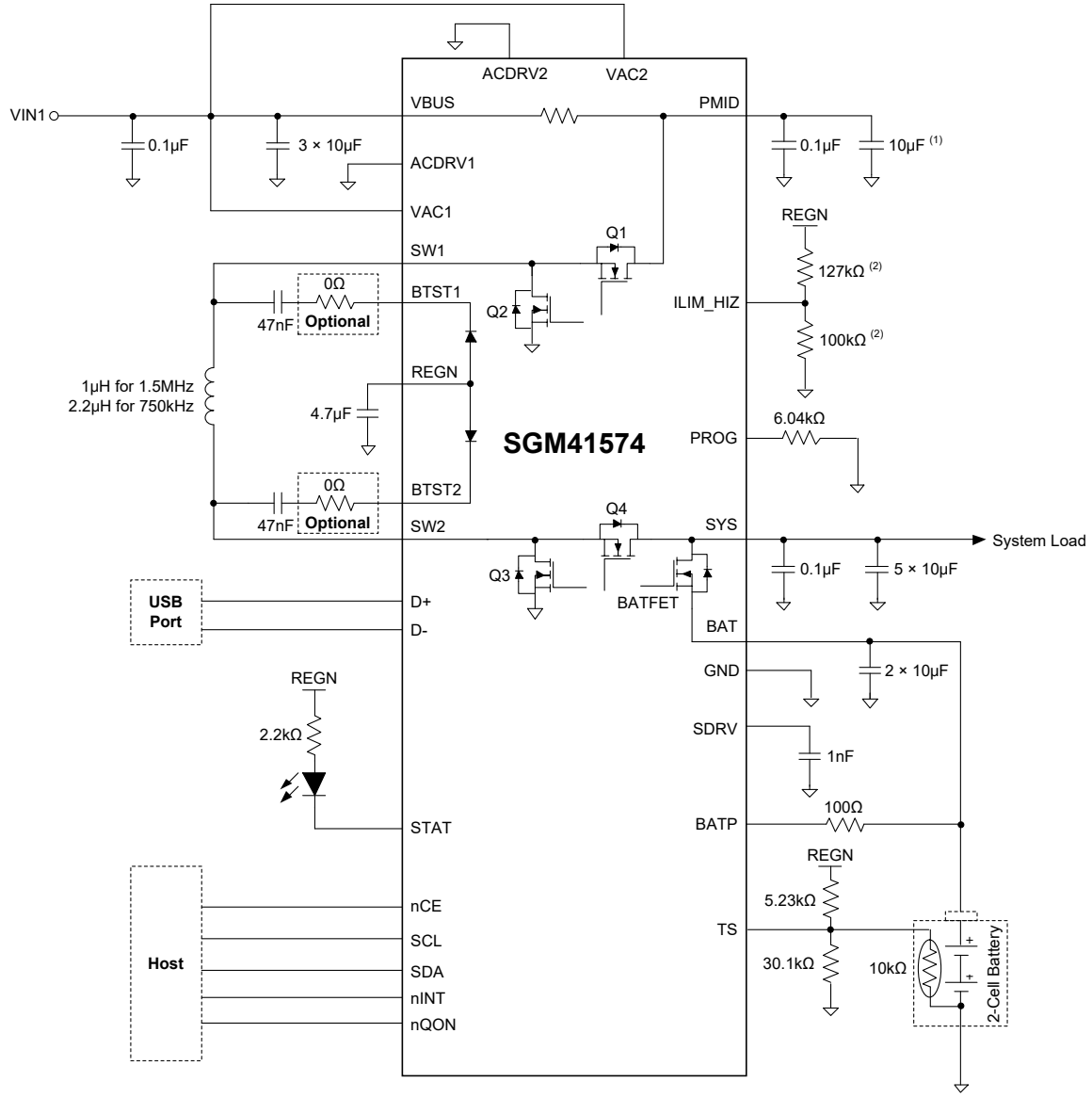
1. A typical 10mΩ resistor is connected internally between VBUS and PMID pins for current sensing capability. In some applications (such as high-voltage adapter hot plug-in or surge test), VBUS/PMID voltage power-up/down rapidly. During this period, a transient high current flows through the resistor. Once the transient peak current exceeds 60A, the resistor risks damage, thereby affecting the current sensing accuracy. The transient current is proportional to the voltage change slew rate and the PMID effective capacitance. Therefore, the capacitor placed at PMID pin cannot be too large. It is recommended to connect only one 10μF/25V/0805 ceramic capacitor and one 0.1μF ceramic capacitor from PMID pin to GND close to the device.

2. If the ACFET-RBFET is installed, adding an RC snubber helps suppress the input voltage spike when hot plugging adapter.

3. For the 127kΩ and 100kΩ resistor divider, the maximum input current limit is set to about 1.5A. If a higher input current limit is required, the resistor ratio needs to be adjusted.

Figure 1. Typical Application Circuit with Two Input Sources and Ship FET

TYPICAL APPLICATION CIRCUITS (continued)



NOTES:

1. A typical 10mΩ resistor is connected internally between VBUS and PMID pins for current sensing capability. In some applications (such as high-voltage adapter hot plug-in or surge test), VBUS/PMID voltage power-up/down rapidly. During this period, a transient high current flows through the resistor. Once the transient peak current exceeds 60A, the resistor risks damage, thereby affecting the current sensing accuracy. The transient current is proportional to the voltage change slew rate and the PMID effective capacitance. Therefore, the capacitor placed at PMID pin cannot be too large. It is recommended to connect only one 10μF/25V/0805 ceramic capacitor and one 0.1μF ceramic capacitor from PMID pin to GND close to the device.

2. For the 127kΩ and 100kΩ resistor divider, the maximum input current limit is set to about 1.5A. If a higher input current limit is required, the resistor ratio needs to be adjusted.

Figure 2. Typical Application Circuit with Single Input Source and No Ship FET

FUNCTIONAL BLOCK DIAGRAM

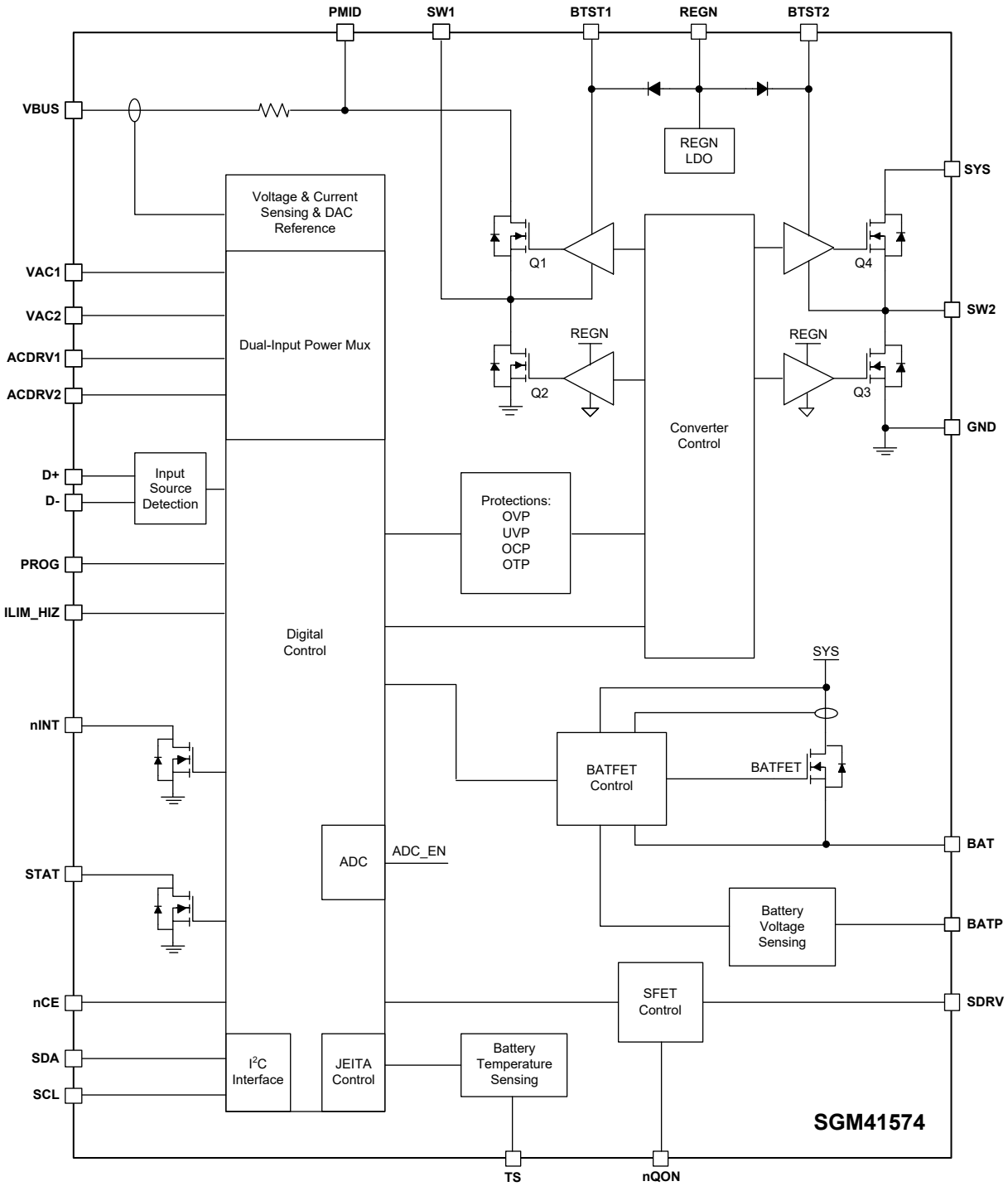


Figure 3. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM41574 is an integrated 4 switching MOSFETs Buck-Boost battery charger and system power path management device for 1-4 cells Li-Ion or Li-polymer batteries. Its low-impedance power path optimizes efficiency, reduces battery charging time, and extends battery life. I²C programming makes it a flexible powering and charger design solution.

The SGM41574 can detect the input source types which include SDP/CDP/DCP and non-standard adaptor through the D+/D- pins following USB BC1.2 Specification. It provides D+/D- handshake to support fast charging with the adjustable high voltage adaptor (HVDCP).

To support 1-4 cells Li-Ion battery charging, the SGM41574 automatically works at Buck, Boost or Buck-Boost configurations according to the adaptor voltage and battery voltage. The SGM41574 supports two different input sources with its dual input source selector management.

The SGM41574 employs narrow VDC architecture (NVDC) with BATFET separating system from the battery. Even without battery or with a fully depleted battery, the system is regulated to above the minimum system voltage. The SGM41574 features a Dynamic Power Management (DPM) to avoid input adaptor overloading or to meet the maximum current limit. It keeps the system voltage regulated to its minimum setting in DPM mode by reducing the charge current. The SGM41574 also provides supplement mode to further support system output in case that charge current decreased to zero and input is still overload. The SGM41574 can provide maximum power point with an algorithm called input current optimizer (ICO) to avoid the input source overload.

The SGM41574 supports the default mode (standalone) without host control. It automatically detects the battery voltage and starts the charge. A charge cycle automatically terminates when a full charge is detected if the device is not in thermal regulation or DPM mode. The charger automatically initiates a new charging cycle if battery voltage falls below the recharge threshold.

The SGM41574 supports USB On-The-Go (OTG) operation by supplying default 5V on the VBUS with an output current limit up to 3.32A. To support the programmable power supply (PPS) feature defined by the USB-PD 3.0 Specifications, the OTG voltage is programmable from 2.8V to 22V with 10mV resolution.

To save the power from battery to system, the SGM41574 provides an SDRV pin to control an external N-channel ship FET. Host can set charger to ship mode or shutdown mode to reduce the leakage current from battery by I²C.

The SGM41574 provides full protections for safety of battery charging and system operation, including battery temperature monitoring, charging safety timer, over-current and over-voltage protections. When any fault occurs, the SGM41574 asserts an nINT pulse to notify the host.

The SGM41574 provides integrated 16-bit ADC for monitoring input voltage, input current, battery voltage, charge current, system voltage, battery temperature and die temperature.

Power-On Reset (POR)

When V_{VBUS} > V_{VBUS_UVLOZ} or V_{BAT} > V_{BAT_UVLOZ}, the integrated selector chooses the higher power to supply the internal bias circuits. If both VBUS and VBAT are invalid, and the V_{VAC1} > $V_{VAC_PRESENT}$ or V_{VAC2} > $V_{VAC_PRESENT}$, the internal bias circuits will be powered from the first present power of V_{VAC1} and V_{VAC2}.

Once there is a valid input voltage provided at SGM41574, the device starts the power-on reset (POR) detection after a 5ms delay. Then the device sets the POR registers according to the ACFET-RBFET presence detection and PROG resistance detection results. The host can write or read the I²C registers 20ms later after the valid power provided. There is an nINT pulse to signal I²C ready to communicate.

DETAILED DESCRIPTION (continued)

PROG Pin Configuration

The SGM41574 has a default switching frequency and battery cell count setting after power-on. These configurations come from the PROG resistance detection result during POR period. Also, the VSYSMIN[5:0], ICHG[8:0] and VREG[10:0] registers are configured to the according default setting associated with the battery cell count. Table 1 and Table 2 give the relationship between POR setting and PROG pin resistance. It is recommended to use 1% or 2% SMT resistor on PROG pin.

The VSYSMIN[5:0] and ICHG[8:0] registers can be changed to any values within the registers define range by host after POR. But the VREG programmable range is limited by the CELL[1:0] register setting, which is shown in Table 2. The SGM41574 ignores any write out of the VREG range. When the REG_RST bit is set, the VSYSMIN[5:0], ICHG[8:0] and VREG[10:0] registers are returned to POR default values.

If the host changes the CELL[1:0] register after POR, the VSYSMIN[5:0], ICHG[8:0] and VREG[10:0] registers are automatically reset to the new default values associated with the updated CELL[1:0] register setting. The CELL[1:0] register cannot be reset by REG_RST or watchdog timer.

Power-Up from Battery Only (No Input Source)

When there is no other input source, but only the battery is present, and the voltage is higher than the UVLO threshold (V_{BAT_UVLOZ}), the BATFET turns on to connect the system to the battery. The quiescent current is minimum because the REGN LDO remains off. Conduction losses are also low due to small R_{DSON} of BATFET. Low losses help to extend the battery run time. The discharge current through BATFET is continuously monitored. The sequences of actions when battery is only powered up are:

1. ACFET-RBFET presence detection, PROG pin resistance detection and set the POR registers.
2. Host can write or read the I²C registers 20ms later after the valid battery voltage is provided.
3. BATFET turns on.

Table 1. POR Switching Frequency and Battery Cell Count Configuration by PROG Pin Resistance

Typical Resistance at PROG Pin	Switching Frequency	Cell Count
3.0kΩ	1.5MHz	1 Cell
4.7kΩ	750kHz	1 Cell
6.04kΩ	1.5MHz	2 Cells
8.2kΩ	750kHz	2 Cells
10.5kΩ	1.5MHz	3 Cells
13.7kΩ	750kHz	3 Cells
17.4kΩ	1.5MHz	4 Cells
27.0kΩ	750kHz	4 Cells

Table 2. POR Charging Setting Associated with Battery Cell Count

Charging Parameters	CELL[1:0] (REG0x0A[7:6])			
	1-Cell	2-Cell	3-Cell	4-Cell
VSYSMIN[5:0] (REG0x00[5:0])	3.5V	7V	9V	12V
ICHG[8:0] (REG0x03/04)	2A	2A	1A	1A
VREG[10:0] (REG0x01/02)	4.2V	8.4V	12.6V	16.8V
VREG Range	3V - 4.99V	5V - 9.99V	10V - 13.99V	14V - 18.8V

DETAILED DESCRIPTION (continued)

Power-Up Process from the Input Power Source

Upon connection of a valid input source (V_{VBUS} > $V_{VBUS_PRESENT}$ or V_{VACx} > $V_{VAC_PRESENT}$), the input source from VBUS pin is checked to turn on the internal REGN LDO regulator and the bias circuits (whether the battery is present or not). Before the Buck-Boost converter starts switching, the SGM41574 detects and sets the input current limit threshold. The sequences of actions when VBUS as input source is powered up are:

1. ACFET-RBFET presence detection, PROG pin resistance detection and set the POR registers.
2. The ACDRVx pin changes to high if the ACFETx-RBFETx is detected. If both ACFETx-RBFETx are detected, turn on which VAC comes first.
3. Host can write or read the I²C registers 20ms later after the valid input voltage is provided.
4. The SGM41574 sets the VBUS_PRESENT_STAT bit to 1 when detecting V_{VBUS} > $V_{VBUS_PRESENT}$. And it turns on REGN after 128ms delay.
5. The SGM41574 starts the poor source detection after the REGN on.
6. After passing poor source detection, the ADC reads the V_{VBUS} to update the VINDPM, and reads the V_{ILIM_HIZ} to clamp the IINDPM to use. At the same time, the SGM41574 starts the input source type detection, and then updates the VBUS_STAT[3:0] and IINDPM[8:0] registers.
7. The Buck-Boost converter starts switching.

Dual-Input Power Path Management

To select and manage the power from two different input sources, the SGM41574 provides two ACDRVx pins to control the external N-channel ACFET-RBFET. During POR, the internal bias circuit detects the ACFETx-RBFETx presence, and then updates the ACRBx_STAT status bit accordingly. The ACDRVx is controlled by the associated EN_ACDRVx bits. According to the different application cases, SGM41574 provides below 3 connections for input source selection.

Single Input without ACFET-RBFET

In one input source configuration, the external ACFETx-RBFETx are not required. Both VAC1 and VAC2 need to be connected to VBUS directly. ACDRV1 and ACDRV2 are pulled down to ground, as shown in Figure 4.

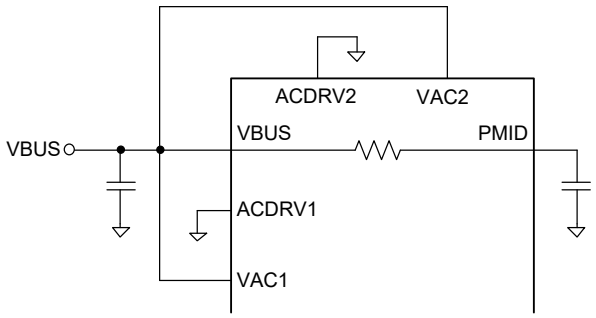


Figure 4. Single Input without ACFET-RBFET

During POR, the SGM41574 detects that no ACFETx-RBFETx are populated, updates the ACRB1_STAT and ACRB2_STAT bits to 0, and locks both EN_ACDRV1 and EN_ACDRV2 bits to 0.

Single or Dual Input with ACFET1-RBFET1

In this configuration, ACFET1-RBFET1 is populated, and ACFET2-RBFET2 is not populated. As shown in Figure 5, VAC1 is tied to ACFET1's drain end, and ACDRV1 is tied to ACFET1-RBFET1's gate end. VAC2 is shorted to the VBUS and ACDRV2 is pulled low to ground. This structure is able to support either single input or dual input application.

Single input: One from VAC1, or one from VBUS directly.
Dual input: One from VAC1, the other one from VBUS directly.

1. During POR, the SGM41574 detects that ACFET1-RBFET1 is populated and ACFET2-RBFET2 is not populated, then ACRB1_STAT is updated to 1 and ACRB2_STAT remains 0.

2. The charger locks the EN_ACDRV2 bit to 0, and the ACDRV2 pin always stays low.

3. After V_{VAC1} > $V_{VAC_PRESENT}$, the SGM41574 sets EN_ACDRV1 bit to 1 and then ACDRV1 pin changes to high, the ACFET1-RBFET1 turns on.

4. To switch the VAC1 input source to the VBUS input source, the host should first turn off the ACFET1-RBFET1 to avoid the two input sources shorting together. In this configuration, writing EN_ACDRV1 = 0 directly will be ignored by SGM41574. The host can set ACDRV_DIS = 1 first to force EN_ACDRV1 = 0, after the ACFET1-RBFET1 turns off, then enable the input source from VBUS.

5. To switch the VBUS input source to the VAC1 input source, the host should first remove the VBUS input source, and then set ACDRV_DIS = 0 to enable ACDRV1 and the ACFET1-RBFET1 turns on.

DETAILED DESCRIPTION (continued)

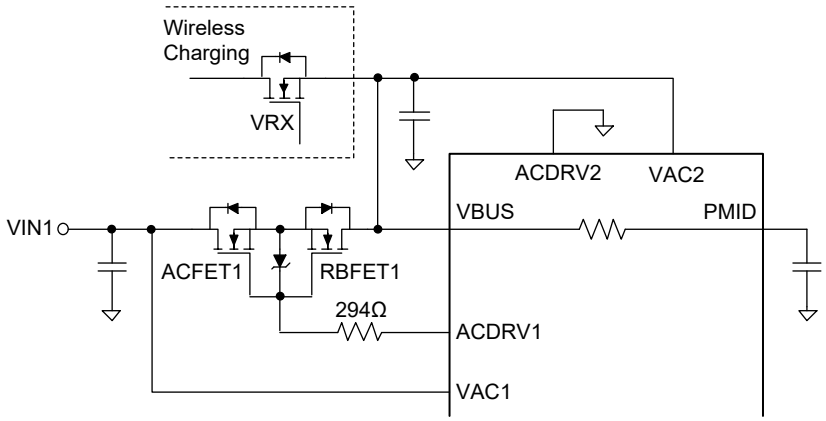


Figure 5. One Input at VAC1 and/or One Input at VBUS with ACFET1-RBFET1

Dual Input with ACFET1-RBFET1 and ACFET2-RBFET2

In this configuration, both ACFET1-RBFET1 and ACFET2-RBFET2 are populated and the SGM41574 supports the dual input source from VAC1 and VAC2. VAC1 and VAC2 are tied to the drain of ACFET1 and ACFET2, respectively. ACDRV1 and ACDRV2 are connected to the gate of ACFET1 and ACFET2, respectively.

1. During POR, the SGM41574 detects that ACFET1-RBFET1 and ACFET2-RBFET2 are both populated, and updates ACRB1_STAT and ACRB2_STAT to 1.

2. After V_{VACa} > $V_{VAC_PRESENT}$ (suffix "a" means 1 or 2, depending on which comes first, "b" means the other input source), the SGM41574 sets EN_ACDRVa to 1 and then ACDRVa pin changes to high, the ACFETa-RBFETa turns on. Regardless of the other input source valid or not later, the EN_ACDRVb keeps 0, the ACDRVb pin remains low and the ACFETb-RBFETb keeps off.

3. In this configuration, the host can program EN_ACDRV1 and EN_ACDRV2 with below limitations.

a. Avoid turning on both ACFETx-RBFETx to short the two input source together, the SGM41574 will ignore the REG0x13[7:6] = 11 command (set both EN_ACDRVx bits to 1) from the host.

b. With only one valid input source connected at either VAC1 or VAC2 case, the SGM41574 always tries to connect the only one input source to power the charger, then the host cannot turn off the both ACFETx-RBFETx by setting REG0x13[7:6] = 00. In this case, setting ACDRV_DIS to 1 can force to turn off the both ACFETx-RBFETx. With two valid input sources at VAC1 and VAC2 case, both ACFETx-RBFETx can be turned off by setting REG0x13[7:6] = 00 or ACDRV_DIS = 1.

Supposing both VAC1 and VAC2 are valid and the ACFET1-RBFET1 turns on, the host can switch the input source from VAC1 to VAC2 by setting REG0x13[7:6] (EN_ACDRV2, EN_ACDRV1) from 01 to 10. If there is a fault on VAC1 such as VAC_OVP, the SGM41574 automatically switches the input source to VAC2 by setting REG0x13[7:6] internally from 01 to 10. The switchover from VAC2 to VAC1 shares the same control logic.

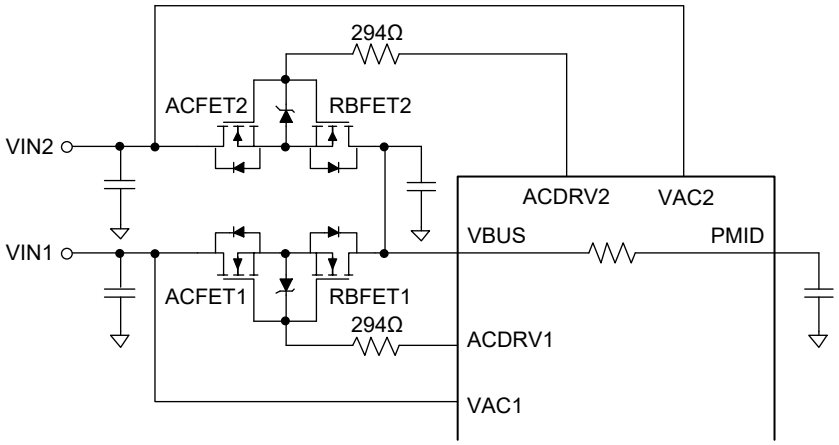


Figure 6. Dual Input with ACFET1-RBFET1 and ACFET2-RBFET2

DETAILED DESCRIPTION (continued)

Figure 7 shows the input changes from VAC1 to VAC2 when VAC1 is removed. At the beginning, both VAC1 = 5V and VAC2 = 9V are valid. When VAC1 is invalid, the SGM41574 completes the input source auto switchover from VAC1 to VAC2 without the host control.

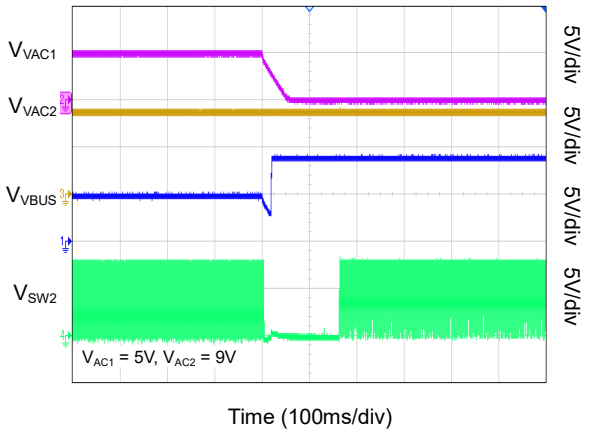


Figure 7. Input Source Auto Switchover from VAC1 to VAC2 when VAC1 is Removed

If the battery voltage is too low, the system voltage drops during the switchover, because there is a short time period stop switching after ACFET1-RBFET1 turns off and before ACFET2-RBFET2 turns on. The user should be aware of this behavior and make sure to switch the input source under appropriate battery voltage condition.

After the input source is switched to VAC2, the SGM41574 keeps ACFET2-RBFET2 on and ACFET1-RBFET1 off even if the VAC1 is valid again. In this case, the switchover happens when the VAC2 input source becomes invalid or the host sets REG0x13[7:6] from 10 to 01.

In this dual input with ACFET1-RBFET1 and ACFET2-RBFET2 configuration, the EN_ACDRVx bits are related to the ACDRVx pin voltage and the ACFETx-RBFETx on/off. The host can write EN_ACDRVx to 1 or 0 to turn on/off the ACFETx-RBFETx, or read the EN_ACDRVx value to indicate the ACFETx-RBFETx on/off status.

The ACFETx-RBFETx not only can be turned off by setting EN_ACDRVx = 0 or ACDRV_DIS = 1, but the SGM41574 internal logic also turns them off in the related fault protection (e.g. IBUS_OCP or VAC_OVP).

REGN LDO Power-Up

When the device is powered up from the input source and $V_{VBUS_PRESENT}$ < V_{VBUS} < V_{VBUS_OVP}, the REGN LDO is turned on to supply the internal bias circuits and the MOSFETs gate drivers. When the device is powered from a battery only state, the REGN LDO is turned on under each of the below conditions:

1. The charger is operated in the OTG mode.
2. V_{BAT} > V_{BAT_UVLOZ}, and TS ADC channel is on (EN_ADC = 1 and TS_ADC_DIS = 0).

The TS, STAT and ILIM_HIZ pull-up powers can be connected to REGN. The nINT pin is recommended to be pulled up to external logic high rail because the REGN may stay off in battery only condition.

The REGN is critical for the charge normal operation. Do not connect other external circuits on REGN.

Poor Power Source Detection (Qualification)

When REGN LDO is powered, the input source is checked for its current capacity. To pass the poor source qualification, the input (VBUS) must meet the following conditions:

1. V_{VBUS} < V_{VBUS_OVP}.
2. V_{VBUS} > V_{BAD_SRC} + $V_{BAD_SRC_HYS}$ (250mV TYP) during 30ms test period in which the I_{BAD_SRC} (35mA TYP) current is pulled from VBUS.

Once the VBUS over-voltage protection is detected, the SGM41574 will automatically retry the detection when the over-voltage fault condition disappears. If above condition 2 is detected (bad source adaptor), the SGM41574 retries the detection and enters HIZ mode (EN_HIZ bit is set to 1) after 7 consecutive failures. In HIZ mode, the system is supplied by the battery only. Resume the converter operation requires re-plugging the adaptor and/or toggling the EN_HIZ bit. When the adaptor is plugged in, the EN_HIZ bit is automatically reset to 0.

After the input source passes the poor source qualification, the PG_STAT bit is set to 1. The PG_FLAG will be set to 1 and the nINT pin also generates a 256μs negative pulse to notify the host if PG_MASK = 0.

When the SGM41574 enters HIZ mode after 7 consecutive failures, the POORSRC_STAT bit is set to 1 and POORSRC_FLAG = 1, the nINT pin is pulsed to notify the host if POORSRC_MASK = 0.

DETAILED DESCRIPTION (continued)

Default VINDPM Setting

After a good input source is detected, the SGM41574 starts the ADC reading including the VBUS pin voltage. At that time, the converter has not started switching and there is no load on VBUS. With the VBUS_ADC measurement result VBUS0, the SGM41574 updates the POR default threshold of VINDPM[7:0] register to be VBUS0 - 0.7V (VBUS0 < 7V) or VBUS0 - 1.4V (7V ≤ VBUS0 ≤ 22V). The VINDPM[7:0] register default value is clamped to 22V when VBUS0 ≥ 22V (TYP).

Please note that due to the offset of the internal sampling circuit, there may be some deviation for the 22V initial voltage detection. For example, the default value of the VINDPM[7:0] register may be clamped to 22V when VBUS0 is about 21.6V. In this case, it is recommended to change the VINDPM[7:0] register by host.

During the converter normal switching, the host can re-write the VINDPM[7:0] register to any other value within the register range. If V_{BAT} > V_{SYSMIN}, the host also can execute the VBUS0 (VBUS at no load condition) measurement by setting FORCE_VINDPM_DET bit to 1. After FORCE_VINDPM_DET bit is set to 1, the SGM41574 stops switching for VBUS0 measurement, and then updates the VINDPM[7:0] register. The FORCE_VINDPM_DET bit is automatically reset to 0 and the converter resume switching after the VINDPM[7:0] register is reset. To avoid the system voltage dropping below V_{SYSMIN} during the VBUS0 measurement, the FORCE_VINDPM_DET = 1 command is ignored by SGM41574 if V_{BAT} < V_{SYSMIN}.

If the calculated VINDPM from VBUS0 is out of VINDPM[7:0] register range, the SGM41574 clamps the VINDPM to a minimum of 3.6V or a maximum of 22V.

ILIM_HIZ Pin

After a good input source is detected, the SGM41574 starts the ADC reading including the ILIM_HIZ pin voltage. When EN_EXTILIM bit is set to 1, the ILIM_HIZ pin voltage sets the IINDPM[8:0] register to the high clamp value ILIM. The ILIM is calculated as I_{LIM} = (V_{ILIM_HIZ} - 1V)/800mΩ. If the input current limit from the input source type detection is higher than that ILIM, the IINDPM[8:0] register will be clamped at ILIM. After POR, if the host writes the new IINDPM value higher than the ILIM, the SGM41574 ignores this invalid write command and keeps the IINDPM[8:0] register unchanged.

It is recommended to use a resistor voltage divider from REGN or an external power source to provide the required ILIM_HIZ voltage. When V_{ILIM_HIZ} < 1.08V, the ILIM is clamp to 100mA minimum value. The converter stops switching and REGN keeps on at either charging mode or OTG mode if V_{ILIM_HIZ} < 0.7V. When V_{ILIM_HIZ} > 1.1V, the switching resumes.

Input Source Type Detection

The input power source detection will run through the D+/D- lines after the adaptor passes the poor source qualification when the EN_AUTO_INDET bit is set to 1. The SGM41574 follows the USB Battery Charging Specification 1.2 (BC1.2) to detect input adaptor power source type via D+/D- lines. All the types of SDP, CDP, DCP and non-standard adaptor can be automatically detected and indicated. If the DCP adaptor is detected, the SGM41574 optional provides further high voltage adaptor handshake on D+/D- lines by enabling the HVDCP detection.

The following registers are changed after the input source type detection:

1. Input current limit register (IINDPM[8:0]) is changed to set the right current limit. The IINDPM also be clamped by V_{ILIM_HIZ} setting if EN_EXTILIM = 1.
2. Change VBUS_STAT[3:0] according to the input source type detection result.

The SGM41574 input current is always limited by IINDPM[8:0] registers and can be changed to other value by host after the detection is completed. If host write the new IINDPM value is higher than 3.3A (the maximum IINDPM[8:0] register range) or higher than the clamp value by V_{ILIM_HIZ} if EN_EXTILIM = 1, the SGM41574 ignores this invalid write command and keeps the IINDPM[8:0] register unchanged.

The input source type detection can be bypassed by setting EN_AUTO_INDET = 0. In this case, the IINDPM[8:0] register remains unchanged and the VBUS_STAT[3:0] is not qualified adaptor.

Input Current Limit by D+/D- Detection

The input current limit of the SGM41574 is determined and set by the integrated D+/D- based input power source detection. Five major steps are included in the D+/D- detection: VBUS Detection, Data Contact Detect (DCD, detect Non-Standard adaptor), Primary Detection (detect SDP adaptor), Secondary Detection (detect CDP adaptor and DCP adaptor), and High Voltage detection (detect HVDCP adaptor). Please refer to Figure 8.

DETAILED DESCRIPTION (continued)

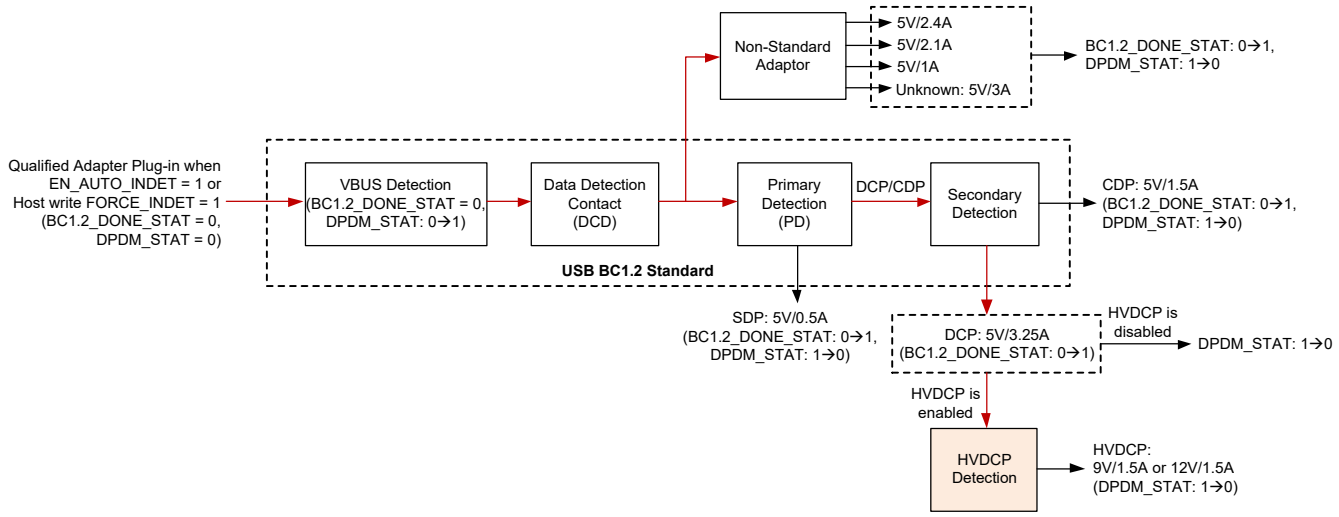


Figure 8. D+/D- Detection Flow including Corresponding Status

Table 3. Non-Standard Adaptor Type Detection

Non-Standard Adaptor	D+ Threshold	D- Threshold	Input Current Limit (A)
Divider 1	V_{D+} within V_{2P8_VTH}	V_{D-} within V_{2P0_VTH}	2.1
Divider 2	V_{D+} within V_{2P0_VTH}	V_{D-} within V_{2P8_VTH}	1
Divider 3	V_{D+} within V_{2P8_VTH}	V_{D-} within V_{2P8_VTH}	2.4
Unknown	V_{D+} = 1MΩ to 0V	V_{D-} = 3.3V	3.0

If HVDCP detection is enabled (EN_HVDCP = 1 and either EN_9V = 1 or EN_12V = 1), the SGM41574 continues to proceed the HVDCP handshakes to adjust the adaptor output voltage to 9V or 12V for fast charging.

As shown in Figure 8, after the input power source type detection is completed, the DPDM_STAT bit is updated to 0 and the DPDM_DONE_FLAG bit is set to 1. The nINT pin sends out a negative pulse to notify the host if DPDM_DONE_MASK = 0. Besides, the VBUS_STAT[3:0] and IINDPM[8:0] registers are updated as shown in Table 4.

Some notes for HVDCP detection:

1. The EN_12V = 1 has higher priority when EN_12V bit and EN_9V bit are both set to 1 before the detection.
2. If a non-QC adaptor is plugged in and the HVDCP related bits are enabled, the HVDCP detection will fail, and the VBUS_STAT[3:0] keeps 0011 to indicate the USB DCP adaptor.
3. If a QC adaptor is plugged in and the HVDCP related bits are disabled, there is no HVDCP detection and the VBUS_STAT[3:0] also keeps 0011 to indicate the USB DCP adaptor.

Table 4. Input Current Limit Setting from D+/D- Detection

D+/D- Detection	VBUS_STAT[3:0]	Input Current Limit
USB SDP	0001	500mA
USB CDP	0010	1.5A
USB DCP	0011	3.25A
Adjustable High Voltage DCP (HVDCP)	0100	1.5A
Unknown Adaptor	0101	3A
Non-Standard Adaptor, Divider 1	0110	2.1A
Non-Standard Adaptor, Divider 2	0110	1A
Non-Standard Adaptor, Divider 3	0110	2.4A

DETAILED DESCRIPTION (continued)

Force Input Current Limit Detection

In host mode, the host can set FORCE_INDET bit to 1 to force the charger to run the input current limit detection. FORCE_INDET bit is automatically reset to 0 once the detection is done. Due to the force detection result, the VBUS_STAT[3:0] register and IINDPM[8:0] register may be changed. The VINDPM[7:0] register keeps unchanged when the FORCE_INDET bit is set to 1.

D+/D- Status

The host can set different status on D+ or D- pins of the SGM41574 via DPLUS_DAC[2:0] and DMINUS_DAC[2:0] registers. The D+ pin status can be set to HIZ, 0V, 0.6V, 1.2V, 2.0V, 2.7V, 3.3V or "short to D-", and the D- pin status can be set to HIZ, 0V, 0.6V, 1.2V, 2.0V, 2.7V or 3.3V. The D+/D- pins are only applied at the VAC1 input source. If D+/D- status change is required for more QC adaptor detection, the host should set the DPLUS_DAC[2:0] and DMINUS_DAC[2:0] registers after input source D+/D- detection is done (DPDM_STAT = 0). The D+/D- status change command during D+/D- detection period will be ignored by SGM41574.

Connector Fault Detection

The host can read the SGM41574 D+ and D- pin voltages via DP_ADC[15:0] and DM_ADC[15:0] registers. This ADC value can help the host detect the connection faults.

Input Current Optimizer (ICO)

The SGM41574 provides input current optimizer (ICO) to identify the input adaptor source maximum power point. To avoid the input adaptor source overload and stay in VINDPM, the ICO algorithm automatically identifies the maximum input current limit of the adaptor and updates this input current limit to ICO_ILIM[8:0] register.

The ICO function is default disabled, and it can be enabled by setting EN_ICO bit to 1. After a DCP type input source is detected, the ICO algorithm runs automatically when EN_ICO = 1. For DCP or any other input source adaptors, the host also can set FORCE_ICO bit to 1 to force the ICO algorithm under EN_ICO = 1 condition.

The actual input current limit is reported by ICO_ILIM[8:0] register in ICO mode, while it is decided by the IINDPM[8:0] register when out of ICO mode.

When the ICO algorithm is activated, it runs to dynamically and continuously adjust the input current limit using ICO_ILIM[8:0] register until the ICO_STAT[1:0] and ICO_FLAG bits are finally set. The operation of ICO algorithm depends on the battery voltage as following:

1. When V_{BAT} < V_{SYS_MIN}, the device starts ICO algorithm by ICO_ILIM[8:0] register with an initial value that equals the IINDPM. Where the IINDPM is the maximum input current limit that determined by the system.
2. When V_{BAT} > V_{SYS_MIN}, the device starts ICO algorithm by ICO_ILIM[8:0] register with an initial value of 500mA. The 500mA is minimum input current limit which minimizes the input power source overload.

During the optimization, if VINDPM is triggered, the algorithm decreases the input current limit (the dynamic ICO_ILIM[8:0] register) to avoid input source overloading. When the maximum input current limit is detected, the ICO_ILIM[8:0] register reflects the optimal maximum input current limit which is not trigger VINDPM. The ICO_FLAG bit is set and the ICO_STAT[1:0] bits are updated to 10 to indicate the maximum input current detected.

In above case 1, if both VINDPM and IINDPM are not triggered at ICO_ILIM[8:0] initial value, the ICO_ILIM[8:0] registers keeps the initial value and the ICO_STAT[1:0] = 01 to indicate the ICO optimization is in process. If the load becomes heavier, the VINDPM still not triggered but IINDPM is triggered, the algorithm is also completed, the ICO_ILIM[8:0] register keeps the initial value still, the ICO_FLAG bit is set and ICO_STAT[1:0] bits are updated to 10 to indicate the maximum input current detected.

In above case 2, if the VINDPM is not triggered and the converter is under light load condition, the ICO_ILIM[8:0] register gives the input current limit a little higher than the actual input current. The ICO_STAT[1:0] bits remains 01 to indicate the ICO optimization is in process. If the load becomes heavier, the algorithm automatically runs to set new ICO_ILIM[8:0] register value.

Once the algorithm is completed (ICO_STAT[1:0] = 10), the ICO_ILIM[8:0] register will keep unchanged unless one of the following events occurs. Each of the follow events can force the ICO algorithm to run again and reset the ICO_STAT[1:0] bits to 01:

1. Re-plugin the input source.
2. Host changes the IINDPM[8:0] register.
3. Host changes the VINDPM[7:0] register.
4. Host sets the FORCE_ICO bit to 1.
5. Resume from VBUS_OVP.

DETAILED DESCRIPTION (continued)

Buck-Boost Converter Operation

The SGM41574 provides 3.6V to 24V wide operation input voltage range, which can support legacy 5V USB adaptor, HVDCP and USB-PD adaptor application. To support 1-4 cells Li-Ion battery charging, the SGM41574 automatically works at Buck, Boost or Buck-Boost configurations according to the adaptor voltage and battery voltage.

Pulse Frequency Modulation (PFM)

At light load, if charging is disabled or the battery voltage is lower than V_{SYS_MIN}, the SGM41574 changes from PWM mode to PFM mode, this is helpful to improve the efficiency. The host can disable the PFM operation via writing PFM_FWD_DIS bit = 1. If the PFM mode is selected, the out-of-audio (OOA) feature can be chosen under FWD_OOA_DIS = 0 condition. In OOA operation mode, the converter switching frequency is larger than 20kHz even at extremely light load to prevent the audible range operation.

Device HIZ State

Host setting the EN_HIZ bit to 1 can enable the HIZ mode of the SGM41574. In this mode, the converter stops switching and REGN LDO is off. The power loss is extremely low at HIZ state. If the battery is present, only BATFET turns on to support system.

Table 5 summarizes the converter switching, REGN status and EN_HIZ bit status in some condition of the SGM41574 operation.

Table 5. Status Summarizes

Conditions	Converter Switching	REGN LDO	EN_HIZ Bit
Host Sets EN_HIZ = 1	Stop	Off	1
Fail Poor Source Qualification (after 7 Consecutive Failures)	Stop	Off	1
IBUS_OCP	Stop	Off	1
VSYS_SHORT (after 7 Consecutive Failures)	Stop	Off	1
V_{ILIM_HIZ} < 0.7V	Stop	On	0
VBUS_OVP			
VSYS_OVP			
VBAT_OVP			
OTG_OVP			
TS Fault in OTG Mode			

USB On-The-Go (OTG) Mode

The SGM41574 supports USB On-The-Go. When a load device is connected to the USB port, the converter can deliver power from battery to USB port. The USB OTG output voltage is programmable from 2.8V to 22V with 10mV step size via VOTG[10:0] register. The OTG output current limit is programmable from 120mA to 3.32A with 40mA step size via IOTG[6:0] register. To enable the OTG mode, the following conditions should be satisfied first:

1. $V_{BAT} > V_{BAT_OTG}$.
2. $V_{VBUS} < V_{VBUS_PRESENT}$ and $V_{VAC} < V_{VAC_PRESENT}$.
3. TS pin voltage is out of BHOT and BCOLD range.

The output voltage is set to the programmed value by VOTG[10:0] register and is maintained as long as V_{BAT} is above V_{BAT_OTG}. The output current can reach up to the programmed value by IOTG[6:0] register. The VBUS_STAT[3:0] status register is set to 0111 in OTG mode.

The OTG behavior is shown in Table 6 according to the different input ACFETx-RBFETx presence.

If the OTG output is already on VAC1, the EN_ACDRV1 = 1 and EN_ACDRV2 = 0. To switch the OTG output to VAC2, the host should first write EN_ACDRV1 = 0 to turn off the ACFET1-RBFET1, and then write EN_ACDRV2 = 1 to turn on the ACFET2-RBFET2. The OTG output switchover from VAC2 to VAC1 shares the same control logic.

In OTG mode, the SGM41574 works in PFM mode by default at light load to improve the efficiency. The host can disable the OTG PFM operation via writing PFM_OTG_DIS = 1. If the PFM mode is selected, the out-of-audio (OOA) feature can be chosen under OTG_OOA_DIS = 0 condition. In OOA operation mode, the converter switching frequency is larger than 20kHz even at extremely light load to prevent the audible range operation.

DETAILED DESCRIPTION (continued)

Table 6. OTG Behavior for Different Input ACFETx-RBFETx Presence

ACDRV_DIS (REG0x12[7])	ACRB1_STAT (REG0x1E[6])	ACRB2_STAT (REG0x1E[7])	OTG Enable Condition and Behavior
1	x	x	10ms after setting EN_OTG = 1, VBUS starts to rise up.
0	0	0	10ms after setting EN_OTG = 1, VBUS starts to rise up.
0	1	0	Set EN_OTG = 1, no switching. Then set EN_ACDRV1 = 1, VAC1 starts to rise up.
0	0	1	Set EN_OTG = 1, no switching. Then set EN_ACDRV2 = 1, VAC2 starts to rise up.
0	1	1	Set EN_OTG = 1, no switching. Then set EN_ACDRV1 = 1 to output to VAC1 or EN_ACDRV2 = 1 to output to VAC2.

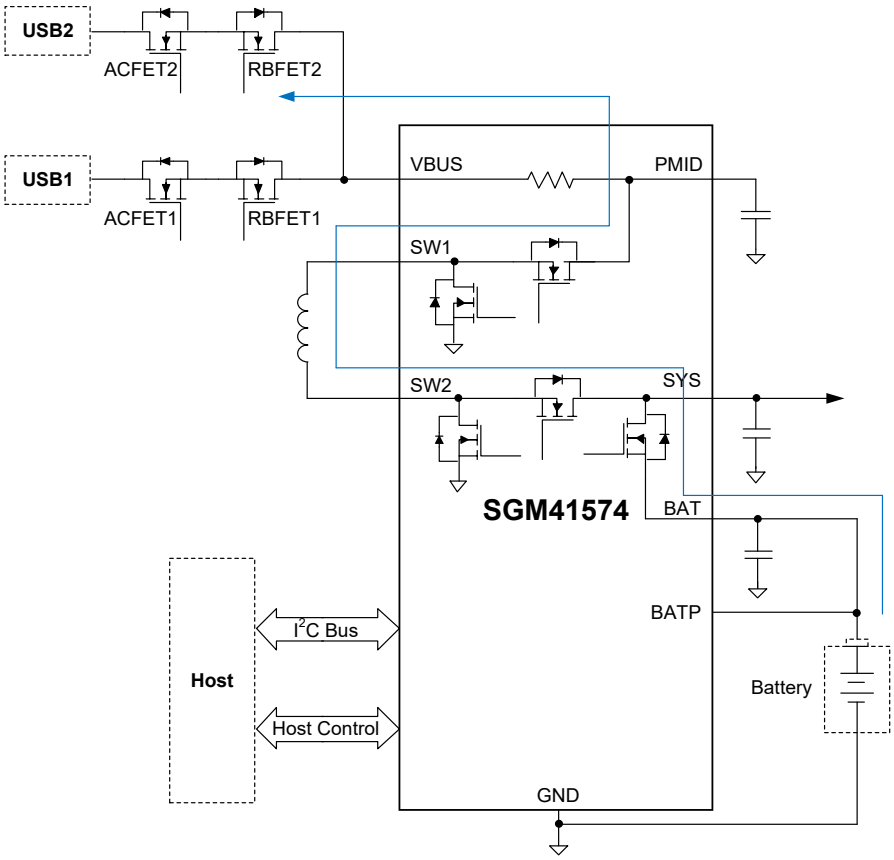


Figure 9. OTG Mode Application Diagram

In OTG mode, the SGM41574 delivers the power from battery to external USB port, the power flow is shown in Figure 9.

In OTG mode, the SGM41574 monitors and regulates the battery discharge current. Due to the higher priority in system load, once the discharge current is higher than IBAT_REG[1:0] setting threshold, the SGM41574 reduces the OTG output current. The IBAT_REG_STAT and IBAT_REG_FLAG bits are both set to 1. There is an nINT pulse to notify the host if IBAT_REG_MASK = 0. If the OTG output current is reduced to 0 but the system current is still larger than IBAT_REG[1:0] setting, the SGM41574 will not limit the discharge current. If the ship FET is present and EN_BATOC = 1, the large discharge current may trigger the IBAT OCP.

DETAILED DESCRIPTION (continued)

Battery Charging Management

The SGM41574 is designed for charging 1-4 cells Li-Ion or Li-poly batteries with a charge current up to 5A (MAX). The battery connection switch (BATFET) is in the charge or discharge current path and features low on-resistance to allow high efficiency and low voltage drop.

Charging Cycle in Autonomous Mode

Charging is enabled if EN_CHG = 1 and nCE pin is pulled low. In default mode, the SGM41574 runs a charge cycle with the default parameters itemized in Table 7. At any moment, the SGM41574 can be controlled by changing to the host mode.

Table 7. Charging Parameter Default Settings

Default Mode	SGM41574
Charging Voltage	4.2V (1-cell), 8.4V (2-cell), 12.6V (3-cell), 16.8V (4-cell)
Recharging Voltage Threshold	200mV
Trickle Charge Current	80mA
Trickle Charge Safety Timer	1h
Pre-Charge Current	120mA
Pre-Charge Safety Timer	2h
Fast Charge Current	2A (1-cell and 2-cell), 1A (3-cell and 4-cell)
Fast Charge Safety Timer	12h
Termination Current	200mA
Temperature Profile	JEITA

Start a New Charging Cycle

If the converter can start switching and all the following conditions are satisfied, a new charge cycle starts:

• NTC temperature fault is not asserted (TS pin).
• Safety timer fault is not asserted.
• Charging enabled (2 conditions: EN_CHG bit = 1, nCE pin is low).
• Battery voltage is below the programmed full charge level (V_{REG}).

Normally a charge cycle terminates when the SGM41574 is operated in the battery constant voltage regulation loop and the charging current falls below the termination threshold if the device is not in thermal regulation or dynamic power management (DPM) mode. If the charge cycle is finished, a new charging cycle can be initiated by toggling of the nCE pin or EN_CHG bit.

A new charge cycle starts automatically if battery voltage falls below the recharge threshold level (configured by VRECHG[3:0] bits).

After charge termination, the SGM41574 turns off the BATFET and the adaptor supplies the power to system load. The system voltage is regulated to 150mV (TYP) above the battery voltage. This charge termination feature is important to extend the battery life by avoiding charge and discharge battery frequently when V_{BAT} is closed to the setting charge voltage.

Charge Status Report

The charge status bits (CHG_STAT[2:0]) indicate the SGM41574's charging phases as below:

• 000 = Not Charging
• 001 = Trickle Charge
• 010 = Pre-Charge
• 011 = Fast Charge CC Mode
• 100 = Taper Charge CV Mode
• 101 = Reserved
• 110 = Top-Off Timer Active
• 111 = Charge Termination

When the device changes to any of the above statuses, or the charge cycle is completed, the nINT pin is pulsed to notify the host.

DETAILED DESCRIPTION (continued)

Battery Charging Profile

The SGM41574 features a full battery charging profile with five phases. When a charging cycle starts, the battery voltage (V_{BAT}) is tested, and appropriate current and voltage regulation levels are selected as shown in Table 8. Depending on the detected status of the battery, the proper phase is selected to start or for continuation of the charging cycle. The five phases are: trickle charge (battery voltage too low), pre-charge, constant current, constant voltage and an optional top-off trickle charging phase.

Note that in the DPM or thermal regulation modes, normal charging functions are temporarily modified:

1. The charge current is less than the value in the register.
2. Termination is disabled.
3. The charging safety timer is slowed down by counting at half clock rate.

The V_{BAT_LOWV} indicates the battery voltage threshold for the transition from pre-charge to fast charge, which is defined as a ratio of battery voltage regulation limit (V_{REG}). The V_{BAT_SHORTZ} indicates the battery voltage threshold for the transition from trickle charge to pre-charge, which is fixed value 2.3V. For the configuration that $V_{BAT_LOWV} < V_{BAT_SHORTZ}$, there is no pre-charge phase.

The SGM41574 provides the LDO_DIS bit to disable the BATFET LDO operation. After LDO_DIS is set to 1, the system voltage is not regulated at V_{SYSMIN} + 200mV at $V_{BAT_SHORT} < V_{BAT} < V_{SYSMIN}$ condition. Meanwhile, the pre-charge current and fast charge current are consistent with the corresponding register setting, and regulated by the converter PWM current regulation loop. When $V_{BAT} < V_{BAT_SHORT}$, the system voltage is still regulated to V_{SYSMIN} + 200mV even if the LDO_DIS is set to 1, and the trickle charge current keeps the register setting value.

Table 8. Charging Current Setting Based on V_{BAT}

V_{BAT} Voltage	Selected Charging Current	Default Value in the Register	CHG_STAT[2:0]
$V_{BAT} < V_{BAT_SHORT}$	I_{SHORT}	80mA	001
$V_{BAT_SHORT} < V_{BAT} < V_{BAT_LOW}$	I_{PRECHG}	120mA	010
$V_{BAT} > V_{BAT_LOW}$	I_{CHG}	2A (1-cell and 2-cell) 1A (3-cell and 4-cell)	011

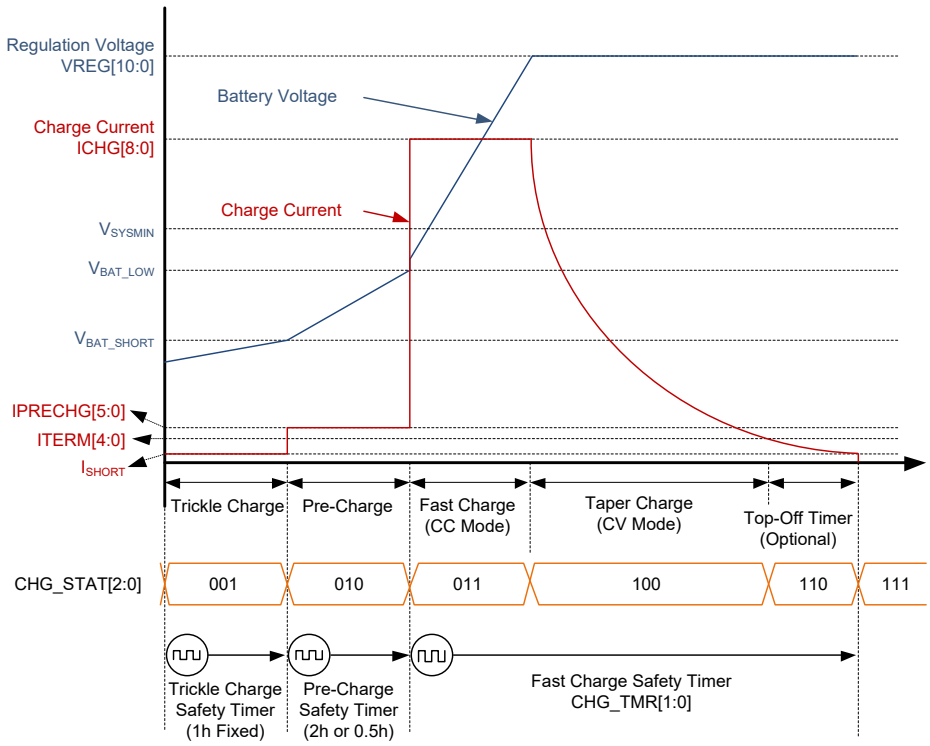


Figure 10. Battery Charging Profile

DETAILED DESCRIPTION (continued)

Charge Termination

Normally, a charge cycle terminates when the SGM41574 is operated in the battery constant voltage regulation loop and the charging current falls below the termination threshold, if the device is not in thermal regulation or dynamic power management (DPM) mode. Unless there is a high power demand for system and need to operate in supplement mode, the BATFET turns off at the end of the charge cycle. Even after termination, the Buck-Boost converter operates continuously to supply the system. The system voltage is regulated to 150mV (TYP) above the battery voltage.

The CHG_STAT[2:0] register is set to 111 and a negative pulse is sent to nINT pin after termination.

If the charger is regulating the input current or input voltage or junction temperature instead of the charge current, the termination will be temporarily prevented. The EN_TERM bit is a termination control bit and can be set to 0 to permanently disable termination before it happens.

Due to the offset of the internal current comparator, the termination charge current may be much higher (40% TYP) than the set value when it is set too low (e.g. below 160mA). A delay in termination can be added (optional) as a compensation for comparator offset using a programmable top-off timer. During the delay, the constant-voltage charge phase continues and gives the falling charge current a chance to drop closer to the programmed value. The setting of the top-off timer is applied at the time of termination detection, and unless a new charge cycle is started, modifying the top-off timer parameters after termination has no effect. A negative pulse is sent to nINT when top-off timer is started or ended. If set CHG_MASK bit to 1, the CHG_STAT[2:0] bit change will not produce nINT pulse.

The top-off delay timer has the same restrictions of the safety timer. In other words, under some conditions, if the safety timer is suspended, the top-off timer will also be suspended or if the safety timer is slowed down, the top-off timer will also be slowed down. Code 110 at CHG_STAT[2:0] indicates the in top-off timer is valid. The CHG_STAT[2:0] bits change to 111 after the top-off timer expires. And the nINT pin reports a negative pulse to notify the host.

Any of the following events resets the top-off timer:

1. Disable to enable transition of nCE (charge enable).
2. A low to high change in the status of termination.
3. Set REG_RST bit to 1.

Charging Safety Timer

Abnormal battery conditions may result in prolonged charge cycles. An internal safety timer is considered to stop charging in such conditions. If the charging safety timer timeout occurs, the corresponding *_TMR_STAT bit is set and a negative pulse is sent to nINT pin.

The trickle charge, pre-charge and fast charge safety timers can be enabled or disabled by configuring the EN_TRICHG_TMR, EN_PRECHG_TMR or EN_CHG_TMR bit. When each charge phase starts, the timer starts to count if the corresponding enable bit is set to 1. If the host enables the safety timer during the charge phase, the timer will restart to count.

The safety timer counts at half clock rate when charger is under input voltage regulation, input current regulation or thermal regulation, and the actual charge current is always reduced. As an example, if the charging safety timer is set to 2 hours and the charger is under input current regulation (IINDPM_STAT = 1) in the whole charge cycle, the actual safety time will be 4 hours. Clearing the EN_TMR2X bit will disable the half clock rate feature. Changing the EN_TMR2X bit while the device is charging has no effect on the safety timer count. It is recommended to set the EN_TMR2X bit before starting the charging cycle (changing the EN_CHG bit, toggling the nCE pin, when a charged battery falls below recharge threshold or the adaptor power-on).

The safety timer is paused if a fault occurs which disables the charging. The EN_TMR2X bit also has no effect in this condition because the timer counting is stopped. It will resume once the fault condition is removed. If the charging cycle is stopped and restarted by toggling nCE pin or EN_CHG bit, the timer resets and restarts a new timing.

The fast charge safety timer can be reset by the following events:

1. Stop and restart the charging cycle (change EN_CHG bit, toggle nCE pin, or the charged battery falls below recharge threshold).
2. Charge status changes between pre-charge and fast charge (in default mode or host mode).
3. Host changes the CHG_TMR[1:0] register setting.
4. Host disables and then enables the EN_CHG_TMR bit during the fast charge phase.

DETAILED DESCRIPTION (continued)

The pre-charge safety timer can be reset by the following events:

1. Stop and restart the charging cycle (change EN_CHG bit or toggle nCE pin).
2. Charge status changes between pre-charge and fast charge or between trickle charge and pre-charge (in default mode or host mode).
3. Host changes the PRECHG_TMR register setting.
4. Host disables and then enables the EN_PRECHG_TMR bit during the pre-charge phase.

The trickle charge safety timer can be reset by the following events:

1. Stop and restart the charging cycle (change EN_CHG bit or toggle nCE pin).
2. Charge status changes between trickle charge and pre-charge (in default mode or host mode).
3. Host disables and then enables the EN_TRICHG_TMR bit during the trickle charge phase.

Narrow VDC (NVDC) Design in SGM41574

The SGM41574 provides 3.6V to 24V wide operation input voltage range, which can support legacy 5V USB adaptor, HVDCP and USB-PD adaptor application. The power path management automatically optimizes the power supply source to system at different system load condition.

The SGM41574 features an NVDC design using the BATFET that connects the system to the battery. By using the linear region of the BATFET, the charger regulates the system bus voltage (SYS pin) above the minimum setting using Buck-Boost converter even if the battery voltage is very low. MOSFET linear mode allows for the large voltage difference between SYS and BAT pins to appear as V_{DS} across the switch while conducting and charging battery. VSYSMIN[5:0] register sets the minimum system voltage. If the system is in minimum system voltage regulation, VSYS_STAT bit is set.

The BATFET operates in linear region when the battery voltage is lower than the minimum system voltage. The system voltage is regulated at 200mV (TYP) above the minimum system voltage setting. As the battery gradually gets charged, until its voltage get rising higher than the minimum system voltage, the BATFET changes from linear mode to fully turned-on mode, and the system voltage keeps V_{DS} of BATFET higher than the battery voltage.

The system voltage is always regulated to 150mV (TYP) above the battery voltage if:

1. The charging is terminated.
2. $V_{BAT} > V_{SYSMIN}$, and the charging is disabled.

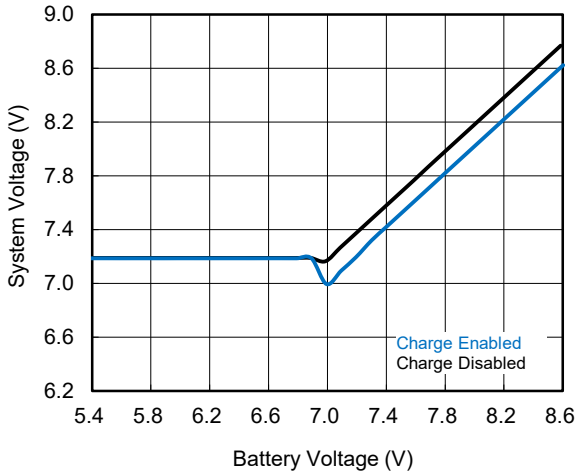


Figure 11. System Voltage vs. Battery Voltage for a 2-Cell Battery Configuration

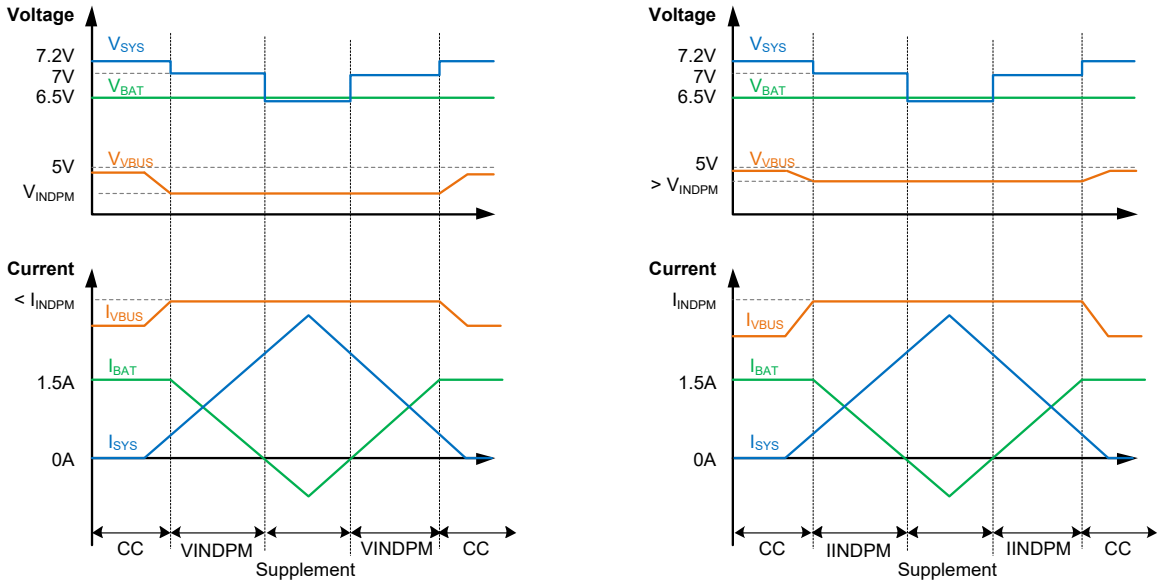
Dynamic Power Management (DPM)

The SGM41574 features a dynamic power management (DPM). To implement DPM, the device always monitors the input current and voltage to regulate power demand from the source and avoid input adaptor overloading or to meet the maximum current limits specified in the USB specifications. Overloading an input power source may result in either the voltage tending to fall below the input voltage limit (V_{INDPM}) or the current trying to exceed the input current limit (I_{INDPM} or ICO_ILIM[8:0]). With DPM, the device keeps the VSYS regulated to its minimum setting by reducing the battery charge current adequately such that the input parameter (voltage or current) does not exceed the limit. In other words, charge current is reduced to satisfy $I_{IN} \le I_{INDPM}$ or $V_{IN} \ge V_{INDPM}$ whichever occurs first. DPM can be either an I_{IN} type (IINDPM) or V_{IN} type (VINDPM), depending on which limit is reached.

Changing to the supplement mode may be required if the charge current is decreased and reached to zero while the input is still overloaded. In this case, the charger reduces the system voltage below the battery voltage to allow operation in the supplement mode and provide a portion of system power demand from the battery through the BATFET.

The IINDPM_STAT or VINDPM_STAT status bits are set during an IINDPM or VINDPM respectively. Figure 12 summarizes the DPM behavior for a design example with a 5V/3A adaptor, 6.5V battery, 1.5A charge current setting and 7V minimum system voltage setting.

DETAILED DESCRIPTION (continued)



a) Input, Battery and System Voltage and Currents in VINDPM

b) Input, Battery and System Voltage and Currents in IINDPM

Figure 12. Input, Battery and System Voltage and Currents in DPM

Battery Supplement Mode

When the system is under heavy load, the system voltage may drop below the battery voltage, the BATFET gradually starts to turn on. At low discharge currents, the BATFET gate voltage is regulated (R_{DS} modulation). At higher currents, the BATFET will turn fully on (reaching its lowest R_{DSON}). From this point, increasing the discharge current will linearly increase the BATFET V_{DS} (determined by $R_{DSON} \times I_D$). Using the MOSFET linear mode at lower currents prevents swinging oscillation of entering and exiting the supplement mode.

BATFET gate regulation V-I characteristics is shown in Figure 13. If the battery voltage falls below its minimum depletion, the BATFET turns off and exits supplement mode.

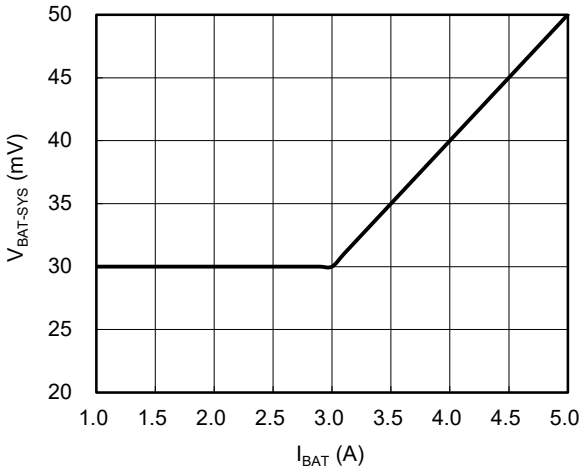


Figure 13. BATFET Gate Regulation V-I Curve

Temperature Qualification

The charging current and voltage of the battery must be limited when battery is cold or hot. A thermistor input for battery temperature monitoring is included in the device that can protect the battery based on JEITA guidelines. There is no battery temperature protection when the Buck-Boost converter stops switching.

Compliance with JEITA Guideline

JEITA guideline (April 20, 2007 release) is implemented in the device for safe charging of the Li-Ion battery. JEITA highlights the considerations and limits that should be considered for charging at cold or hot battery temperatures. High charge current and voltage must be avoided outside normal operating temperatures (typically 0℃ and 60℃). Four temperature levels are defined by JEITA from T1 (minimum) to T4 (maximum). Outside this range, charging should be stopped. The battery cool range is between T1 and T2, and the warm range is between T3 and T4. Charge must be limited in the cool and warm ranges.

One of the conditions for starting a charge cycle is having the battery temperature within V_{T1} to V_{T4} window limits. If the battery is too cold or too hot during charging and TS voltage exceeds the T1 - T4 limits, charging is suspended (zero charge current) and the controller waits for the battery temperature to come back within the T1 to T4 window.

DETAILED DESCRIPTION (continued)

JEITA recommends reducing charge current to 1/2 of fast charging current or lower at cool temperatures (T1 - T2). For warmer temperature (within T3 - T4 range), charge voltage is recommended to be kept below 4.1V/cell.

The SGM41574 follows the JEITA requirement by its flexible charge parameter settings. Figure 14 shows the TS charging values. At warm temperature range (T3 - T4), the charge voltage can be set by JEITA_VSET[2:0] register. At both warm temperature range (T3 - T4) and cool temperature range (T1 - T2), the fast charge current can be set to 100%, 40%, or 20% of I_{CHG} or charge suspend through JEITA_ISETH[1:0] bits and JEITA_ISETC[1:0] bits, respectively. When the "cool" or "warm" temperature is detected, the charge termination feature is still enabled.

At warm temperature range (T3 - T4), the large VREG reduction setting by JEITA_VSET[2:0] register may cause the VBAT_OVP fault during the VREG transition if the battery voltage is closed to the VREG before battery entering the warm temperature range.

The safety timer may be changed in warm temperature range (T3 - T4) and cool temperature range (T1 - T2), depends on the charge voltage setting by JEITA_VSET[2:0] and charge current setting by JEITA_ISETH[1:0] and JEITA_ISETC[1:0] registers. If the charge current is unchanged, the safety timer keeps unchanged. If the charge is suspended (set by either JEITA_VSET[2:0] = 00 or JEITA_ISETH[1:0] = 00), the safety time is suspended. If the charge current is reduced to 20% or 40%, the safety timer counts at half clock rate.

The SGM41574 senses the battery temperature from TS pin, which connects an external NTC resistor voltage divider from REGN. The corresponding voltages sensed by NTC are named V_{T1} to V_{T4}. Due to the sensor negative resistance, a higher temperature results in a lower voltage on TS pin.

The SGM41574 provides programmable comparators threshold for V_{T2} and V_{T3} in forward charge mode. The host can get more flexible configuration by setting TS_COOL[1:0] and TS_WARM[1:0] registers.

The SGM41574 has 4 TS_STAT bits to indicate the battery temperature range, including TS_COLD_STAT, TS_COOL_STAT, TS_WARM_STAT and TS_HOT_STAT. When the battery temperature changes among the different range, the corresponding TS status bit and TS flag bit will be set to 1, an nINT is pulsed to notify the host if the corresponding TS mask bit is set to 0. If the battery temperature is not required to monitor, the SGM41574 ignores the TS pin voltage during both charging mode and OTG mode by setting TS_IGNORE = 1. In this case, all the 4 TS_STAT bits are always reported to 0.

The typical TS resistor network is recommended as shown in Figure 15.

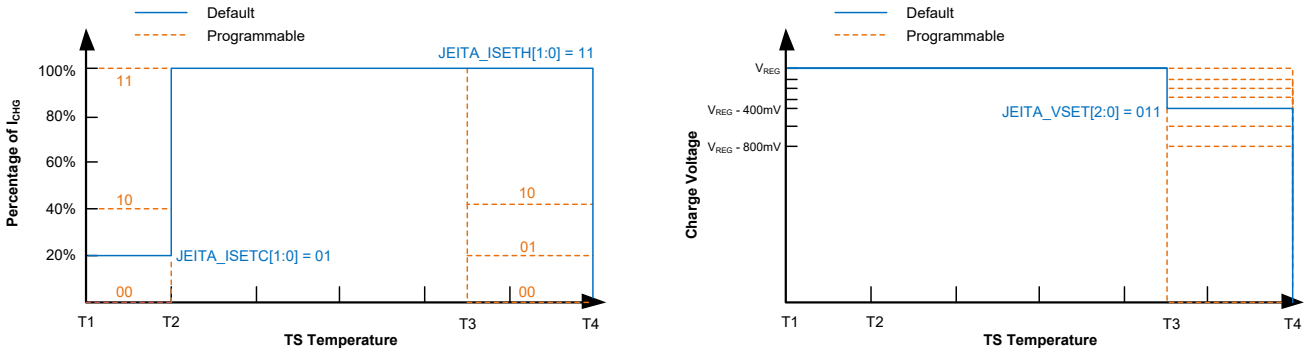


Figure 14. TS Charging Values

DETAILED DESCRIPTION (continued)

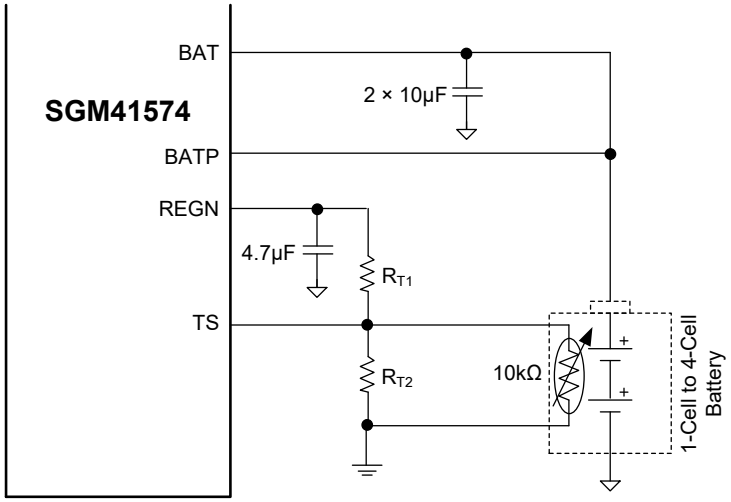


Figure 15. TS Resistor Network

A 103AT-2 type thermistor is recommended to use for the SGM41574. Other thermistors with the bias network (see Figure 15) can be calculated based on the following equations:

$$R_{T2} = \frac{R_{THCOLD} \times R_{THHOT} \times \left(\frac{1}{V_{T1}} - \frac{1}{V_{T4}}\right)}{R_{THHOT} \times \left(\frac{1}{V_{T4}} - 1\right) - R_{THCOLD} \times \left(\frac{1}{V_{T1}} - 1\right)} \quad (1)$$

$$R_{T1} = \frac{\left(\left(\frac{1}{V_{T1}}\right) - 1\right)}{\left(\frac{1}{R_{T2}}\right) + \left(\frac{1}{R_{THCOLD}}\right)} \quad (2)$$

Where, V_{T1} and V_{T4} are T_{COLD} and T_{HOT} threshold voltages on TS pin as percentage to V_{REGN}, R_{THCOLD} and R_{THHOT} are thermistor resistances (R_{TH}) at desired T1 (Cold) and T4 (Hot) temperatures. Select T_{COLD} = 0℃ and T_{HOT} = 60℃ for Li-Ion or Li-polymer batteries. For a 103AT-2 type thermistor R_{THCOLD} = 27.28kΩ and R_{THHOT} = 3.02kΩ, the calculation results are: R_{T1} = 5.39kΩ and R_{T2} = 34.68kΩ.

OTG Mode Temperature Monitoring

The SGM41574 is capable of monitoring the battery temperature for safety during the OTG mode. The temperature must remain within the V_{BCOLDx} to V_{BHOTx} thresholds, otherwise the OTG mode will be suspended and VBUS_STAT[3:0] bits are set to 0000. Moreover, the corresponding TS_STAT bit is updated to report OTG mode cold or hot condition. Once the temperature returns within the normal window, the OTG mode is resumed and the corresponding TS_STAT bit report to 0.

The SGM41574 provides programmable comparators threshold for V_{BCOLDx} and V_{BHOTx} in OTG mode. The host can get more flexible configuration by setting BCOLD and BHOT[1:0] registers.

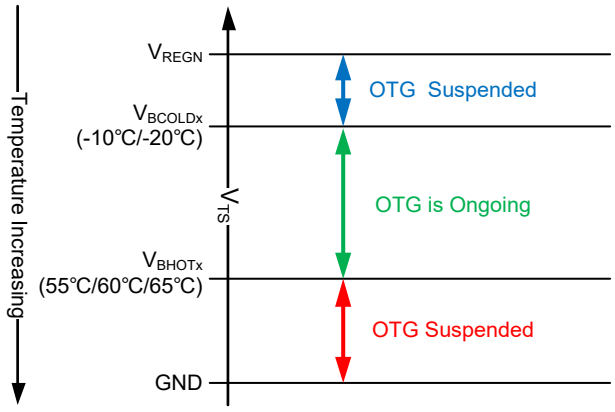


Figure 16. TS Pin Thermistor Sense Threshold in OTG Mode

DETAILED DESCRIPTION (continued)

Ship FET Control

The SGM41574 also supports ship mode, shutdown mode and system power reset feature by connecting an external N-channel ship FET (SFET). Connect the gate of SFET to charger's SDRV pin, the source of SFET to BAT pin and the drain to the battery, the application circuit for external SFET is shown as Figure 17. Through setting the SDRV_CTRL[1:0] register, the host can control some internal logic block and the on/off state of SFET to force IC entering different operation mode according to the application requirement.

If the ship FET is not populated, connect the battery to BAT pin directly and a 1nF capacitor from SDRV to GND is recommended.

After POR, the SFET_PRESENT bit is default 0, the SGM41574 doesn't support the features associated with the SFET. The SDRV_CTRL[1:0] register is always locked to 00 (IDEL mode) when SFET_PRESENT = 0, even if the SFET is populated. In IDEL mode, the SFET is fully turned on. The internal BATFET status depends on the charging status.

Ship Mode

Configuring the SDRV_CTRL[1:0] register to 10 can set the SGM41574 into ship mode. The SDRV_DLY bit is used to set the delay time from configuring SDRV_CTRL[1:0] = 10 to the charger entering the ship mode. In ship mode, the I²C keeps active but the internal BATFET and external SFET are both turned off. This mode is designed for battery only application. It is target to save quiescent current in idle, storage or shipping condition and extend the battery life.

Once one of the following events happens, the SGM41574 exits the ship mode and resets the SDRV_CTRL[1:0] register to 00:

• Host configures SDRV_CTRL[1:0] bits to 00.

• Host configures REG_RST bit to 1, the SDRV_CTRL[1:0] bits are reset to 00.

• Host configures EN_OTG bit to 1.

• An adaptor is plugged in.

• nQON pin changes to low for t_{SM_EXIT} (programmable via WKUP_DLY bit).

Shutdown Mode

Configuring the SDRV_CTRL[1:0] register to 01 can set the SGM41574 into shutdown mode. The SDRV_DLY bit is used to set the delay time from configuring SDRV_CTRL[1:0] = 01 to the charger entering the shutdown mode. In shutdown mode, the I²C is disabled, the internal BATFET and external SFET are both turned off. This mode is designed for battery only application. It is target to further minimize the battery leakage current. Only by plugging in an adaptor can wake up SGM41574 from shutdown mode with the SDRV_CTRL[1:0] register bits being reset to 00.

System Power Reset

Configuring the SDRV_CTRL[1:0] register to 11 can reset the system power. The SDRV_DLY bit is used to set the delay time from configuring SDRV_CTRL[1:0] = 11 to the charger starting to reset the system power. After the delay time, the SGM41574 enters HIZ mode if VBUS is valid and turns off the SFET for 350ms, then exits the HIZ mode and turns on the SFET again. The I²C is active and BATFET keeps the status unchanged during system power reset. There is an internal 30mA sink current on SYS pin during the 350ms period. After the SFET turns on again, the SDRV_CTRL[1:0] register automatically return to 00.

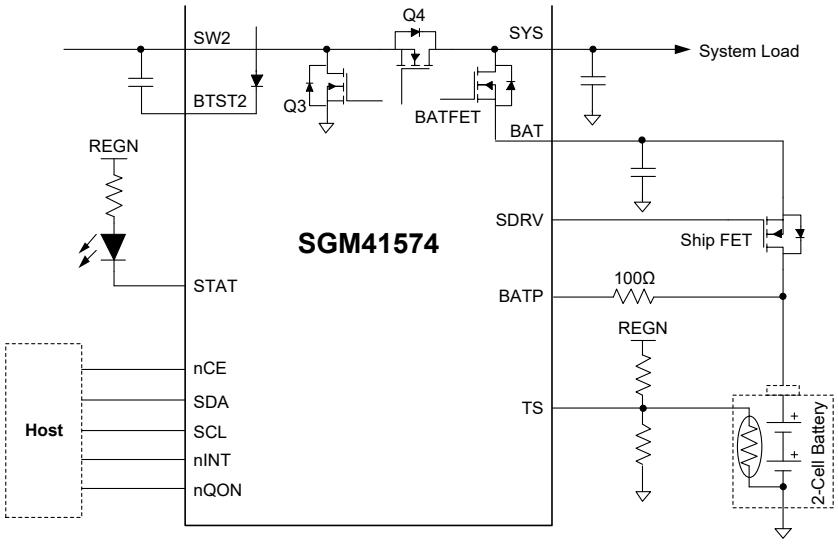


Figure 17. The Application Circuit for the External Ship FET

DETAILED DESCRIPTION (continued)

Besides configuring the SDRV_CTRL[1:0] register to 11, pulling nQON pin low for 10s also resets the power system. These two methods always take affect no matter the SGM41574 is in forward charging mode or battery only condition.

Integrated 16-Bit ADC for Monitoring

The integrated 16-bit ADC in SGM41574 allows the user to get critical system information for optimizing the charger behavior. The ADC related functions are controlled by ADC control register. The EN_ADC bit gives the option to enable or disable the ADC for power save purpose. The ADC conversion behavior can be set to continuous or one-shot mode through the ADC_RATE bit. The EN_ADC bit is automatically cleared once a one-shot conversion cycle completes. Re-assert EN_ADC bit can start a new conversion. Set ADC_AVG bit to 1 to enable the ADC running average algorithm, and the ADC average initial value can be configured by ADC_AVG_INIT bit.

When V_{BAT} > 3.4V (TYP) or V_{VBUS} > $V_{VBUS_PRESENT}$, configure EN_ADC bit to 1 to enable the ADC. The SGM41574 will not perform the ADC conversion if V_{BAT}, V_{VBUS}, and V_{VAC} are all invalid, and the ADC result registers will not be updated. In addition, the SGM41574 resets EN_ADC bit without sending any pulse on nINT pin. The ADC behaves the same if the EN_ADC bit is set while all ADC channels' enable bits are 0. The ADC conversion is interrupted if the charger mode changes during ADC conversion running (e.g. EN_OTG bit goes to 1, EN_HIZ bit goes to 1 or an adaptor plug-in). The ADC resumes with the interrupted channel when the mode change is completed. The host can freely enable or disable the ADC conversion by EN_ADC bit control, even if the charger is in HIZ mode or battery only condition.

The ADC sampling rate is programmable via ADC_SAMPLE[1:0] bits, and the conversion time (t_{ADC_CONV}) for each measurement is changed according to the ADC_SAMPLE[1:0] bits setting. If the sampling rate is programmed during an ADC conversion period, the ADC conversion will reconvert the current channel with the new sampling rate, and the channels that have already finished the ADC conversion will keep the value of the old sampling rate.

By default, the ADC function disable registers (REG0x2F and REG0x30) bits are all zero and all ADC channel will be converted in both continuous and one-shot conversion modes. If one bit is set to 1 in ADC function disable registers before the conversion, the corresponding channel ADC conversion data is not updated to the ADC result registers. In this case, the data host read-back from the ADC result register is from the default POR value or the last valid ADC conversion. If one bit is set to 1 during the ADC conversion cycle, the SGM41574 finishes this channel conversion in this cycle, but does not convert this channel in next cycle. In continuous conversion mode, as long as the EN_ADC bit is set to 1, the ADC circuitry is active even if all ADC channels are disabled. Once one bit in ADC function disable registers is set to 0, the ADC conversion begins soon.

In continuous conversion mode, the ADC_DONE_STAT bit keeps 0 and ADC_DONE_FLAG bit remains unchanged. The ADC_DONE_STAT and ADC_DONE_FLAG bits are set when a one-shot conversion is completed.

For IBAT_ADC channel, the ADC read-back conditions and information are summarized in Table 9.

Table 9. ADC Read-Back Conditions and Information

Conditions	IBAT_ADC
Forward Charging Mode (Trickle Charge, Pre-Charge, Fast Charge, Taper Charge)	Able to read (positive)
Supplement Mode	N/A (1)
Charge Disabled or Termination	0
OTG Mode	Able to read (negative)
Battery Only (EN_OTG = 0)	Able to read (negative)
With Adapter but EN_HIZ = 1, System is Powered by Battery	N/A (1)

NOTE: 1. N/A means that the IBAT_ADC read-back value is approximately 10mA, but not the actual current value.

To exit the ADC measurement, one of following ways is possible to do:

1. Write EN_ADC = 0, the ADC measurement stops immediately. The last valid ADC measurement value can be read back from the ADC measurement result registers.
2. Write all ADC channel disable bits in ADC function disable registers to 1. The ADC stops after the current cycle measurement is completed.
3. Write ADC_RATE to one-shot conversion mode. The ADC stops after one cycle measurement is completed.

If an adaptor is plugged in, the ADC suspends, and it resumes after SGM41574 finishes the input source detection. Other than that, ADC conversion always keeps normal operation even a fault occurs in SGM41574.

DETAILED DESCRIPTION (continued)

Status Output Pins (STAT and nINT)

Power Good Indicator (PG_STAT Bit)

When a good input source is connected to VBUS, the PG_STAT status bit goes high. The PG_FLAG is set. An nINT is pulsed to notify the host if the PG_MASK = 0. A good input source is detected if all following conditions on V_{VBUS} are satisfied:

1. $V_{VBUS_PRESENT} < V_{VBUS} < V_{VBUS_OVP}$.
2. $V_{VBUS} > V_{BAD_SRC} + V_{BAD_SRC_HYS}$ (250mV TYP) during 30ms test period in which the I_{BAD_SRC} (35mA TYP) current is pulled from VBUS.

Charge Status (STAT Pin)

The SGM41574 provides an open-drain STAT pin. Connect this pin to logic high rail through a 2.2kΩ resistor and LED series for charge status indication. Set STAT_DIS bit to 1 can disable the STAT pin indication function.

Table 10. STAT Pin Function

Charging State	STAT Pin and LED Indicator
Charging in progress (not including charging in top-off timer)	Low (LED ON)
Charging completed	High (LED OFF)
HIZ mode, charging is disabled	High (LED OFF)
Battery only mode and OTG mode	High (LED OFF)
Charge is suspended (a fault condition which suspend charging)	Blinking at 1Hz (LED BLINKING)

nINT Interrupt Output Pin

When a new update occurs in the charger states, a 256μs negative pulse is sent through the nINT pin to interrupt the host. The host may not continuously monitor the charger device and by receiving the interrupt, it can react and check the charger situation on time. By default, each of the following events will generate an nINT pulse.

1. Good input power source detected.
   a) $V_{VBUS} < V_{VBUS_OVP}$
   b) $V_{VBUS} > V_{BAD_SRC}$ when I_{BAD_SRC} current is applied
2. Good input power source removed.
3. Entering junction temperature regulation.
4. Entering VINDPM regulation.
5. Entering IINDPM regulation.
6. Watchdog timer expired.
7. VBUS_STAT[3:0] register changes.
8. TS_STAT (one of 4 status registers) changes.
9. CHG_STAT[2:0] register changes, including charge complete.
10. Junction temperature shutdown.
11. VBUS over-voltage detected.
12. VAC over-voltage detected.
13. VBAT over-voltage detected.
14. VSYS over-voltage detected.
15. IBUS over-current detected.
16. IBAT over-current detected.
17. Charge safety timer expired.
18. A rising edge on any of the *_STAT bits of REG0x1B to REG0x21.

If the event mask bit is set to 1, the corresponding nINT pulse does not sent out when the event happens. For each event, there are three related bits:

1. STAT bit: hold the current status.
2. FLAG bit: hold nINT event information, ignore the current status.
3. MASK bit: prevent the event from sending out nINT.

When each of the above events occurs, the SGM41574 sends out an nINT pulse and report the event source through the corresponding FLAG registers. After the host reads the FLAG bits, they are automatically reset to 0, and to re-assert the FLAG requires a new rising edge on STAT bit.

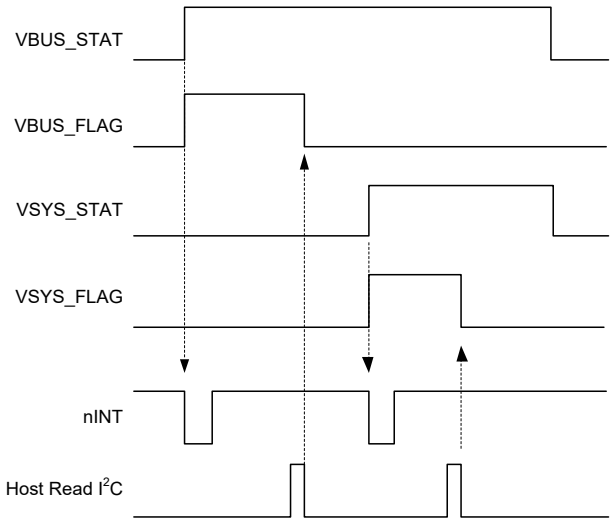


Figure 18. Example of nINT Generation Behavior

DETAILED DESCRIPTION (continued)

Protection Features

Monitoring of Voltage and Current

The device closely monitors the input, system and battery voltage and current, as well as internal FET currents for safe converter operation. The list of the faults protection provided by the charger is as follows:

- VAC Over-Voltage Protection (VAC_OVP)
- VBUS Over-Voltage Protection (VBUS_OVP)
- VBUS Under-Voltage Protection (POORSRC)
- System Over-Voltage Protection (VSYS_OVP)
- System Short Protection (VSYS_SHORT)
- Battery Over-Voltage Protection (VBAT_OVP)
- Battery Over-Current Protection (IBAT_OCP)
- Input Over-Current Protection (IBUS_OCP)
- OTG Over-Voltage Protection (OTG_OVP)
- OTG Under-Voltage Protection (OTG_UVP)

VAC Over-Voltage Protection (VAC_OVP)

In single input with ACFETx-RBFETx configuration (suffix "x" means 1 or 2), if the VACx is higher than the VAC_OVP rising threshold, SGM41574 turns off the ACFETx_RBFETx immediately, the EN_ACDRVx is changed to 0 and VACx_OVP_STAT = 1. Then the VBUS falls down and SGM41574 stops switching. If VACx falls below the VAC_OVP falling threshold, the ACFETx_RBFETx automatically turns on, EN_ACDRVx is changed to 1 and VACx_OVP_STAT = 0. The SGM41574 resumes to normal operation again.

In dual input with ACFET1-RBFET1 and ACFET2-RBFET2 configuration, VAC1 and VAC2 are both valid present. During the operation, if VACa is higher than the VAC_OVP rising threshold (suffix "a" means 1 or 2, depending on which comes first, "b" means the other input source), the EN_ACDRVa is changed to 0 and ACFETa-RBFETa turns off, then EN_ACDRVb changes to 1 and ACFETb-RBFETb turns on, the VBUS voltage switches from VACa to VACb. And the VACa_OVP_STAT keeps 1 until VACa falls below VAC_OVP falling threshold.

VBUS Over-Voltage Protection (VBUS_OVP)

The SGM41574 will stop switching as soon as VBUS voltage exceeds the VBUS_OVP rising threshold. During VBUS_OVP, the SGM41574 sets the VBUS_OVP_STAT and VBUS_OVP_FLAG bits, and reports an nINT pulse if VBUS_OVP_MASK = 0. The REGN keeps on, and STAT pin blinks at 1Hz during VBUS_OVP. After the VBUS_OVP condition disappears, the SGM41574 automatically resumes switching again.

VBUS Under-Voltage Protection (POORSRC)

The input voltage range for SGM41574 operation is above V_{BAD_SRC} and below V_{VBUS_OVP}. If the VBUS falls below the V_{BAD_SRC}, the SGM41574 stops switching, PG_STAT and BC1.2_DONE_STAT bits are set to 0. After VBUS rises up to V_{BAD_SRC} + $V_{BAD_SRC_HYS}$, the SGM41574 runs the poor source qualification and the input source type detection again, and then resumes switching.

System Over-Voltage Protection (VSYS_OVP)

During the system load transient, the SGM41574 clamps the system voltage to protect system components from over-voltage. The VSYS_OVP threshold is designed as 110% of system regulation voltage. Once the system voltage triggers the VSYS_OVP, the SGM41574 stops switching and a 30mA sink current is applied to SYS pin to pull the voltage down. And the SGM41574 sets the VSYS_OVP_STAT and VSYS_OVP_FLAG bits, and reports an nINT pulse if VSYS_OVP_MASK = 0.

System Short Protection (VSYS_SHORT)

To protect system from overloading or short-circuit event, the SGM41574 compares the V_{SYS} to V_{SYS_SHORT}. If the IINDPM is triggered and the heavy load further causes the SYS voltage drop to trigger the V_{SYS_SHORT} threshold, the SGM41574 stops switching and automatically tries to resume from this condition if VSYS_SHORT_DIS bit = 0. If 7 consecutive retry failures are detected, the EN_HIZ bit is set automatically. If VSYS_SHORT_DIS bit = 1, the SGM41574 does not stop switching and the current limit is triggered cycle-by-cycle after entering system short protection. The SGM41574 sets the VSYS_SHORT_STAT and VSYS_SHORT_FLAG bits, and reports an nINT to the host if VSYS_SHORT_MASK = 0.

Battery Over-Voltage Protection (VBAT_OVP)

The over-voltage protection threshold of battery pin is 4% above the programmed battery regulation voltage (VREG) during charging phase. In a case of VBAT_OVP, the charging stops right away, the SGM41574 sets the VBAT_OVP_STAT and VBAT_OVP_FLAG bits, and reports an nINT pulse to host if the VBAT_OVP_MASK bit is set to 0. During VBAT_OVP, a 30mA sink current is applied to BAT pin if EN_AUTO_IBATDIS = 1.

DETAILED DESCRIPTION (continued)

Battery Over-Current Protection (IBAT_OCP)

With SFET configuration, if the battery discharging current triggers the IBAT_OCP threshold under SFET_PRESENT = 1 and EN_BATOC = 1 conditions, both BATFET and SFET turn off immediately and the device enters the ship mode. The SGM41574 sets the IBAT_OCP_STAT and IBAT_OCP_FLAG bits, and reports an nINT pulse if IBAT_OCP_MASK = 0. If a valid adaptor is present, the SGM41574 will automatically retry the detection every 80ms delay time until the over-current fault condition disappears.

Input Over-Current Protection (IBUS_OCP)

In forward mode, if the input current triggers the IBUS_OCP threshold with EN_IBUS_OCP = 1 configuration, the SGM41574 stops switching, and sets the ACDRV_DIS = 1 and EN_HIZ = 1 to enter HIZ mode immediately. Meanwhile, the SGM41574 sets IBUS_OCP_STAT and IBUS_OCP_FLAG bits, and reports an nINT pulse to the host if IBUS_OCP_MASK = 0.

OTG Over-Voltage Protection (OTG_OVP)

In OTG mode, the over-voltage protection threshold of VBUS pin is 13% above the programmed VOTG. If OTG_OVP is triggered, the SGM41574 stops switching right away, and a 30mA sink current is applied to VBUS pin. The SGM41574 sets the OTG_OVP_STAT and OTG_OVP_FLAG, and reports an nINT pulse to the host if OTG_OVP_MASK = 0. During OTG_OVP, the REGN keeps on, EN_OTG bit keeps 1 and VBUS_STAT keeps 0111 (in OTG mode). After the OTG_OVP condition disappears, the SGM41574 automatically resumes switching again.

OTG Under-Voltage Protection (OTG_UVP)

In OTG mode, when the OTG output current triggers the OTG current limit and VBUS voltage drops below V_{OTG_UVP} threshold, the SGM41574 stops switching and automatically tries to resume from this condition if OTG_UVP_DIS bit = 0. If 7 consecutive retry failures are detected, the EN_OTG bit is cleared and REGN turns off. If OTG_UVP_DIS bit = 1, the SGM41574 does not stop switching and the current limit is triggered cycle-by-cycle after entering OTG_UVP. The SGM41574 sets the OTG_UVP_STAT, OTG_UVP_FLAG bits, and reports an nINT to the host if OTG_UVP_MASK = 0.

Thermal Regulation and Thermal Shutdown

The SGM41574 internal junction temperature (T_J) is always monitored to avoid overheating. A limit of +120℃ is considered for maximum IC surface temperature in both forward charging mode and OTG mode, and if T_J intends to exceed this level, the device reduces the charge current or OTG output current to keep maximum temperature limited to +120℃ (thermal regulation mode) and sets the TREG_STAT bit to 1. As expected, the charging current is always lower than programmed value under thermal regulation conditions. The safety timer runs at half clock rate, and the charge termination is disabled. The TREG_STAT and TREG_FLAG bits are set to 1, and an nINT is pulsed to notify the host if TREG_MASK = 0.The thermal regulation temperature is programmable from +60℃ to +120℃ with 20℃ step by TREG[1:0] bits.

If the junction temperature exceeds T_{SHUT}, which is programmable through TSHUT[1:0] register, thermal shutdown protection arise in which the converter is turned off, the SGM41574 sets the TSHUT_STAT and TSHUT_FLAG bits, and reports an nINT pulse if TSHUT_MASK = 0. When the T_J falls below the hysteresis band of T_{SHUT_HYS} (30℃ under T_{SHUT}), the converter resumes switching automatically.

I²C Serial Interface

Standard I²C interface is used to program SGM41574 parameters and get status reports. I²C is the well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM41574 operates as a slave device that address is 0x6B (6BH). It has 41 8-bit registers and 16 16-bit registers, numbered from REG0x00 to REG0x48. A register read beyond REG0x48 (0x48) returns 0xFF.

Physical Layer

The standard I²C interface of SGM41574 supports standard mode and fast mode communication speeds. The frequency of standard mode is up to 100kbits/s, while the fast mode is up to 400kbits/s. Bus lines are pulled high by weak current source or pull-up resistors are in logic high state with no clocking when the bus is free. The SDA pin is open-drain.

DETAILED DESCRIPTION (continued)

I²C Data Communication

START and STOP Conditions

A transaction is started through taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 19. All transactions are started by master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is generated by master when SCL is high and a high to low transition on the SDA. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. After a START and before a STOP, the bus is considered busy. By the way, only a master can send out the START and STOP signals.

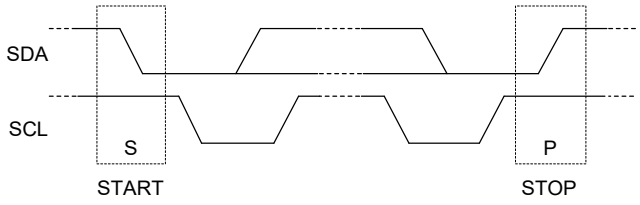


Figure 19. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable during clock high period. The state of SDA can only change when SCL is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 20.

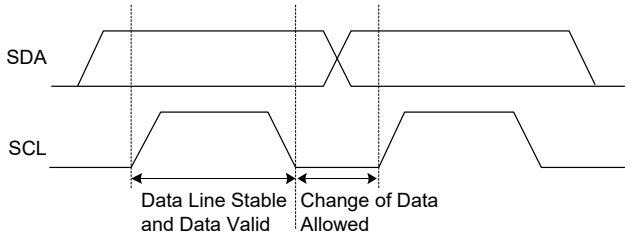


Figure 20. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. Figure 21 shows the byte transfer process with I²C interface.

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and the eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually, the second byte is also a WRITE, sending the register address that is supposed to be accessed in the next byte(s). The 7-bit slave address is 1101011b (0x6B). The address bit arrangement is shown in Figure 22 and Figure 23.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 24 for a single write data transfer. After receiving the ACK, the master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 25), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, the master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

DETAILED DESCRIPTION (continued)

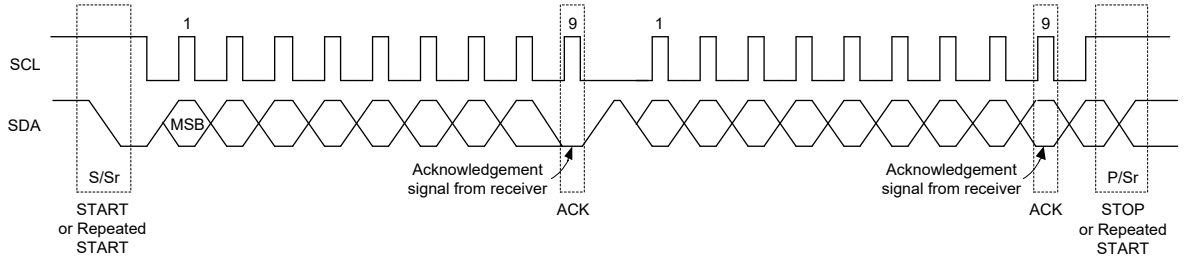


Figure 21. Byte Transfer Process

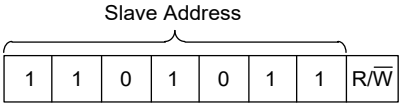


Figure 22. 7-Bit Address Format (0x6B)

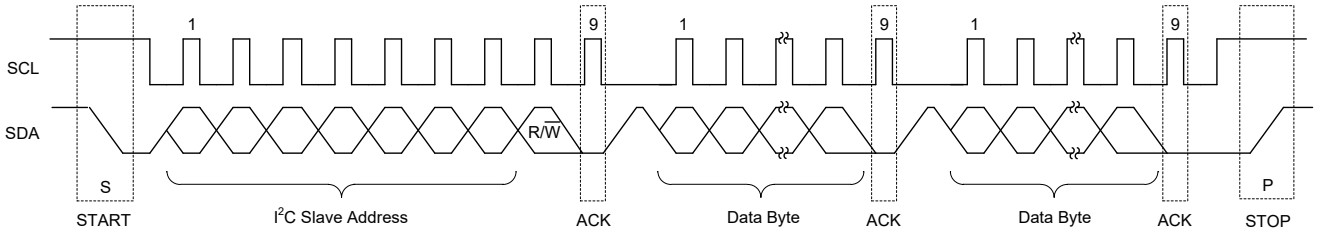


Figure 23. Data Transfer Transaction

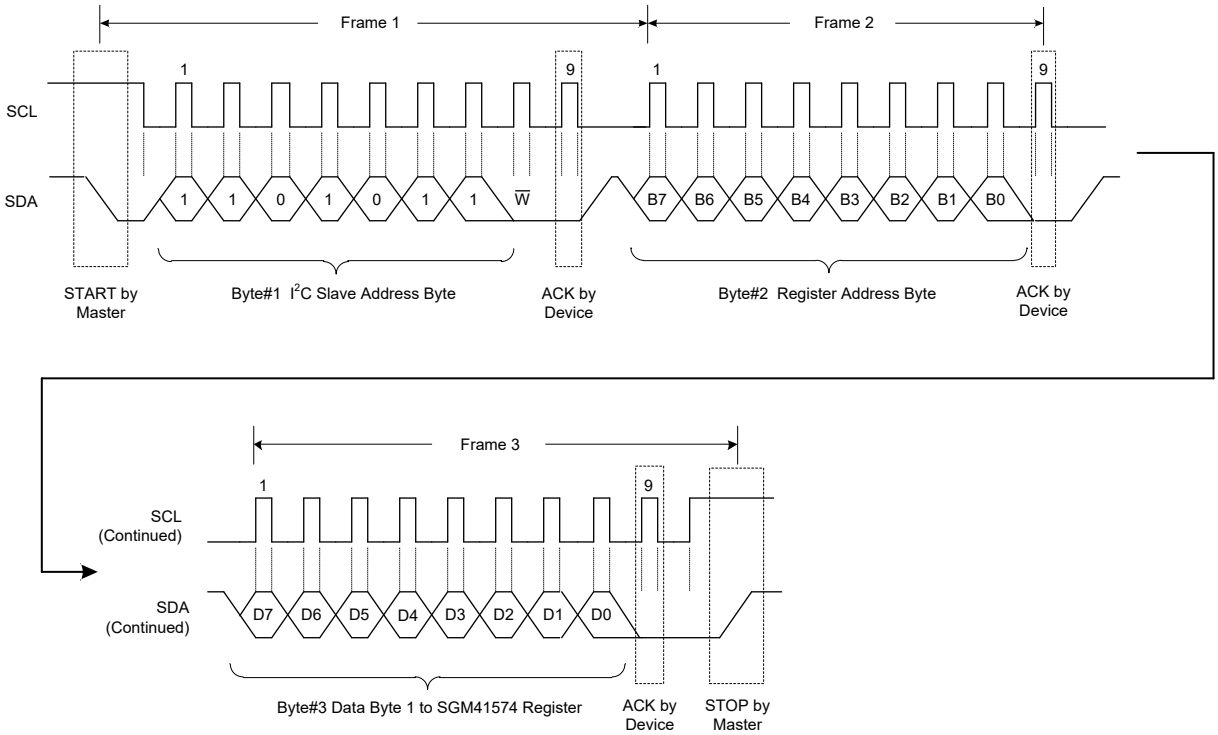


Figure 24. A Single Write Transaction

DETAILED DESCRIPTION (continued)

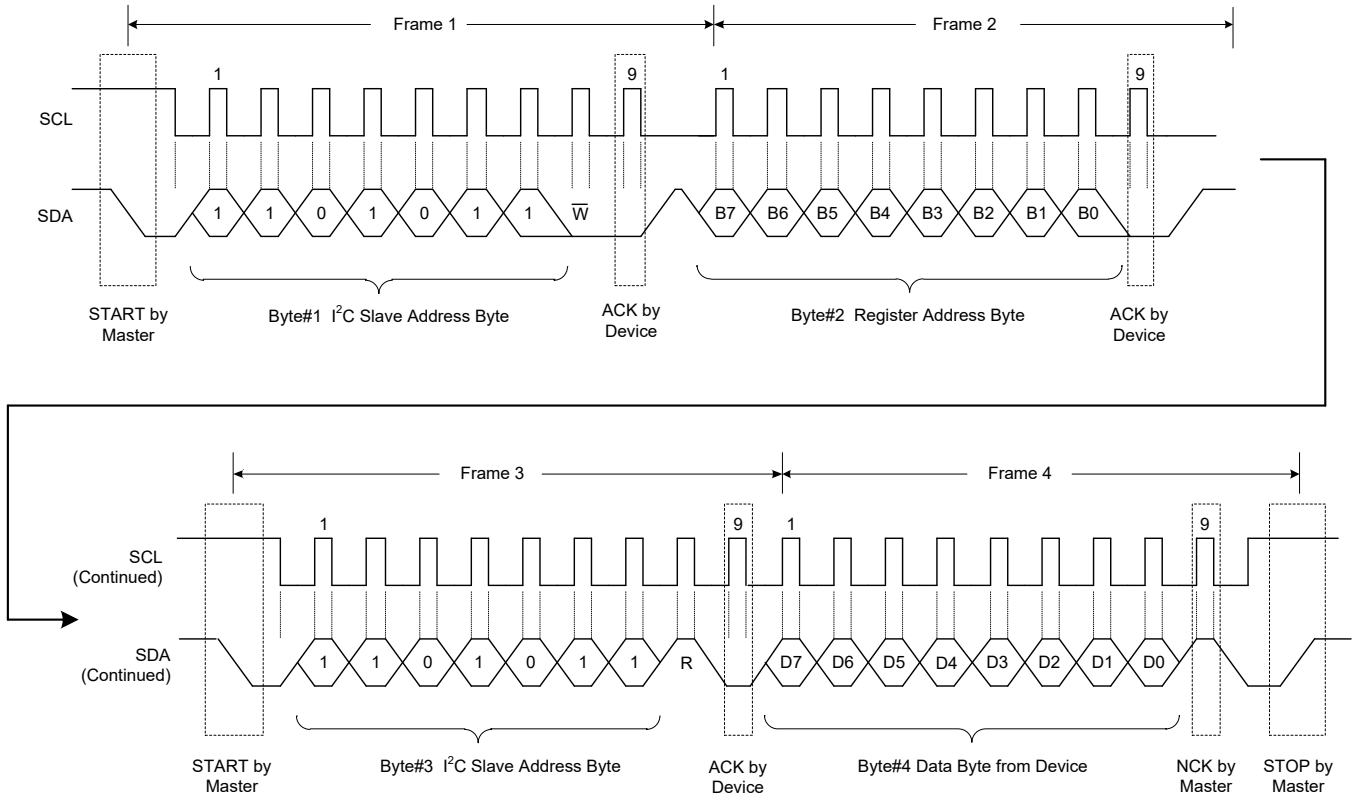


Figure 25. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM41574 for REG0x00 through REG0x48 registers, as explained in Figure 26 and Figure 27.

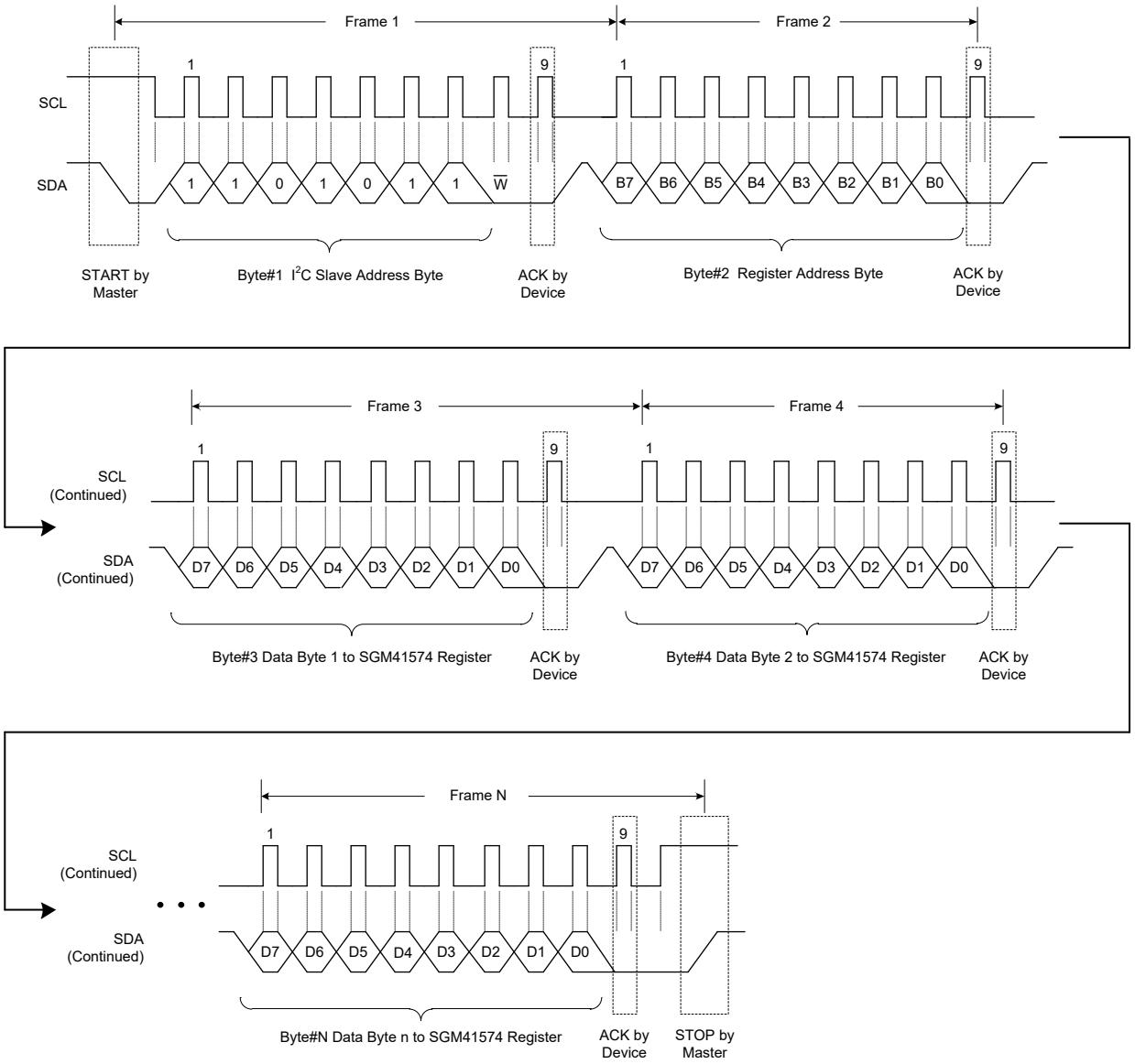


Figure 26. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

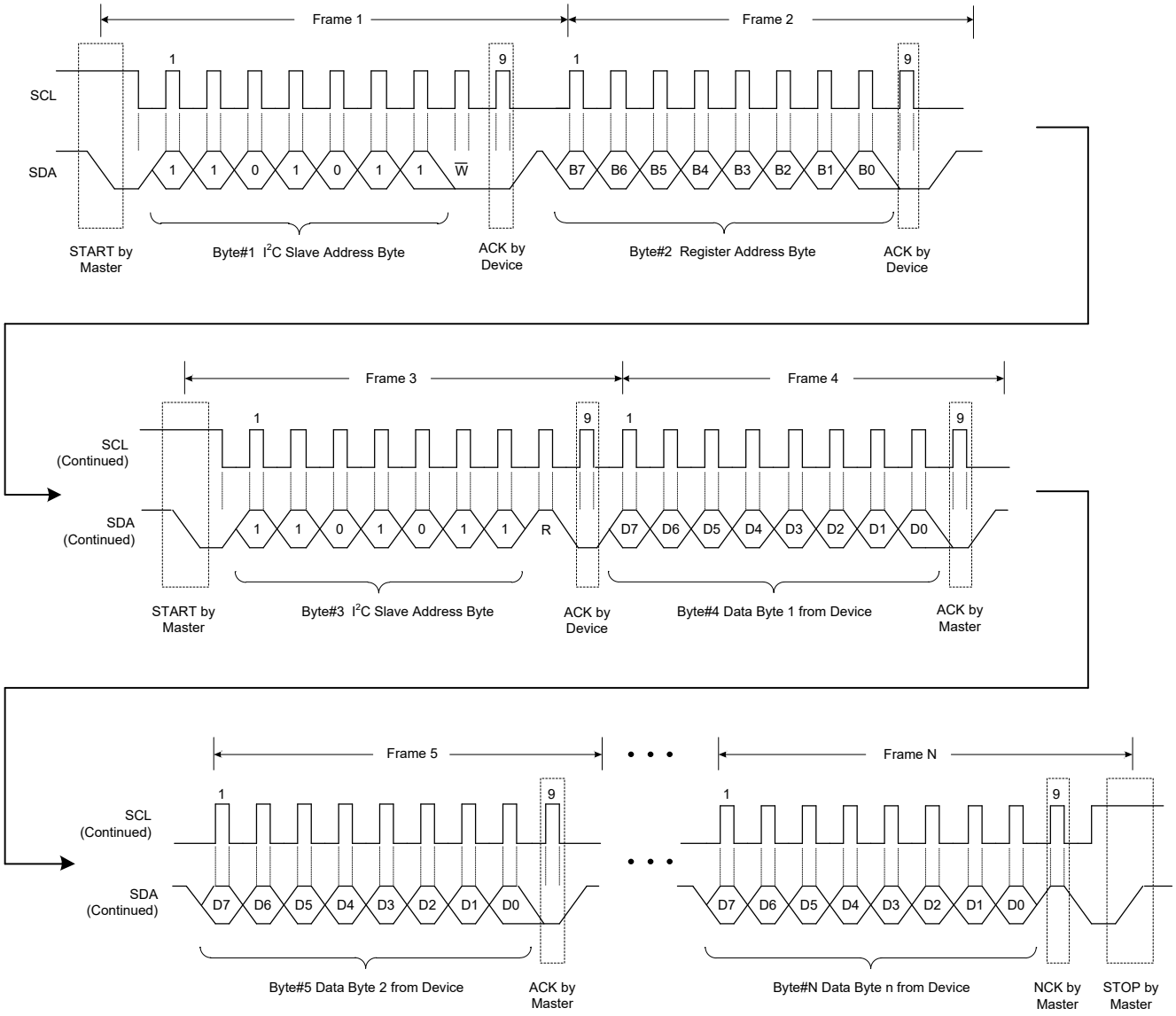


Figure 27. A Multi-Read Transaction

DETAILED DESCRIPTION (continued)

Device Functional Modes

Host Mode and Default Mode

After power-on reset, the SGM41574 starts in default mode (standalone) with all registers reset as default. If the watchdog timer is expired, the device will also enter default mode. When the host is in sleep mode or there is no host, the device stays in the default mode in which the SGM41574 operates like an autonomous charger. There are 3 charging safety timer (shown in Figure 10) corresponding to different charge phase to protect the battery from abnormal charging status. After the safety timer has expired, the SGM41574 stops charging the battery by turning off the BATFET, while the Buck-Boost converter continuously supplies the system load without shutdown.

When the SGM41574 enters the default mode, the WD_STAT and WD_FLAG bits are set to 1, and an nINT is pulsed to notify the host if WD_MASK = 0. Some registers are reset to default POR values (noted in the Register Maps section) in default mode. Any I²C register writing take the SGM41574 out of default mode with the watchdog timer reset. To avoid the charger back to default mode again, the host can set WATCHDOG[2:0] bits = 000 to disable the watchdog timer, or set WD_RST = 1 before the timer expires.

Register Bit Reset

The SGM41574 provides REG_RST bit to reset some registers to default POR values (noted in the Register Maps section) by setting the REG_RST = 1. The REG_RST bit automatically returns to 0 after the reset is completed.

The FORCE_VINDPM_DET and FORCE_INDET bits can be reset to default 0 immediately when REG_RST bit is set to 1, therefore, the register reset may terminate the process of forced VINDPM ADC measurement, or the forced D+/D- detection.

The REG_RST = 1 neither initiates the POR detection nor repeats the VINDPM ADC measurement.

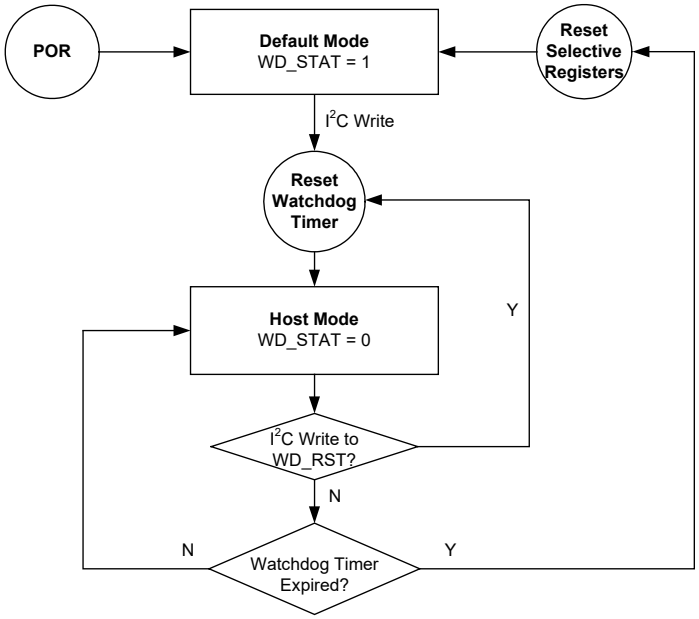


Figure 28. Watchdog Timer Flow Chart

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Register Address Map

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE	DELAY
CHG	0x1C[7:5]	0x23[7]	0x29[7]	—	0x0F[5]	—
VSYSMIN	0x1E[4]	0x24[4]	0x2A[4]	0x00[5:0]	—	—
VREG	—	—	—	0x01[2:0] + 0x02[7:0]	—	—
ICHG	—	—	—	0x03[0] + 0x04[7:0]	—	—
IPRECHG	—	—	—	0x08[5:0]	—	—
ITERM	—	—	—	0x09[4:0]	—	—
VINDPM	0x1B[6]	0x22[6]	0x28[6]	0x05[7:0]	—	—
IINDPM	0x1B[7]	0x22[7]	0x28[7]	0x06[0] + 0x07[7:0]	0x14[2]	—
EXTILIM	—	—	—	—	0x14[1]	—
VBAT_LOWV	—	—	—	0x08[7:6]	—	—
RECHG	—	—	—	0x0A[3:0]	—	0x0A[5:4]
REG_RST	—	—	—	—	0x09[6]	—
CELL	—	—	—	0x0A[7:6]	—	—
OTG	—	—	—	—	0x12[6]	—
VOTG	—	—	—	0x0B[2:0] + 0x0C[7:0]	—	—
IOTG	—	—	—	0x0D[6:0]	—	—
PRECHG_TMR	0x1E[1]	0x24[1]	0x2A[1]	0x0D[7]	0x0E[4]	—
TRICHG_TMR	0x1E[2]	0x24[2]	0x2A[2]	—	0x0E[5]	—
CHG_TMR	0x1E[3]	0x24[3]	0x2A[3]	0x0E[2:1]	0x0E[3]	—
TOPOFF_TMR	—	0x24[0]	0x2A[0]	0x0E[7:6]	0x0E[7:6]	—
TMR2X	—	—	—	—	0x0E[0]	—
AUTO_IBATDIS	—	—	—	—	0x0F[7]	—
FORCE_IBATDIS	—	—	—	—	0x0F[6]	—
ICO	0x1D[7:6]	0x23[6]	0x29[6]	—	0x0F[4]	—
FORCE_ICO	—	—	—	—	0x0F[3]	—
ICO_ILIM	—	—	—	0x19[0] + 0x1A[7:0]	—	—
HIZ	—	—	—	—	0x0F[2]	—
TERM	—	—	—	—	0x0F[1]	—
WD_RST	—	—	—	—	0x10[3]	—
WATCHDOG	0x1B[5]	0x22[5]	0x28[5]	0x10[2:0]	—	—
AUTO_INDET	—	—	—	—	0x11[6]	—
FORCE_INDET	—	—	—	—	0x11[7]	—
FORCE_VINDPM_DET	—	—	—	—	0x13[1]	—
HVDCP	—	—	—	—	0x11[3]	—
9V HVDCP	—	—	—	—	0x11[4]	—
12V HVDCP	—	—	—	—	0x11[5]	—
ACDRV	—	—	—	—	0x12[7]	—
ACDRV1	—	—	—	—	0x13[6]	—
ACDRV2	—	—	—	—	0x13[7]	—

REGISTER MAPS (continued)

I²C Register Address Map (continued)

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE	DELAY
SDRV_CTRL	0x11[2:1]	—	—	—	—	0x11[0]
Wake up by nQON	—	—	—	—	—	0x12[3]
PFM_FWD	—	—	—	—	0x12[4]	—
FWD_OOA	—	—	—	—	0x12[0]	—
PFM_OTG	—	—	—	—	0x12[5]	—
OTG_OOA	—	—	—	—	0x12[1]	—
BATFET LDO	—	—	—	—	0x12[2]	—
PWM_FREQ	—	—	—	0x13[5]		—
STAT Pin	—	—	—	—	0x13[4]	—
IBAT_REG	0x20[7]	0x26[7]	0x2C[7]	0x14[4:3]	—	—
SFET_PRESENT	—	—	—	—	0x14[7]	—
VBUS_PD	—	—	—	—	0x16[3]	—
VAC1_PD	—	—	—	—	0x16[2]	—
VAC2_PD	—	—	—	—	0x16[1]	—
POORSRC	0x1B[4]	0x22[4]	0x28[4]	—	—	—
PG	0x1B[3]	0x22[3]	0x28[3]	—	—	—
VBUS	0x1C[4:1]	0x23[4]	0x29[4]	—	—	—
BC1.2_DONE	0x1C[0]	0x23[0]	0x29[0]	—	—	—
DPDM_DONE	0x1D[1]	0x24[6]	0x2A[6]	—	—	—
AC1_PRESENT	0x1B[1]	0x22[1]	0x28[1]	—	—	—
AC2_PRESENT	0x1B[2]	0x22[2]	0x28[2]	—	—	—
ACRB1	0x1E[6]	—	—	—	—	—
ACRB2	0x1E[7]	—	—	—	—	—
VBUS_PRESENT	0x1B[0]	0x22[0]	0x28[0]	—	—	—
VBAT_PRESENT	0x1D[0]	0x23[1]	0x29[1]	—	—	—
TREG	0x1D[2]	0x23[2]	0x29[2]	0x16[7:6]	—	—
TSHUT	0x21[2]	0x27[2]	0x2D[2]	0x16[5:4]	—	—
IBUS_OCP	0x20[4]	0x26[4]	0x2C[4]	—	0x13[0]	—
IBAT_OCP	0x20[3]	0x26[3]	0x2C[3]	—	0x14[7] + 0x14[0]	—
CONV_OCP	0x20[2]	0x26[2]	0x2C[2]	—	—	—
VAC1_OVP	0x20[0]	0x26[0]	0x2C[0]	0x10[5:4]	—	—
VAC2_OVP	0x20[1]	0x26[1]	0x2C[1]	0x10[5:4]	—	—
VBUS_OVP	0x20[6]	0x26[6]	0x2C[6]	—	—	—
VBAT_OVP	0x20[5]	0x26[5]	0x2C[5]	—	—	—
VSYS_OVP	0x21[6]	0x27[6]	0x2D[6]	—	—	—
OTG_OVP	0x21[5]	0x27[5]	0x2D[5]	—	—	—
VSYS_SHORT	0x21[7]	0x27[7]	0x2D[7]	—	0x13[3]	—
OTG_UVP	0x21[4]	0x27[4]	0x2D[4]	—	0x13[2]	—

REGISTER MAPS (continued)

I²C Register Address Map (continued)

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE
TS_IGNORE	—	—	—	—	0x18[0]
TS_COLD	0x1F[3]	0x25[3]	0x2B[3]	0x18[1] (OTG)	—
TS_COOL	0x1F[2]	0x25[2]	0x2B[2]	0x18[7:6] (Forward)	—
TS_WARM	0x1F[1]	0x25[1]	0x2B[1]	0x18[5:4] (Forward)	—
TS_HOT	0x1F[0]	0x25[0]	0x2B[0]	0x18[3:2] (OTG)	—
JEITA_VSET	—	—	—	0x17[7:5]	—
JEITA_ISETH	—	—	—	0x17[4:3]	—
JEITA_ISETC	—	—	—	0x17[2:1]	—
ADC	0x1E[5]	0x24[5]	0x2A[5]	—	0x2E[7]
ADC_RATE	—	—	—	0x2E[6]	—
ADC_SAMPLE	—	—	—	0x2E[5:4]	—
ADC_AVG	—	—	—	—	0x2E[3]
ADC_AVG_INIT	—	—	—	0x2E[2]	—
DPLUS_DAC	—	—	—	0x47[7:5]	—
DMINUS_DAC	—	—	—	0x47[4:2]	—
PN	—	—	—	0x48[5:3]	—
DEV_REV	—	—	—	0x48[2:0]	—

REGISTER MAPS (continued)

Bit Types:

R/W: Read/Write bit(s)

R: Read only bit(s)

RC: Bit(s) cleared to 0 by being read

R/WC: Read/Write. Writing a 1 clears the bit. Writing a 0 has no effect.

REG0x00: Minimal_System_Voltage Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved.	N/A
D[5:0]	VSYSMIN[5:0]	xx xxxx	R/W	Minimum System Voltage Limit 00 0000 = 2.5V 00 0001 = 2.75V 00 0010 = 3V ... ... 00 0100 = 3.5V (1-cell default) ... ... 01 0010 = 7V (2-cell default) ... ... 01 1010 = 9V (3-cell default) ... ... 10 0110 = 12V (4-cell default) ... ... 11 0110 = 16V 11 0111 to 11 1111 = 16V Note: The SGM41574 reads the PROG pin resistance during POR, and then sets the default cell count and the corresponding default V_{SYSMIN}.	REG_RST

REG0x01: Charge_Voltage_Limit Register [Reset = 0x0XXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:11]	Reserved	0 0000	R	Reserved.	N/A
D[10:0]	VREG[10:0]	xxx xxxx xxxx	R/W	Battery Voltage Regulation Limit 000 0000 0000 to 001 0010 1011 setting will be ignored. 001 0010 1100 = 3V 001 0010 1101 = 3.01V 001 0010 1110 = 3.02V … … 001 1010 0100 = 4.2V (1-cell default) … … 011 0100 1000 = 8.4V (2-cell default) … … 100 1110 1100 = 12.6V (3-cell default) …… 110 1001 0000 = 16.8V (4-cell default) … … 111 0101 1000 = 18.8V 111 0101 1001 to 111 1111 1111 setting will be ignored. Note: The SGM41574 reads the PROG pin resistance during POR, and then sets the default cell count and the corresponding default VREG. Multi-write transaction is required for REG0x01 and REG0x02.	REG_RST

REGISTER MAPS (continued)

REG0x03: Charge_Current_Limit Register [Reset = 0x0XXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:9]	Reserved	000 0000	R	Reserved.	N/A
D[8:0]	ICHG[8:0]	x xxxx xxxx	R/W	Charge Current Limit 0 0000 0000 to 0 0000 0100 setting will be ignored. 0 0000 0101 = 50mA 0 0000 0110 = 60mA 0 0000 0111 = 70mA … … 0 0110 0100 = 1A (3-cell and 4-cell default) … … 0 1100 1000 = 2A (1-cell and 2-cell default) … … 1 1111 0100 = 5A 1 1111 0101 to 1 1111 1111 setting will be ignored. Note: The SGM41574 reads the PROG pin resistance during POR, and then sets the default cell count and the corresponding default ICHG. Multi-write transaction is required for REG0x03 and REG0x04.	REG_RST or Watchdog

REG0x05: Input_Voltage_Limit Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VINDPM[7:0]	xxxx xxxx	R/W	Absolute VINDPM Threshold 0000 0000 to 0010 0011 = 3.6V 0010 0100 = 3.6V 0010 0101 = 3.7V 0010 0110 = 3.8V … … 1101 1010 = 21.8V 1101 1011 = 21.9V 1101 1100 = 22V 1101 1101 to 1111 1111 = 22V Note: 1. When the VBUS is plugged in, the SGM41574 updates the VINDPM[7:0] default value to be VBUS0 - 0.7V (VBUS0 < 7V) or VBUS0 - 1.4V (7V ≤ VBUS0 ≤ 22V). The VINDPM[7:0] register default value is clamped to 22V when VBUS0 ≥ 22V (TYP). The VBUS0 means VBUS at no load condition. 2. The VINDPM is not reset by WATCHDOG and REG_RST.	–

REG0x06: Input_Current_Limit Register [Reset = 0x012C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:9]	Reserved	000 0000	R	Reserved.	N/A
D[8:0]	IINDPM[8:0]	1 0010 1100	R/W	IINDPM Threshold Setting Bits 0 0000 0000 to 0 0000 1001 setting will be ignored. 0 0000 1010 = 100mA 0 0000 1011 = 110mA … … 0 00110010 = 500mA (USB SDP default) … … 0 10010110 = 1.5A (USB CDP and HVDCP default) … … 1 0010 1100 = 3A (POR and Unknown Adaptor default) … … 1 0100 0101 = 3.25A (USB DCP default) … … 1 0100 1010 = 3.3A 1 0100 1011 to 1 1111 1111 setting will be ignored. Non-Standard Adaptor default IINDPM may be 1A, 2.1A or 2.4A. Note: When the VBUS is plugged in, the SGM41574 updates the IINDPM according to input source type (IINDPM is also clamped by ILIM (setting by V_{ILIM_HIZ}). The IINDPM > ILIM setting will be ignored. Multi-write transaction is required for REG0x06 and REG0x07.	REG_RST

REGISTER MAPS (continued)

REG0x08: Pre-Charge_Control Register [Reset = 0xC3]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	VBAT_LOWV[1:0]	11	R/W	Pre-Charge to Fast Charge Transition Threshold for Battery Voltage 00 = 15.3% × V_{REG} 01 = 64% × V_{REG} 10 = 68.7% × V_{REG} 11 = 73.3% × V_{REG} (default) Note: If V_{BAT_LOWV} < V_{BAT_SHORTZ}, there is no pre-charge phase.	REG_RST
D[5:0]	IPRECHG[5:0]	00 0011	R/W	Pre-Charge Current Limit 00 0000 = 40mA 00 0001 = 40mA 00 0010 = 80mA 00 0011 = 120mA (default) … … 11 0001 = 1960mA 11 0010 = 2000mA 11 0011 to 11 1111 = 2000mA	REG_RST or Watchdog

REG0x09: Termination_Control Register [Reset = 0x05]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved.	N/A
D[6]	REG_RST	0	R/WC	Reset Registers to Default Values and Reset Timer 0 = Not reset (default) 1 = Reset (this bit goes to 0 after the reset is completed)	–
D[5]	Reserved	0	R	Reserved.	N/A
D[4:0]	ITERM[4:0]	0 0101	R/W	Termination Current 0 0000 = 40mA 0 0001 = 40mA 0 0010 = 80mA … … 0 0101 = 200mA (default) … … 1 1000 = 960mA 1 1001 = 1000mA 1 1010 to 1 1111 = 1000mA	REG_RST or Watchdog

REG0x0A: Re-Charge_Control Register [Reset = 0xX3]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	CELL[1:0]	xx	R/W	Cell Count Setting 00 = 1-cell 01 = 2-cell 10 = 3-cell 11 = 4-cell Note: The SGM41574 reads the PROG pin resistance during POR, and then sets the default cell count	–
D[5:4]	TRECHG[1:0]	10	R/W	Battery Recharge Deglitch Time 00 = 64ms 01 = 256ms 10 = 1024ms (default) 11 = 2048ms	REG_RST or Watchdog
D[3:0]	VRECHG[3:0]	0011	R/W	Battery Recharge Threshold Offset (below VREG) 0000 = 50mV 0001 = 100mV 0010 = 150mV 0011 = 200mV (default) … … 1110 = 750mV 1111 = 800mV	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x0B: VOTG_Regulation Register [Reset = 0x00DC]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:11]	Reserved	0 0000	R	Reserved.	N/A
D[10:0]	VOTG[10:0]	000 1101 1100	R/W	OTG Output Regulation Voltage 000 0000 0000 = 2800mV 000 0000 0001 = 2810mV 000 0000 0010 = 2820mV … … 000 1101 1100 = 5000mV (default) … … 111 0111 1111 = 21990mV 111 1000 0000 = 22000mV 111 1000 0001 to 111 1111 1111 setting will be ignored. Note: Multi-write transaction is required for REG0x0B and REG0x0C.	REG_RST or Watchdog

REG0x0D: IOTG_Regulation Register [Reset = 0x4B]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PRECHG_TMR	0	R/W	Pre-Charge Safety Timer Setting 0 = 2h (default) 1 = 0.5h	REG_RST or Watchdog
D[6:0]	IOTG[6:0]	100 1011	R/W	OTG Current Limit 000 0000 to 000 0010 = 120mA 000 0011 = 120mA 000 0100 = 160mA 000 0101 = 200mA … … 100 1011 = 3000mA (default) … … 101 0010 = 3280mA 101 0011 = 3320mA 101 0100 to 111 1111 = 3320mA	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x0E: Timer_Control Register [Reset = 0x3D]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	TOPOFF_TMR[1:0]	00	R/W	Top-Off Timer Control 00 = Disabled (default) 01 = 15mins 10 = 30mins 11 = 45mins	REG_RST or Watchdog
D[5]	EN_TRICHG_TMR	1	R/W	Enable Trickle Charge Timer (Fixed as 1h) 0 = Disabled 1 = Enabled (default)	REG_RST or Watchdog
D[4]	EN_PRECHG_TMR	1	R/W	Enable Pre-Charge Timer 0 = Disabled 1 = Enabled (default)	REG_RST or Watchdog
D[3]	EN_CHG_TMR	1	R/W	Enable Fast Charge Timer 0 = Disabled 1 = Enabled (default)	REG_RST or Watchdog
D[2:1]	CHG_TMR[1:0]	10	R/W	Fast Charge Timer Setting 00 = 5h 01 = 8h 10 = 12h (default) 11 = 24h	REG_RST or Watchdog
D[0]	EN_TMR2X	1	R/W	EN_TMR2X 0 = Trickle charge, pre-charge and fast charge timer are not slowed by 2× during input DPM or thermal regulation 1 = Trickle charge, pre-charge and fast charge timer are slowed by 2× during input DPM or thermal regulation (default)	REG_RST or Watchdog

REG0x0F: Charger_Control_0 Register [Reset = 0xA2]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_AUTO_IBATDIS	1	R/W	Enable the Auto Battery Discharging during the Battery OVP Fault 0 = The charger will not apply a discharging current on BAT during battery OVP 1 = The charger will apply a discharging current on BAT during battery OVP (default)	REG_RST
D[6]	FORCE_IBATDIS	0	R/W	Force a Battery Discharging Current 0 = Idle (default) 1 = Force the charger to apply a discharging current on BAT regardless the battery OVP status	REG_RST
D[5]	EN_CHG	1	R/W	Charger Enable Configuration 0 = Charge disable 1 = Charge enable (default)	REG_RST or Watchdog
D[4]	EN_ICO	0	R/W	Input Current Optimizer (ICO) Enable 0 = Disable ICO (default) 1 = Enable ICO	REG_RST
D[3]	FORCE_ICO	0	R/WC	Force Start Input Current Optimizer (ICO) 0 = Do not force ICO (default) 1 = Force ICO start (this bit goes to 0 after ICO algorithm starts, it is only valid when EN_ICO = 1)	REG_RST or Watchdog
D[2]	EN_HIZ	0	R/W	Enable HIZ Mode 0 = Disable (default) 1 = Enable	REG_RST
D[1]	EN_TERM	1	R/W	Enable Termination 0 = Disable 1 = Enable (default)	REG_RST or Watchdog
D[0]	Reserved	0	R	Reserved.	N/A

REGISTER MAPS (continued)

REG0x10: Charger_Control_1 Register [Reset = 0x05]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved.	N/A
D[5:4]	VAC_OVP[1:0]	00	R/W	VAC_OVP Thresholds 00 = 26V (default) 01 = 22V 10 = 12V 11 = 7V	REG_RST
D[3]	WD_RST	0	R/WC	I²C Watchdog Timer Reset 0 = Normal (default) 1 = Reset (this bit goes back to 0 after timer resets)	REG_RST or Watchdog
D[2:0]	WATCHDOG[2:0]	101	R/W	Watchdog Timer Settings 000 = Disable 001 = 0.5s 010 = 1s 011 = 2s 100 = 20s 101 = 40s (default) 110 = 80s 111 = 160s Note: The watchdog timer will not restart if modifying the WATCHDOG[2:0] register before the watchdog timer expires.	REG_RST

REG0x11: Charger_Control_2 Register [Reset = 0x40]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	FORCE_INDET	0	R/WC	Force D+/D- Detection 0 = Do not force D+/D- detection (default) 1 = Force D+/D- algorithm, when D+/D- detection is done, this bit will be reset to 0	REG_RST or Watchdog
D[6]	EN_AUTO_INDET	1	R/W	Automatic D+/D- Detection Enable 0 = Disable D+/D- detection when VBUS is plugged in 1 = Enable D+/D- detection when VBUS is plugged in (default)	REG_RST or Watchdog
D[5]	EN_12V	0	R/W	EN_12V HVDC 0 = Disable 12V mode in HVDCP (default) 1 = Enable 12V mode in HVDCP	REG_RST
D[4]	EN_9V	0	R/W	EN_9V HVDC 0 = Disable 9V mode in HVDCP (default) 1 = Enable 9V mode in HVDCP	REG_RST
D[3]	EV_HVDCP	0	R/W	High Voltage DCP Enable 0 = Disable HVDCP handshake (default) 1 = Enable HVDCP handshake	REG_RST
D[2:1]	SDRV_CTRL[1:0]	00	R/W	SFET Control The external ship FET control logic can force the device to enter different modes. 00 = Idle (default) 01 = Shutdown mode 10 = Ship mode 11 = System power reset Notes: 1. The SDRV_CTRL[1:0] bits are always locks to 00 when SFET_PRESENT = 0, even if the SFET is populated. 2. If the external SFET is not populated, it is recommended to keep the SDRV_CTRL[1:0] bits to 00.	REG_RST
D[0]	SDRV_DLY	0	R/W	Delay Time Added to the Taking Action in Bits [2:1] of the SFET Control 0 = Add 10s delay time (default) 1 = Do not add 10s delay time	REG_RST

REGISTER MAPS (continued)

REG0x12: Charger_Control_3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ACDRV_DIS	0	R/W	When this bit is set, the charger will force both EN_ACDRV1 = 0 and EN_ACDRV2 = 0.	–
D[6]	EN_OTG	0	R/W	OTG Mode Control 0 = OTG disable (default) 1 = OTG enable	REG_RST or Watchdog
D[5]	PFM_OTG_DIS	0	R/W	Disable PFM in OTG Mode 0 = Enable (default) 1 = Disable Note: It is not recommended to write PFM_OTG_DIS = 1 in OTG Boost mode.	REG_RST or Watchdog
D[4]	PFM_FWD_DIS	0	R/W	Disable PFM in Forward Mode 0 = Enable (default) 1 = Disable	REG_RST
D[3]	WKUP_DLY	0	R/W	Time required to pull the nQON pin low when waking up the device from ship mode (t_{SM_EXIT}). 0 = 1s (default) 1 = 15ms	REG_RST
D[2]	LDO_DIS	0	R/W	Disable BATFET LDO Mode in Pre-Charge Stage 0 = Enable (default) 1 = Disable	REG_RST or Watchdog
D[1]	OTG_OOA_DIS	0	R/W	Disable OOA in OTG Mode 0 = Enable (default) 1 = Disable	REG_RST or Watchdog
D[0]	FWD_OOA_DIS	0	R/W	Disable OOA in Forward Mode 0 = Enable (default) 1 = Disable	REG_RST

REGISTER MAPS (continued)

REG0x13: Charger_Control_4 Register [Reset = 0xX1]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_ACDRV2	0	R/W	External ACFET2-RBFET2 Gate Driver Control and Indication 0 = Turn off (default) 1 = Turn on	–
D[6]	EN_ACDRV1	0	R/W	External ACFET1-RBFET1 Gate Driver Control and Indication 0 = Turn off (default) 1 = Turn on	–
D[5]	PWM_FREQ	x	R/W	Switching Frequency Selection 0 = 1.5MHz 1 = 750kHz Note: The SGM41574 reads the PROG pin resistance during POR, and then sets the default switching frequency.	–
D[4]	STAT_DIS	0	R/W	Disable the STAT Pin Output 0 = Enable (default) 1 = Disable	REG_RST or Watchdog
D[3]	VSYS_SHORT_DIS	0	R/W	Disable Forward Mode VSYS Short Hiccup Protection 0 = Enable (default) 1 = Disable	REG_RST
D[2]	OTG_UVP_DIS	0	R/W	Disable OTG Mode OTG UVP Hiccup Protection 0 = Enable (default) 1 = Disable	REG_RST
D[1]	FORCE_VINDPM_DET	0	R/WC	Force VINDPM Detection 0 = Do not force VINDPM detection (default) 1 = Force the converter stop switching, and ADC measures the VBUS voltage without input current, then the charger updates the VINDPM register accordingly. Notes: 1. This bit goes back to 0 after the VINDPM[7:0] register is reset. 2. The VINDPM detection only can be done when $V_{BAT} > V_{SYSMIN}$.	REG_RST
D[0]	EN_IBUS_OCP	1	R/W	Enable IBUS_OCP in Forward Mode 0 = Disable 1 = Enable (default)	REG_RST

REGISTER MAPS (continued)

REG0x14: Charger_Control_5 Register [Reset = 0x16]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	SFET_PRESENT	0	R/W	0 = No ship FET populated (The EN_BATOC bit and SDRV_CTRL[1:0] bits are locked to 0 even if the SFET is populated) 1 = Ship FET populated (The EN_BATOC bit and SDRV_CTRL[1:0] bits are programmable and the SGM41574 can support all the features associated with the SFET) Note: If the external SFET is not populated, it is recommended to keep the SFET_PRESENT bit to 0.	–
D[6:5]	Reserved	00	R	Reserved.	N/A
D[4:3]	IBAT_REG[1:0]	10	R/W	Battery Discharging Current Regulation in OTG Mode 00 = 3A 01 = 4A 10 = 5A (default) 11 = Disable	REG_RST or Watchdog
D[2]	EN_IINDPM	1	R/W	Enable the Internal IINDPM Register Input Current Regulation and the OTG Current Limit in OTG Mode 0 = Disable 1 = Enable (default)	REG_RST or Watchdog
D[1]	EN_EXTILIM	1	R/W	Enable the External ILIM_HIZ Pin Input Current Regulation 0 = Disable 1 = Enable (default)	REG_RST
D[0]	EN_BATOC	0	R/W	Enable the Battery Discharging Current OCP 0 = Disable (default) 1 = Enable Note: The EN_BATOC bit is always locked to 0 when SFET_PRESENT = 0, even if the SFET is populated.	REG_RST or Watchdog

REG0x15: Reserved Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	Reserved	0000 0000	R	Reserved.	N/A

REG0x16: Temperature_Control Register [Reset = 0xC0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	TREG[1:0]	11	R/W	Thermal Regulation Thresholds 00 = 60℃ 01 = 80℃ 10 = 100℃ 11 = 120℃ (default)	REG_RST or Watchdog
D[5:4]	TSHUT[1:0]	00	R/W	Thermal Shutdown Thresholds 00 = 150℃ (default) 01 = 130℃ 10 = 120℃ 11 = 85℃	REG_RST or Watchdog
D[3]	EN_VBUS_PD	0	R/W	Enable VBUS Pull-Down Resistor (6kΩ) 0 = Disable (default) 1 = Enable	REG_RST
D[2]	EN_VAC1_PD	0	R/W	Enable VAC1 Pull-Down Resistor 0 = Disable (default) 1 = Enable	REG_RST
D[1]	EN_VAC2_PD	0	R/W	Enable VAC2 Pull-Down Resistor 0 = Disable (default) 1 = Enable	REG_RST
D[0]	Reserved	0	R	Reserved.	N/A

REGISTER MAPS (continued)

REG0x17: NTC_Control_0 Register [Reset = 0x7A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	JEITA_VSET[2:0]	011	R/W	JEITA High Temperature Range (T_{WARM} - T_{HOT}) Charge Voltage Setting 000 = Charge suspend 001 = Set V_{REG} to V_{REG} - 800mV 010 = Set V_{REG} to V_{REG} - 600mV 011 = Set V_{REG} to V_{REG} - 400mV (default) 100 = Set V_{REG} to V_{REG} - 300mV 101 = Set V_{REG} to V_{REG} - 200mV 110 = Set V_{REG} to V_{REG} - 100mV 111 = V_{REG} unchanged	REG_RST or Watchdog
D[4:3]	JEITA_ISETH[1:0]	11	R/W	JEITA High Temperature Range (T_{WARM} - T_{HOT}) Charge Current Setting 00 = Charge suspend 01 = Set the charge current to 20% × I_{CHG} (fast charge stage) or 20% × I_{PRECHG} (pre-charge stage) 10 = Set the charge current to 40% × I_{CHG} (fast charge stage) or 40% × I_{PRECHG} (pre-charge stage) 11 = Charge current unchanged (default)	REG_RST or Watchdog
D[2:1]	JEITA_ISETC[1:0]	01	R/W	JEITA Low Temperature Range (T_{COLD} - T_{COOL}) Charge Current Setting 00 = Charge suspend 01 = Set the charge current to 20% × I_{CHG} (fast charge stage) or 20% × I_{PRECHG} (pre-charge stage) (default) 10 = Set the charge current to 40% × I_{CHG} (fast charge stage) or 40% × I_{PRECHG} (pre-charge stage) 11 = Charge current unchanged	REG_RST or Watchdog
D[0]	Reserved	0	R	Reserved.	N/A

REG0x18: NTC_Control_1 Register [Reset = 0x54]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	TS_COOL[1:0]	01	R/W	JEITA VT2 Comparator Voltage Rising Thresholds 00 = 71.7% (5℃) 01 = 69.1% (10℃) (default) 10 = 66.1% (15℃) 11 = 63% (20℃)	REG_RST or Watchdog
D[5:4]	TS_WARM[1:0]	01	R/W	JEITA VT3 Comparator Voltage Falling Thresholds 00 = 48.3% (40℃) 01 = 44.7% (45℃) (default) 10 = 41.1% (50℃) 11 = 37.6% (55℃)	REG_RST or Watchdog
D[3:2]	BHOT[1:0]	01	R/W	OTG Mode TS HOT Temperature Threshold 00 = 37.6% × V_{REGN} (55℃) 01 = 34.3% × V_{REGN} (60℃) (default) 10 = 31.2% × V_{REGN} (65℃) 11 = Disable	REG_RST or Watchdog
D[1]	BCOLD	0	R/W	OTG Mode TS COLD Temperature Threshold 0 = 77.5% × V_{REGN} (-10℃) (default) 1 = 80.4% × V_{REGN} (-20℃)	REG_RST or Watchdog
D[0]	TS_IGNORE	0	R/W	Ignore the TS feedback, the charger will consider that the TS is always good to allow the charging and OTG modes, all four TS status bits are always kept at 0000 to report the normal condition. 0 = Not ignore (default) 1 = Ignore	REG_RST or Watchdog

NOTE: The corresponding temperature in the brackets is based on R_{T1} = 5.24kΩ, R_{T2} = 30.31kΩ and a 103AT NTC thermistor.

REGISTER MAPS (continued)

REG0x19: ICO_Current_Limit Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:9]	Reserved	000 0000	R	Reserved.	N/A
D[8:0]	ICO_ILIM[8:0]	0000 00000	R	Actual Input Current Limit 0 0000 1010 = 100mA 0 0000 1011 = 110mA 0 0000 1100 = 120mA … … 1 0100 1000 = 3280mA 1 0100 1001 = 3290mA 1 0100 1010 = 3300mA	N/A

REG0x1B: Charger_Status_0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IINDPM_STAT	0	R	IINDPM Status (Forward Mode) or IOTG Status (OTG Mode) 0 = Normal (default) 1 = In IINDPM regulation or IOTG regulation	N/A
D[6]	VINDPM_STAT	0	R	VINDPM Status (Forward Mode) or VOTG Status (OTG Mode) 0 = Normal (default) 1 = In VINDPM regulation or VOTG regulation	N/A
D[5]	WD_STAT	0	R	I²C Watchdog Timer Status 0 = Normal (default) 1 = WD timer expired	N/A
D[4]	POORSRC_STAT	0	R	Poor Source Detection Status 0 = Normal (default) 1 = Weak adaptor detected	N/A
D[3]	PG_STAT	0	R	Power Good Status 0 = Not in power good status (default) 1 = Power good	N/A
D[2]	AC2_PRESENT_STAT	0	R	VAC2 Insert Status 0 = VAC2 not present (default) 1 = VAC2 present (above present threshold)	N/A
D[1]	AC1_PRESENT_STAT	0	R	VAC1 Insert Status 0 = VAC1 not present (default) 1 = VAC1 present (above present threshold)	N/A
D[0]	VBUS_PRESENT_STAT	0	R	VBUS Present Status 0 = VBUS not present (default) 1 = VBUS present (above present threshold)	N/A

REGISTER MAPS (continued)

REG0x1C: Charger_Status_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	CHG_STAT[2:0]	000	R	Charge Status Bits 000 = Not charging (default) 001 = Trickle charge 010 = Pre-charge 011 = Fast charge (CC mode) 100 = Taper charge (CV mode) 101 = Reserved 110 = Top-off timer active charging 111 = Charge termination done	N/A
D[4:1]	VBUS_STAT[3:0]	0000	R	VBUS Status Bits 0000 = No input or BHOT or BCOLD in OTG mode (default) 0001 = USB SDP (500mA) 0010 = USB CDP (1.5A) 0011 = USB DCP (3.25A) 0100 = Adjustable high voltage DCP (HVDCP) (1.5A) 0101 = Unknown adaptor (3A) 0110 = Non-standard Adaptor (1A/2.1A/2.4A) 0111 = In OTG mode 1000 = Not qualified adaptor 1001 = Reserved 1010 = Reserved 1011 = Reserved 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved	N/A
D[0]	BC1.2_DONE_STAT	0	R	BC1.2 Status Bit 0 = BC1.2 or non-standard detection not complete (default) 1 = BC1.2 or non-standard detection complete	N/A

REG0x1D: Charger_Status_2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	ICO_STAT[1:0]	00	R	Input Current Optimizer (ICO) Status 00 = ICO disabled (default) 01 = ICO optimization in progress 10 = Maximum input current detected 11 = Reserved	N/A
D[5:3]	Reserved	000	R	Reserved.	N/A
D[2]	TREG_STAT	0	R	IC Thermal Regulation Status 0 = Normal (default) 1 = Device in thermal regulation	N/A
D[1]	DPDM_STAT	0	R	D+/D- Detection Status Bits 0 = The D+/D- detection is not started yet, or the detection is done (default) 1 = The D+/D- detection is ongoing	N/A
D[0]	VBAT_PRESENT_STAT	0	R	Battery Present Status (V_{BAT} > V_{BAT_UVLOZ}) 0 = VBAT not present (default) 1 = VBAT present	N/A

REGISTER MAPS (continued)

REG0x1E: Charger_Status_3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ACRB2_STAT	0	R	The ACFET2-RBFET2 Status 0 = ACFET2-RBFET2 is not placed (default) 1 = ACFET2-RBFET2 is placed	N/A
D[6]	ACRB1_STAT	0	R	The ACFET1-RBFET1 Status 0 = ACFET1-RBFET1 is not placed (default) 1 = ACFET1-RBFET1 is placed	N/A
D[5]	ADC_DONE_STAT	0	R	ADC Conversion Status (in One-Shot Mode Only) 0 = Conversion not complete (default) 1 = Conversion complete	N/A
D[4]	VSYS_STAT	0	R	VSYS Regulation Status (Forward Mode) 0 = Not in VSYSMIN regulation (V_{BAT} > V_{SYSMIN}) (default) 1 = In VSYSMIN regulation (V_{BAT} < V_{SYSMIN})	N/A
D[3]	CHG_TMR_STAT	0	R	Fast Charge Timer Status 0 = Normal (default) 1 = Safety timer expired	N/A
D[2]	TRICHG_TMR_STAT	0	R	Trickle Charge Timer Status 0 = Normal (default) 1 = Safety timer expired	N/A
D[1]	PRECHG_TMR_STAT	0	R	Pre-Charge Timer Status 0 = Normal (default) 1 = Safety timer expired	N/A
D[0]	Reserved	0	R	Reserved.	N/A

REG0x1F: Charger_Status_4 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved.	N/A
D[4]	VBATOTG_LOW_STAT	0	R	The battery voltage is too low to enable OTG mode. 0 = The battery voltage is high enough to enable the OTG operation (default) 1 = The battery voltage is too low to enable the OTG operation	N/A
D[3]	TS_COLD_STAT	0	R	The TS temperature is in the cold range, lower than T1. 0 = TS status is not in the cold range (default) 1 = TS status is in the cold range	N/A
D[2]	TS_COOL_STAT	0	R	The TS temperature is in the cool range, between T1 and T2. 0 = TS status is not in cool range (default) 1 = TS status is in cool range	N/A
D[1]	TS_WARM_STAT	0	R	The TS temperature is in the warm range, between T3 and T4. 0 = TS status is not in the warm range (default) 1 = TS status is in the warm range	N/A
D[0]	TS_HOT_STAT	0	R	The TS temperature is in the hot range, higher than T4. 0 = TS status is not in the hot range (default) 1 = TS status is in the hot range	N/A

REGISTER MAPS (continued)

REG0x20: FAULT_Status_0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBAT_REG_STAT	0	R	IBAT Regulation Status 0 = Normal (default) 1 = Device in battery discharging current regulation	N/A
D[6]	VBUS_OVP_STAT	0	R	VBUS Over-Voltage Status 0 = Normal (default) 1 = Device in over-voltage protection	N/A
D[5]	VBAT_OVP_STAT	0	R	VBAT Over-Voltage Status 0 = Normal (default) 1 = Device in over-voltage protection	N/A
D[4]	IBUS_OCP_STAT	0	R	IBUS Over-Current Status 0 = Normal (default) 1 = Device in over-current protection	N/A
D[3]	IBAT_OCP_STAT	0	R	IBAT Over-Current Status 0 = Normal (default) 1 = Device in over-current protection	N/A
D[2]	CONV_OCP_STAT	0	R	Converter Over-Current Status 0 = Normal (default) 1 = Converter in over-current protection	N/A
D[1]	VAC2_OVP_STAT	0	R	VAC2 Over-Voltage Status 0 = Normal (default) 1 = Device in over-voltage protection	N/A
D[0]	VAC1_OVP_STAT	0	R	VAC1 Over-Voltage Status 0 = Normal (default) 1 = Device in over-voltage protection	N/A

REG0x21: FAULT_Status_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VSYS_SHORT_STAT	0	R	VSYS Short-Circuit Status 0 = Normal (default) 1 = Device in SYS short-circuit protection	N/A
D[6]	VSYS_OVP_STAT	0	R	VSYS Over-Voltage Status 0 = Normal (default) 1 = Device in SYS over-voltage protection	N/A
D[5]	OTG_OVP_STAT	0	R	OTG Over-Voltage Status 0 = Normal (default) 1 = Device in OTG over-voltage	N/A
D[4]	OTG_UVP_STAT	0	R	OTG Under-Voltage Status 0 = Normal (default) 1 = Device in OTG under-voltage	N/A
D[3]	Reserved	0	R	Reserved.	N/A
D[2]	TSHUT_STAT	0	R	IC Temperature Shutdown Status 0 = Normal (default) 1 = Device in thermal shutdown protection	N/A
D[1:0]	Reserved	00	R	Reserved.	N/A

REGISTER MAPS (continued)

REG0x22: Charger_Flag_0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IINDPM_FLAG	0	RC	IINDPM/IOTG Flag 0 = Normal (default) 1 = IINDPM/IOTG signal rising edge is detected	N/A
D[6]	VINDPM_FLAG	0	RC	VINDPM/VOTG Flag 0 = Normal (default) 1 = VINDPM/VOTG regulation signal rising edge is detected	N/A
D[5]	WD_FLAG	0	RC	I²C Watchdog Timer Flag 0 = Normal (default) 1 = WD timer signal rising edge is detected	N/A
D[4]	POORSRC_FLAG	0	RC	Poor Source Detection Flag 0 = Normal (default) 1 = Poor source status rising edge is detected	N/A
D[3]	PG_FLAG	0	RC	Power Good Flag 0 = Normal (default) 1 = Any change in PG_STAT even (adaptor good qualification or adaptor good going away)	N/A
D[2]	AC2_PRESENT_FLAG	0	RC	VAC2 Present Flag 0 = Normal (default) 1 = VAC2 present status is changed	N/A
D[1]	AC1_PRESENT_FLAG	0	RC	VAC1 Present Flag 0 = Normal (default) 1 = VAC1 present status is changed	N/A
D[0]	VBUS_PRESENT_FLAG	0	RC	VBUS Present Flag 0 = Normal (default) 1 = VBUS present status is changed	N/A

REG0x23: Charger_Flag_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	CHG_FLAG	0	RC	Charge Status Flag 0 = Normal (default) 1 = Charge status is changed	N/A
D[6]	ICO_FLAG	0	RC	ICO Status Flag 0 = Normal (default) 1 = ICO status is changed	N/A
D[5]	Reserved	0	R	Reserved.	N/A
D[4]	VBUS_FLAG	0	RC	VBUS Status Flag 0 = Normal (default) 1 = VBUS status is changed	N/A
D[3]	Reserved	0	R	Reserved.	N/A
D[2]	TREG_FLAG	0	RC	IC Thermal Regulation Flag 0 = Normal (default) 1 = TREG signal rising threshold is detected	N/A
D[1]	VBAT_PRESENT_FLAG	0	RC	VBAT Present Flag 0 = Normal (default) 1 = VBAT present status is changed	N/A
D[0]	BC1.2_DONE_FLAG	0	RC	BC1.2 Status Flag 0 = Normal (default) 1 = BC1.2 detection status is changed	N/A

REGISTER MAPS (continued)

REG0x24: Charger_Flag_2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved.	N/A
D[6]	DPDM_DONE_FLAG	0	RC	D+/D- Detection is Done Flag 0 = D+/D- detection is not started or still ongoing (default) 1 = D+/D- detection is completed	N/A
D[5]	ADC_DONE_FLAG	0	RC	ADC Conversion Flag (Only in One-Shot Mode) 0 = Conversion is not completed (default) 1 = Conversion is completed	N/A
D[4]	VSYS_FLAG	0	RC	VSYSMIN Regulation Flag 0 = Normal (default) 1 = Enter or exit VSYSMIN regulation	N/A
D[3]	CHG_TMR_FLAG	0	RC	Fast Charge Timer Flag 0 = Normal (default) 1 = Fast charge timer expired rising edge is detected	N/A
D[2]	TRICHG_TMR_FLAG	0	RC	Trickle Charge Timer Flag 0 = Normal (default) 1 = Trickle charger timer expired rising edge is detected	N/A
D[1]	PRECHG_TMR_FLAG	0	RC	Pre-Charge Timer Flag 0 = Normal (default) 1 = Pre-charge timer expired rising edge is detected	N/A
D[0]	TOPOFF_TMR_FLAG	0	RC	Top-Off Timer Flag 0 = Normal (default) 1 = Top-off timer expired rising edge is detected	N/A

REG0x25: Charger_Flag_3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved.	N/A
D[4]	VBATOTG_LOW_FLAG	0	RC	VBAT Too Low to Enable OTG Flag 0 = Normal (default) 1 = VBAT falls below the threshold to enable the OTG mode	N/A
D[3]	TS_COLD_FLAG	0	RC	TS Cold Temperature Flag 0 = Normal (default) 1 = TS across cold temperature (T1) is detected	N/A
D[2]	TS_COOL_FLAG	0	RC	TS Cool Temperature Flag 0 = Normal (default) 1 = TS across cool temperature (T2) is detected	N/A
D[1]	TS_WARM_FLAG	0	RC	TS Warm Temperature Flag 0 = Normal (default) 1 = TS across warm temperature (T3) is detected	N/A
D[0]	TS_HOT_FLAG	0	RC	TS Hot Temperature Flag 0 = Normal (default) 1 = TS across hot temperature (T4) is detected	N/A

REGISTER MAPS (continued)

REG0x26: FAULT_Flag_0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBAT_REG_FLAG	0	RC	IBAT Regulation Flag 0 = Normal (default) 1 = Enter or exit IBAT regulation	N/A
D[6]	VBUS_OVP_FLAG	0	RC	VBUS Over-Voltage Flag 0 = Normal (default) 1 = Enter VBUS OVP	N/A
D[5]	VBAT_OVP_FLAG	0	RC	VBAT Over-Voltage Flag 0 = Normal (default) 1 = Enter VBAT OVP	N/A
D[4]	IBUS_OCP_FLAG	0	RC	IBUS Over-Current Flag 0 = Normal (default) 1 = Enter IBUS OCP	N/A
D[3]	IBAT_OCP_FLAG	0	RC	IBAT Over-Current Flag 0 = Normal (default) 1 = Enter discharged OCP	N/A
D[2]	CONV_OCP_FLAG	0	RC	Converter Over-Current Flag 0 = Normal (default) 1 = Enter converter OCP	N/A
D[1]	VAC2_OVP_FLAG	0	RC	VAC2 Over-Voltage Flag 0 = Normal (default) 1 = Enter VAC2 OVP	N/A
D[0]	VAC1_OVP_FLAG	0	RC	VAC1 Over-Voltage Flag 0 = Normal (default) 1 = Enter VAC1 OVP	N/A

REG0x27: FAULT_Flag_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VSYS_SHORT_FLAG	0	RC	VSYS Short-Circuit Flag 0 = Normal (default) 1 = Stop switching due to system short	N/A
D[6]	VSYS_OVP_FLAG	0	RC	VSYS Over-Voltage Flag 0 = Normal (default) 1 = Stop switching due to system over-voltage	N/A
D[5]	OTG_OVP_FLAG	0	RC	OTG Over-Voltage Flag 0 = Normal (default) 1 = Stop OTG due to VBUS over-voltage	N/A
D[4]	OTG_UVP_FLAG	0	RC	OTG Under-Voltage Flag 0 = Normal (default) 1 = Stop OTG due to VBUS under-voltage	N/A
D[3]	Reserved	0	R	Reserved.	N/A
D[2]	TSHUT_FLAG	0	RC	IC Thermal Shutdown Flag 0 = Normal (default 1 = TS shutdown signal rising threshold is detected	N/A
D[1:0]	Reserved	00	R	Reserved.	N/A

REGISTER MAPS (continued)

REG0x28: Charger_Mask_0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IINDPM_MASK	0	R/W	IINDPM/IOTG Mask Flag 0 = Enter IINDPM/IOTG produces nINT pulse (default) 1 = Enter IINDPM/IOTG does not produce nINT pulse	REG_RST
D[6]	VINDPM_MASK	0	R/W	VINDPM/VOTG Mask Flag 0 = Enter VINDPM/VOTG produces nINT pulse (default) 1 = Enter VINDPM/VOTG does not produce nINT pulse	REG_RST
D[5]	WD_MASK	0	R/W	I²C Watchdog Timer Mask Flag 0 = I²C watchdog timer expired produces nINT pulse (default) 1 = I²C watchdog timer expired does not produce nINT pulse	REG_RST
D[4]	POORSRC_MASK	0	R/W	Poor Source Detection Mask Flag 0 = Poor source detected produces nINT (default) 1 = Poor source detected does not produce nINT	REG_RST
D[3]	PG_MASK	0	R/W	Power Good Mask Flag 0 = PG toggle produces nINT (default) 1 = PG toggle does not produce nINT	REG_RST
D[2]	AC2_PRESENT_MASK	0	R/W	VAC2 Present Mask Flag 0 = VAC2 present status change produces nINT (default) 1 = VAC2 present status change does not produce nINT	REG_RST
D[1]	AC1_PRESENT_MASK	0	R/W	VAC2 Present Mask Flag 0 = VAC2 present status change produces nINT (default) 1 = VAC2 present status change does not produce nINT	REG_RST
D[0]	VBUS_PRESENT_MASK	0	R/W	VBUS Present Mask Flag 0 = VBUS present status change produces nINT (default) 1 = VBUS present status change does not produce nINT	REG_RST

REG0x29: Charger_Mask_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	CHG_MASK	0	R/W	Charge Status Mask Flag 0 = Charging status change produces nINT (default) 1 = Charging status change does not produce nINT	REG_RST
D[6]	ICO_MASK	0	R/W	ICO Status Mask Flag 0 = ICO status change produces nINT (default) 1 = ICO status change does not produce nINT	REG_RST
D[5]	Reserved	0	R	Reserved.	N/A
D[4]	VBUS_MASK	0	R/W	VBUS Status Mask Flag 0 = VBUS status change produces nINT (default) 1 = VBUS status change does not produce nINT	REG_RST
D[3]	Reserved	0	R	Reserved.	N/A
D[2]	TREG_MASK	0	R/W	IC Thermal Regulation Mask Flag 0 = Entering TREG produces nINT (default) 1 = Entering TREG does not produce nINT	REG_RST
D[1]	VBAT_PRESENT_MASK	0	R/W	VBAT Present Mask Flag 0 = VBAT present status change produces nINT (default) 1 = VBAT present status change does not produce nINT	REG_RST
D[0]	BC1.2_DONE_MASK	0	R/W	BC1.2 Status Mask Flag 0 = BC1.2 status change produces nINT (default) 1 = BC1.2 status change does not produce nINT	REG_RST

REGISTER MAPS (continued)

REG0x2A: Charger_Mask_2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved.	N/A
D[6]	DPDM_DONE_MASK	0	R/W	D+/D- Detection is Done Mask Flag 0 = D+/D- detection done produces nINT pulse (default) 1 = D+/D- detection done does not produce nINT pulse	REG_RST
D[5]	ADC_DONE_MASK	0	R/W	ADC Conversion Mask Flag (Only in One-Shot Mode) 0 = ADC conversion done produces nINT pulse (default) 1 = ADC conversion done does not produce nINT pulse	REG_RST
D[4]	VSYS_MASK	0	R/W	VSYS Min Regulation Mask Flag 0 = Enter or exit VSYSMIN regulation produces nINT pulse (default) 1 = Enter or exit VSYSMIN regulation does not produce nINT pulse	REG_RST
D[3]	CHG_TMR_MASK	0	R/W	Fast Charge Timer Mask Flag 0 = Fast charge timer expire produces nINT (default) 1 = Fast charge timer expire does not produce nINT	REG_RST
D[2]	TRICHG_TMR_MASK	0	R/W	Trickle Charge Timer Mask Flag 0 = Trickle charge timer expire produces nINT (default) 1 = Trickle charge timer expire does not produce nINT	REG_RST
D[1]	PRECHG_TMR_MASK	0	R/W	Pre-Charge Timer Mask Flag 0 = Pre-charge timer expire produces nINT (default) 1 = Pre-charge timer expire does not produce nINT	REG_RST
D[0]	TOPOFF_TMR_MASK	0	R/W	Top-Off Timer Mask Flag 0 = Top-off timer expire produces nINT (default) 1 = Top-off timer expire does not produce nINT	REG_RST

REG0x2B: Charger_Mask_3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved.	N/A
D[4]	VBATOTG_LOW_MASK	0	R/W	VBAT Too Low to Enable OTG Mask 0 = VBAT falling below the threshold to enable the OTG mode, produces nINT (default) 1 = VBAT falling below the threshold to enable the OTG mode, does not produce nINT	REG_RST or Watchdog
D[3]	TS_COLD_MASK	0	R/W	TS Cold Temperature Interrupt Mask 0 = TS across cold temperature (T1) produces nINT (default) 1 = TS across cold temperature (T1) does not produce nINT	REG_RST or Watchdog
D[2]	TS_COOL_MASK	0	R/W	TS Cool Temperature Interrupt Mask 0 = TS across cool temperature (T2) produces nINT (default) 1 = TS across cool temperature (T2) does not produce nINT	REG_RST or Watchdog
D[1]	TS_WARM_MASK	0	R/W	TS Warm Temperature Interrupt Mask 0 = TS across warm temperature (T3) produces nINT (default) 1 = TS across warm temperature (T3) does not produce nINT	REG_RST or Watchdog
D[0]	TS_HOT_MASK	0	R/W	TS Hot Temperature Interrupt Mask 0 = TS across hot temperature (T4) produces nINT (default) 1 = TS across hot temperature (T4) does not produce nINT	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x2C: FAULT_Mask_0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBAT_REG_MASK	0	R/W	IBAT Regulation Mask Flag 0 = Entering or exiting IBAT regulation produces nINT (default) 1 = Entering or exiting IBAT regulation does not produce nINT	REG_RST
D[6]	VBUS_OVP_MASK	0	R/W	VBUS Over-Voltage Mask Flag 0 = Entering VBUS OVP produces nINT (default) 1 = Entering VBUS OVP does not produce nINT	REG_RST
D[5]	VBAT_OVP_MASK	0	R/W	VBAT Over-Voltage Mask Flag 0 = Entering VBAT OVP produces nINT (default) 1 = Entering VBAT OVP does not produce nINT	REG_RST
D[4]	IBUS_OCP_MASK	0	R/W	IBUS Over-Current Mask Flag 0 = IBUS OCP fault produces nINT (default) 1 = IBUS OCP fault does not produce nINT	REG_RST
D[3]	IBAT_OCP_MASK	0	R/W	IBAT Over-Current Mask Flag 0 = IBAT OCP fault produces nINT (default) 1 = IBAT OCP fault does not produce nINT	REG_RST
D[2]	CONV_OCP_MASK	0	R/W	Converter Over-Current Mask Flag 0 = Converter OCP fault produces nINT (default) 1 = Converter OCP fault does not produce nINT	REG_RST
D[1]	VAC2_OVP_MASK	0	R/W	VAC2 Over-Voltage Mask Flag 0 = Entering VAC2 OVP produces nINT (default) 1 = Entering VAC2 OVP does not produce nINT	REG_RST
D[0]	VAC1_OVP_MASK	0	R/W	VAC1 Over-Voltage Mask Flag 0 = Entering VAC1 OVP produces nINT (default) 1 = Entering VAC1 OVP does not produce nINT	REG_RST

REG0x2D: FAULT_Mask_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VSYS_SHORT_MASK	0	R/W	VSYS Short-Circuit Mask Flag 0 = System short fault produces nINT (default) 1 = System short fault does not produce nINT	REG_RST
D[6]	VSYS_OVP_MASK	0	R/W	VSYS Over-Voltage Mask Flag 0 = System over-voltage fault produces nINT (default) 1 = System over-voltage fault does not produce nINT	REG_RST
D[5]	OTG_OVP_MASK	0	R/W	OTG Over-Voltage Mask Flag 0 = OTG VBUS over-voltage fault produces nINT (default) 1 = OTG VBUS over-voltage fault does not produce nINT	REG_RST
D[4]	OTG_UVP_MASK	0	R/W	OTG Under-Voltage Mask Flag 0 = OTG VBUS under-voltage fault produces nINT (default) 1 = OTG VBUS under-voltage fault does not produce nINT	REG_RST
D[3]	Reserved	0	R	Reserved.	N/A
D[2]	TSHUT_MASK	0	R/W	IC Thermal Shutdown Mask Flag 0 = TSHUT produces nINT (default) 1 = TSHUT does not produce nINT	REG_RST
D[1:0]	Reserved	00	R	Reserved.	N/A

REGISTER MAPS (continued)

REG0x2E: ADC_Control Register [Reset = 0x30]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_ADC	0	R/W	ADC Control 0 = Disable (default) 1 = Enable	REG_RST or Watchdog
D[6]	ADC_RATE	0	R/W	ADC Conversion Rate Control 0 = Continuous conversion (default) 1 = One-shot conversion	REG_RST
D[5:4]	ADC_SAMPLE[1:0]	11	R/W	ADC Sample Speed 00 = 15-bit effective resolution 01 = 14-bit effective resolution 10 = 13-bit effective resolution 11 = 12-bit effective resolution (default)	REG_RST
D[3]	ADC_AVG	0	R/W	ADC Average Control 0 = Single value (default) 1 = Run average	REG_RST
D[2]	ADC_AVG_INIT	0	R/W	ADC Average Initial Value Control 0 = Start average using the existing register value (default) 1 = Start average using a new ADC conversion	REG_RST
D[1:0]	Reserved	00	R	Reserved.	N/A

REG0x2F: ADC_Function_Disable_0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBUS_ADC_DIS	0	R/W	IBUS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[6]	IBAT_ADC_DIS	0	R/W	IBAT ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[5]	VBUS_ADC_DIS	0	R/W	VBUS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[4]	VBAT_ADC_DIS	0	R/W	VBAT ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[3]	VSYS_ADC_DIS	0	R/W	VSYS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[2]	TS_ADC_DIS	0	R/W	TS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[1]	TDIE_ADC_DIS	0	R/W	TDIE ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[0]	Reserved	0	R	Reserved.	N/A

REGISTER MAPS (continued)

REG0x30: ADC_Function_Disable_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DP_ADC_DIS	0	R/W	D+ ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[6]	DM_ADC_DIS	0	R/W	D- ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[5]	VAC2_ADC_DIS	0	R/W	VAC2 ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[4]	VAC1_ADC_DIS	0	R/W	VAC1 ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[3:0]	Reserved	0000	R	Reserved.	N/A

REG0x31: IBUS_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15]	IBUS_POL	0	R	Polarity of IBUS 0 = Positive (IBUS flow into VBUS pin) (default) 1 = Negative (IBUS flow out of VBUS pin)	N/A
D[14:0]	IBUS_ADC[14:0]	000 0000 0000 0000	R	15-Bit ADC IBUS Data (1mA Resolution) D[15:0] overall results are reported in two's complement. LSB<12:0>: 4096mA, 2048mA, 1024mA, 512mA, 256mA, 128mA, 64mA, 32mA,16mA, 8mA, 4mA, 2mA, 1mA	N/A

REG0x33: IBAT_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15]	IBAT_POL	0	R	Polarity of IBAT 0 = Positive (battery charge) (default) 1 = Negative (battery discharge)	N/A
D[14:0]	IBAT_ADC[14:0]	000 0000 0000 0000	R	15-Bit ADC IBAT Data (1mA Resolution) D[15:0] overall results are reported in two's complement. LSB<12:0>: 4096mA, 2048mA, 1024mA, 512mA, 256mA, 128mA, 64mA, 32mA,16mA, 8mA, 4mA, 2mA, 1mA	N/A

REG0x35: VBUS_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:0]	VBUS_ADC[15:0]	0000 0000 0000 0000	R	16-Bit ADC VBUS Data (1mV Resolution) LSB<14:0>: 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV	N/A

REG0x37: VAC1_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:0]	VAC1_ADC[15:0]	0000 0000 0000 0000	R	16-Bit ADC VAC1 Data (1mV Resolution) LSB<14:0>: 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV	N/A

REGISTER MAPS (continued)

REG0x39: VAC2_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:0]	VAC2_ADC[15:0]	0000 0000 0000 0000	R	16-Bit ADC VAC2 Data (1mV Resolution) LSB<14:0>: 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV	N/A

REG0x3B: VBAT_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:0]	VBAT_ADC[15:0]	0000 0000 0000 0000	R	The Battery Differential Sensing Voltage (VBATP) ADC Data (1mV Resolution) LSB<14:0>: 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV	N/A

REG0x3D: VSYS_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:0]	VSYS_ADC[15:0]	0000 0000 0000 0000	R	16-Bit ADC VSYS Data (1mV Resolution) LSB<14:0>: 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV	N/A

REG0x3F: TS_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:0]	TS_ADC[15:0]	0000 0000 0000 0000	R	TS ADC Reading (0.0976563% Resolution) Default: 0% (0h) Range: 0% - 99.9023% Fixed offset: 0% Bit step size: 0.0976563%	N/A

REG0x41: TDIE_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15]	TDIE_POL	0	R	Polarity of TDIE 0 = Positive (default) 1 = Negative	N/A
D[14:0]	TDIE_ADC[14:0]	000 0000 0000 0000	R	15-Bit TDIE ADC Data (0.5℃ Resolution) D[15:0] overall results are reported in two's complement. LSB<8:0>: 128℃, 64℃, 32℃, 16℃, 8℃, 4℃, 2℃, 1℃, 0.5℃	N/A

REGISTER MAPS (continued)

REG0x43: DP_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:0]	DP_ADC[15:0]	0000 0000 0000 0000	R	D+ ADC Data LSB<11:0>: 2048mV, 1024mV, 512mV, 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV	N/A

REG0x45: DM_ADC Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[15:0]	DM_ADC[15:0]	0000 0000 0000 0000	R	D- ADC Data LSB<11:0>: 2048mV, 1024mV, 512mV, 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV	N/A

REG0x47: DPDM_Driver Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	DPLUS_DAC[2:0]	000	R/W	D+ Output Driver 000 = HIZ (default) 001 = 0V 010 = 0.6V 011 = 1.2V 100 = 2.0V 101 = 2.7V 110 = 3.3V 111 = Short D+ to D- Note: If the customized adaptor interface specification is not used, it is recommended to keep the DPLUS_DAC[2:0] and DMIMUS_DAC[2:0] bits to HIZ (000) for power saving.	–
D[4:2]	DMINUS_DAC[2:0]	000	R/W	D- Output Driver 000 = HIZ (default) 001 = 0V 010 = 0.6V 011 = 1.2V 100 = 2.0V 101 = 2.7V 110 = 3.3V 111 = Reserved Note: If the customized adaptor interface specification is not used, it is recommended to keep the DPLUS_DAC[2:0] and DMIMUS_DAC[2:0] bits to HIZ (000) for power saving.	–
D[1:0]	Reserved	00	R	Reserved.	N/A

REG0x48: Part_Information Register [Reset = 0x21]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved.	N/A
D[5:3]	PN[2:0]	100	R	Device Part Number 100 = SGM41574 All the other options are reserved.	N/A
D[2:0]	DEV_REV[2:0]	001	R	Device Revision	N/A

APPLICATION INFORMATION

The SGM41574 is typically used as a charger with power path management in smart phones, tablets and other portable devices. In the design, it comes along with a host controller (a processor with I²C interface) and a 1-4 cells Li-Ion or Li-polymer battery.

Detailed Design Procedure

Inductor Selection

The SGM41574 provides 750kHz and 1.5MHz frequency operation to save the solution size. The frequency is configured at POR by PROG pin resistance. It is also programmable during normal operation. For better performance, the 2.2μH inductor is recommended for 750kHz operation and the 1μH inductor is recommended for 1.5MHz operation.

The Inductor selection should consider both the Buck operation and Boost operation.

For the Buck mode operation:

$$I_{PK_BUCK} = I_{OUT} + \frac{I_{RIPPLE_BUCK}}{2} \quad (3)$$

$$I_{RIPPLE_BUCK} = \frac{V_{SYS} \times (V_{VBUS} - V_{SYS})}{V_{VBUS} \times f_{SW} \times L} \quad (4)$$

For the Boost mode operation:

$$I_{PK_BOOST} = I_{IN} + \frac{I_{RIPPLE_BOOST}}{2} \quad (5)$$

$$I_{RIPPLE_BOOST} = \frac{V_{VBUS} \times (V_{SYS} - V_{VBUS})}{V_{SYS} \times f_{SW} \times L} \quad (6)$$

It is recommended to choose the inductor with both I_{RIPPLE_BUCK} and I_{RIPPLE_BOOST} within 20% - 40% of the maximum output or input current. And the inductor saturation current I_{SAT} should be higher than the larger value of I_{PK_BUCK} and I_{PK_BOOST}.

Input (VBUS/PMID) Capacitor

The input capacitor selection should consider both the Buck operation and Boost operation.

For the Buck mode operation, select low ESR ceramic input capacitor (X7R or X5R) with sufficient voltage and RMS ripple current rating for decoupling of the input switching ripple current (I_{CIN}). The RMS ripple current in the worst case is around the I_{CHG}/2 when D ≈ 0.5. If the converter does not operate at D ≈ 50%, the worst case capacitor RMS current can be estimated from equation (7) in which D is the closest operating duty cycle to 0.5.

$$I_{CIN_BUCK} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (7)$$

The input voltage ripple is calculated by equation (8):

$$\Delta V_{IN_BUCK} = \frac{D \times (1-D) \times I_{OUT}}{C_{IN} \times f_{SW}} \quad (8)$$

For the Boost mode operation, the effective capacitance of VBUS and PMID should be enough to absorb the VBUS input switching ripple current. The equation below shows the input capacitor RMS current I_{CIN} calculation.

$$I_{CIN_BOOST} = \frac{I_{RIPPLE_BOOST}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE_BOOST} \quad (9)$$

Low ESR ceramic capacitors are recommended for input capacitor. The input capacitor voltage ripple can be calculated as follow:

$$\Delta V_{IN_BOOST} = \frac{V_{IN}}{8 \times f_{SW}^2 \times L \times C_{IN}} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (10)$$

Considerations: a typical 10mΩ resistor is connected internally between VBUS and PMID pins for current sensing capability. In some applications (such as high-voltage adapter hot plug-in or surge test), VBUS/PMID voltage power-up/down rapidly. During this period, a transient high current flows through the resistor. Once the transient peak current exceeds 60A, the resistor risks damage, thereby affecting the current sensing accuracy. The transient current is proportional to the voltage change slew rate and the PMID effective capacitance. Therefore, the capacitor placed at PMID pin cannot be too large. It is recommended to connect only one 10μF/25V/0805 ceramic capacitor and one 0.1μF ceramic capacitor from PMID pin to GND close to the device.

Output (VSYS) Capacitor

The output capacitor selection should consider both the Buck operation and Boost operation.

In Buck mode operation, the output capacitance (on the system) must have enough RMS (ripple) current rating to carry the inductor switching ripple and provide enough energy for system transient current demands. I_{COUT} (C_{OUT} RMS current) can be calculated by:

$$I_{COUT} = \frac{I_{RIPPLE_BUCK}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE_BUCK} \quad (11)$$

And the output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (12)$$

APPLICATION INFORMATION (continued)

In the Boost mode operation, the output current is discontinuous and therefore requires an output capacitor to supply AC current to the load. Ripple current rating of output capacitor should be higher than the maximum output ripple. The output current ripple can be calculated by below equation and the maximum value occurs at 50% duty cycle.

$$I_{COUT} = I_{IN} \times \sqrt{D \times (1-D)} \quad (13)$$

For the best performance, low ESR ceramic capacitors are recommended. The output voltage ripple can be estimated as follow:

$$\Delta V_{SYS} = \frac{I_{OUT} \times D}{f_{SW} \times C_{OUT}} \quad (14)$$

SFET Selection

The SGM41574 supports ship mode, shutdown mode and system power reset feature by connecting an external N-channel MOSFET (SFET). Connect the gate of SFET to charger's SDRV pin, the source of SFET to BAT pin and the drain to the battery.

The differential voltage between SDRV and BAT pin is the SFET V_{GS} drive voltage. The differential voltage is 5V (TYP) for 2-4 cells battery application. For 1-cell battery application, the differential voltage may decrease to minimum 2.4V. To avoid excessive SFET $R_{DS(ON)}$ and too low BAT voltage (below V_{BAT_UVLO}), the MOSFET with $V_{GS(TH)_MAX}$ below 1.5V is recommended as SFET for 1-cell battery application.

Layout Guidelines

The switching node (SW) creates very high frequency noises, which are several times higher than switch frequency due to sharp rise and fall of the voltage and current in the switches. To reduce the ringing issues and noise generation, it is important to design a proper layout for minimizing the current path impedance and loop area. The following considerations can help to make a better layout.

1. Place the output capacitors as close as possible to SYS and BAT pins. The capacitors ground pins need to be connected to the IC ground with GND plane or short copper trace connections. A 0.1μF small size (such as 0402) capacitor is recommended to be placed closer than the other 10μF capacitors.

2. Place the input capacitor between PMID and GND pins as close as possible to the chip with the shortest copper connections (avoid via). Choose the smallest capacitor size. A 0.1μF small size (such as 0402) capacitor is recommended to be placed closer than the other 10μF capacitors.

3. Connect the inductor as close as possible to SW1 and SW2 pins. The trace should be short and wide to minimize the electrical and magnetic field radiation.

4. Place output capacitor GND pin as close as possible to the GND pin of the device and the GND pin of input capacitor C_{IN}. It is better to avoid using via for these connections and keep the high frequency current paths short enough and on the same layer. A GND copper layer under the component layer helps to reduce noise emissions. Note that the DC current and AC current paths are in the layout and keep them short and decoupled as much as possible.

5. For analog signals, it is better to use a separate analog ground (AGND) branched only at one point from GND pin. To avoid high current flow through the AGND path, it should be connected to GND only at one point (preferably the GND pin).

6. Place decoupling capacitors close to the IC pins with the shortest possible copper connections.

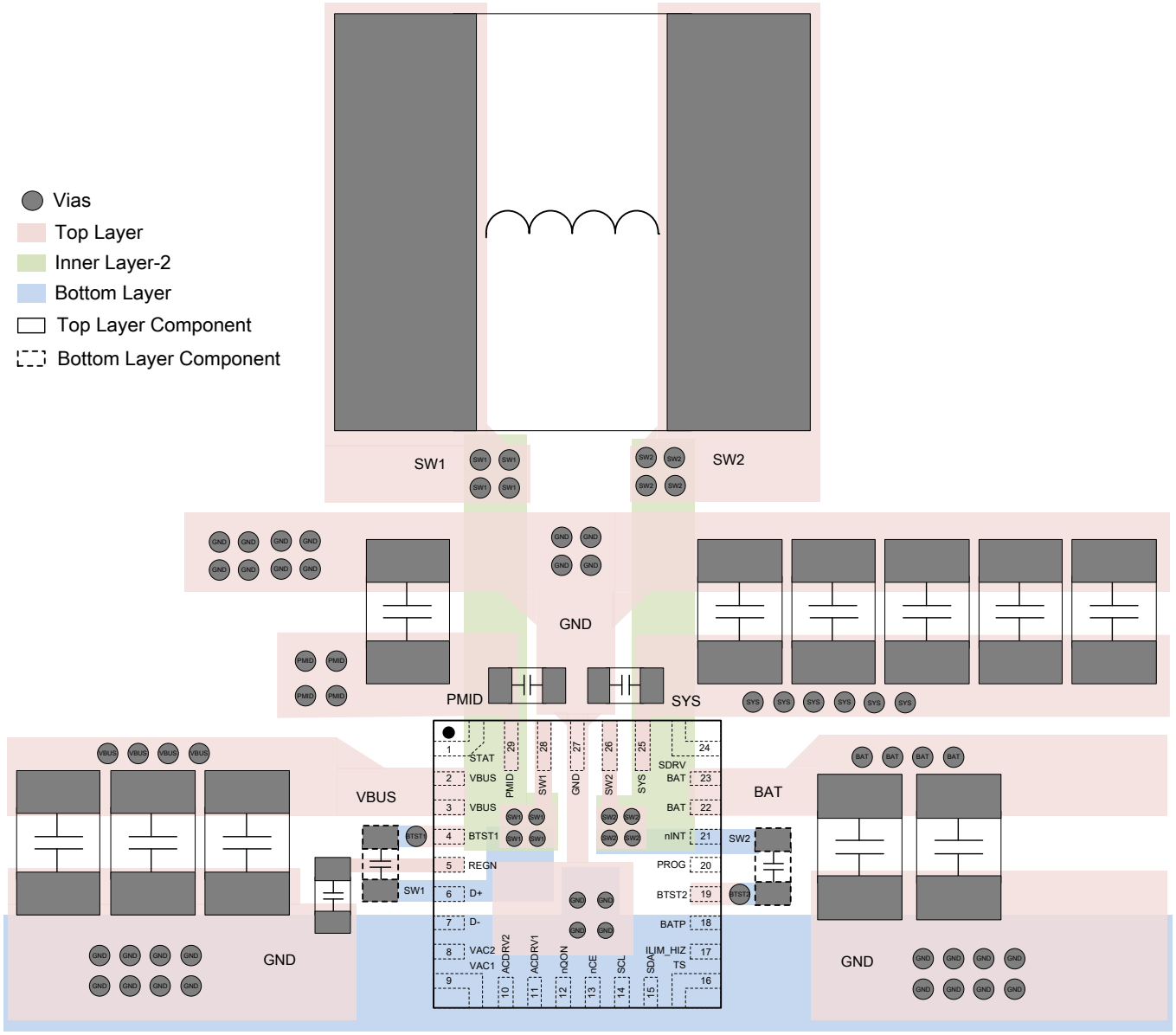
7. Place the BTST capacitors close to the IC with the shortest possible trace connections.

8. Solder the exposed thermal pad of the package to the PCB ground planes. Ensure that there are enough thermal vias directly under the IC, connecting to the ground plane on the other layers for better heat dissipation and cooling of the device.

9. Select proper sizes for the vias and ensure that enough copper is available to carry the current for the given current path. Vias usually have some considerable parasitic inductance and resistance.

10. Kelvin connects BATP pin to the positive and negative battery terminals respectively with 100Ω series resistor. Route the feedback signal BATP away from SW node.

APPLICATION INFORMATION (continued)



NOTES:

1. The layout example is actually a board with 4 layers. The inner layer-1 is a GND copper layer and not shown in the figure.

2. For ease of presentation, the BTST capacitors are placed at the bottom layer and on the side of the chip in the figure, but they can actually be placed directly beneath the chip on the bottom layer.

3. Only the critical circuit path layout is shown for reference, and other heat dissipation planes and vias are not shown in the figure. For more detailed information, please refer to the SGM41574 evaluation kit on www.sg-micro.com.

Figure 29. Layout Example

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JUNE 2026 – REV.A.2 to REV.A.3	Page
Updated Pin Description section	5
Updated Electrical Characteristics section	11
Updated Detailed Description section	27, 30, 34, 40
Updated Register Maps section	53, 55, 57, 58, 60, 67, 68, 69

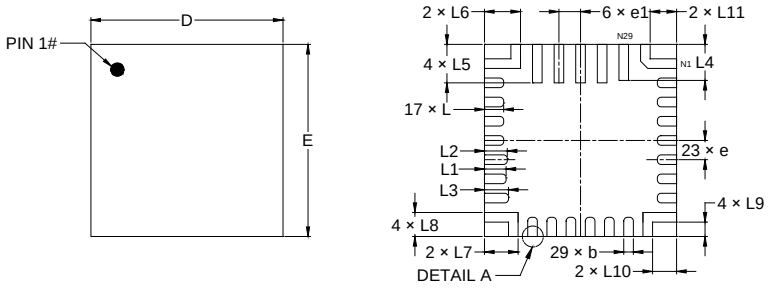
OCTOBER 2025 – REV.A.1 to REV.A.2	Page
Updated Pin Description section	4, 5
Updated Electrical Characteristics section	6
Updated Typical Application Circuits section	19, 20
Updated Functional Block Diagram section	21
Updated Detailed Description section	25, 38, 39, 47
Updated Application Information section	77, 78, 79

APRIL 2025 – REV.A to REV.A.1	Page
Updated Electrical Characteristics section	7, 10, 11
Updated Functional Block Diagram section	21

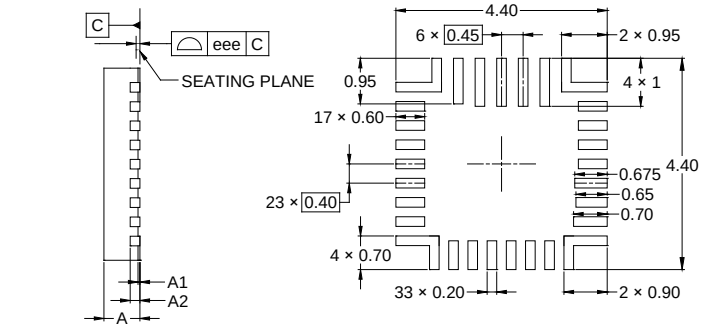
Changes from Original to REV.A (APRIL 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

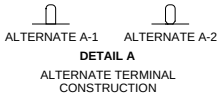
TQFN-4×4-29L



TOP VIEW **BOTTOM VIEW**



SIDE VIEW **RECOMMENDED LAND PATTERN** (Unit: mm)

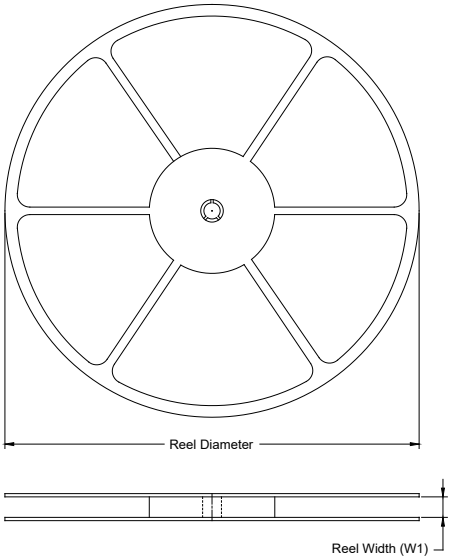


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.150	-	0.250
D	3.900	-	4.100
E	3.900	-	4.100
e		0.400 BSC	
e1		0.450 BSC	
L	0.300	-	0.500
L1	0.350	-	0.550
L2	0.375	-	0.575
L3	0.400	-	0.600
L4	0.650	-	0.850
L5	0.700	-	0.900
L6	0.650	-	0.850
L7	0.600	-	0.800
L8	0.400	-	0.600
L9		0.300 REF	
L10		0.500 REF	
L11		0.550 REF	
eee		0.080	

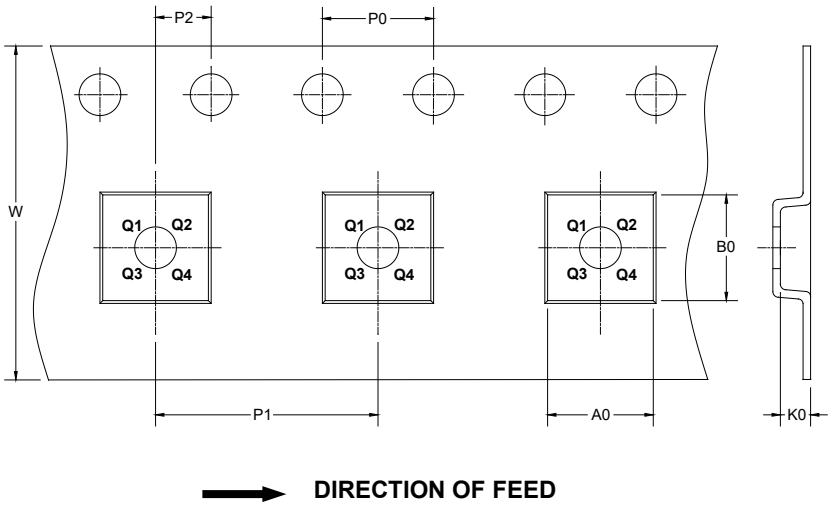
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



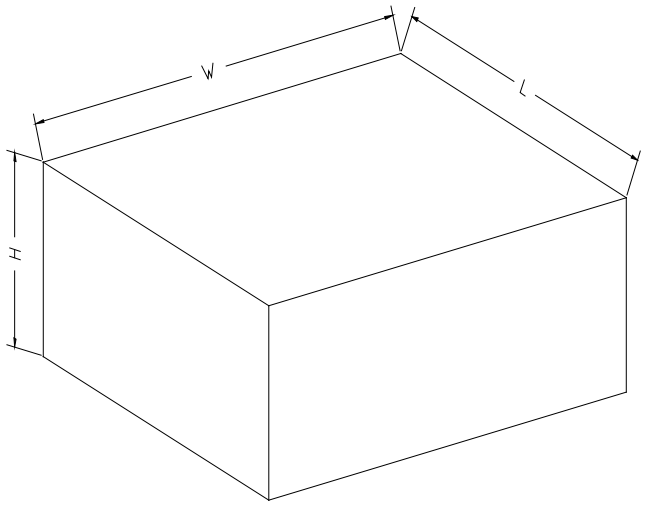
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-29L	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002