SGM41290
Bias and Monitoring Management Circuit

GENERAL DESCRIPTION

The SGM41290 is a highly-integrated bias and monitoring management circuit for silicon optical control applications. There are twelve channels of 12-bit programmable current/voltage output DACs with a maximum output current of 40mA and four channels of 12-bit 300mA high-current output DACs. The IC also has twelve MULTI_IO pins (MULTI_IOx) to monitor the current or DAC output signal. The functions of the twelve pins are configurable respectively through the I^2C interface or SPI.

The SGM41290 is available in a Green WLCSP-3.98×3.89-56B package. It operates over an ambient temperature range of -40℃ to +105℃.

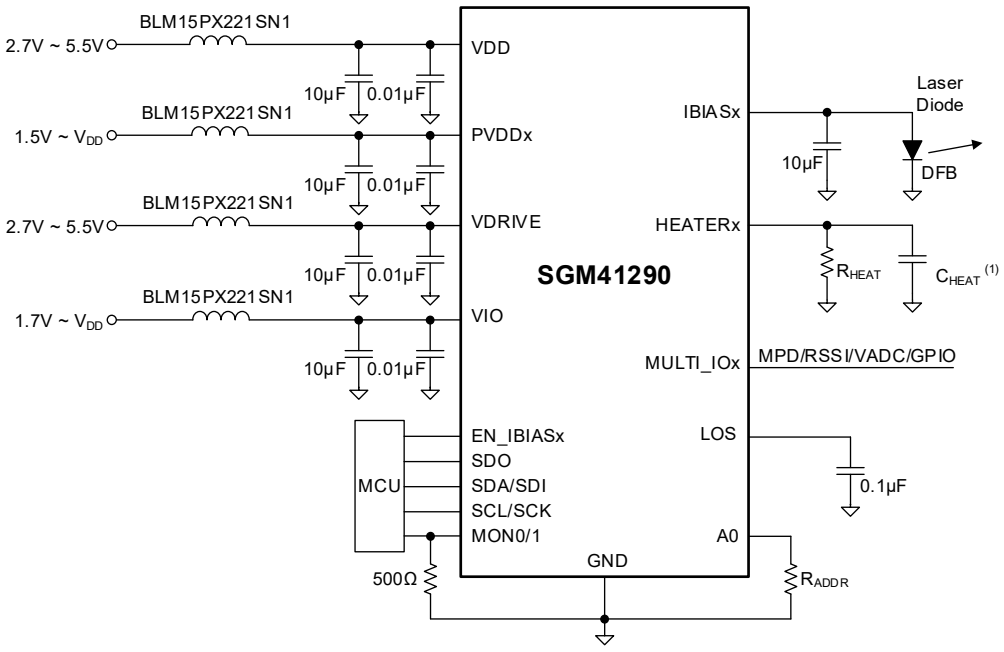
APPLICATIONS

Silicon Optical Control

FEATURES

- **Twelve Channels 12-bit VDAC/IDAC (HEATERx)**
  - **Supports Current and Voltage Output Modes**
  - **Voltage Mode: 0V to 2.5V/5V, Maximum 40mA Load Current**
  - **Current Mode: 0mA to 30mA**
  - **Power Supply (VDRIVE) : 2.7V to 5.5V**
- **Four Channels 12-bit 200mA/300mA IDAC (IBIAS)**
  - **Maximum Current: 200mA/300mA**
  - **EN_IBIASx Enable**
  - **EN_IBIASx Fast Turn-Off Control**
  - **Power Supply Range (PVDD): 1.5V to V_{DD}**
- **Twelve Channels Configurable MULTI_IOx**
  - **Support Current Monitoring**
  - **Support Voltage Monitoring**
  - **Support Digital General IO Function**
- **I^2C Interface Supports a Maximum of 1MHz**
- **SPI Interface Supports a Maximum of 10MHz**
- **Integrated Over-Temperature Alarm Function**
- **Available in a Green WLCSP-3.98×3.89-56B Package**

TYPICAL APPLICATION



NOTE 1: Capacitor in range of 100pF to 500pF is recommended for VDAC mode and in range of 0.1μF to 10μF is recommended for IDAC mode.

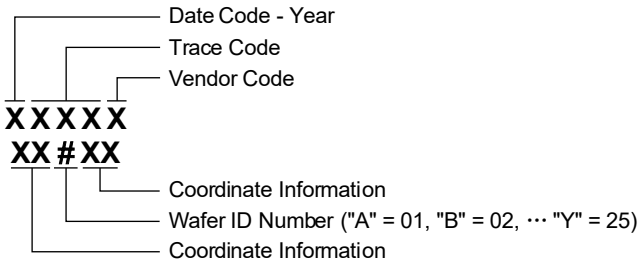
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41290	WLCSP-3.98×3.89-56B	-40℃ to +105℃	SGM41290GG/TR	SGM 41290 XXXXX XX#XX	Tape and Reel, 7000
	WLCSP-3.98×3.89-56B	-40℃ to +105℃	SGM41290GSG/TR	SGM 41290 XXXXX XX#XX	Tape and Reel, 1000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VDD, PVDDx, VDRIVE, VIO ..... -0.3V to 6V
IBIASx..... -0.3V to V_{PVDDx} + 0.3V
HEATERx .....-0.3V to V_{DRIVE} + 0.3V
MULTI_IOx, LOS, SDO..... -0.3V to V_{IO} + 0.3V
MONx.....-0.3V to V_{DD} + 0.3V
RSTN, EN_IBIASx, SCL, SDA, A0 ..... -0.3V to 6V
Package Thermal Resistance
WLCSP-3.98×3.89-56B, θ_{JA}..... 34.4℃/W
WLCSP-3.98×3.89-56B, θ_{JB}..... 10.2℃/W
WLCSP-3.98×3.89-56B, θ_{JC}..... 4.6℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (1) (2)
HBM.....±1500V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

VDD .....2.7V to 5.5V
PVDDx..... 1.5V to V_{DD}
VDRIVE.....2.7V to 5.5V
VIO .....1.7V to V_{DD}
Operating Ambient Temperature Range ..... -40℃ to +105℃
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

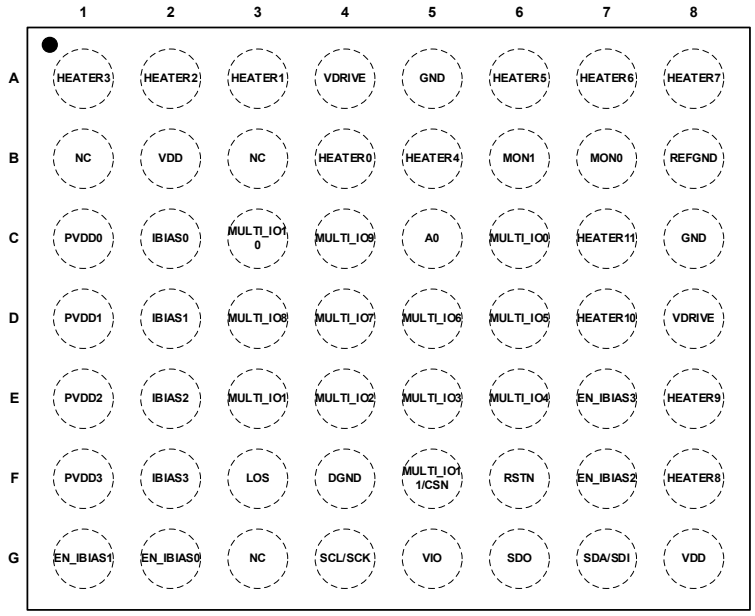
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-3.98×3.89-56B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1	HEATER3	AO	12-bit VDAC3/IDAC3 Output.
A2	HEATER2	AO	12-bit VDAC2/IDAC2 Output.
A3	HEATER1	AO	12-bit VDAC1/IDAC1 Output.
A4, D8	VDRIVE	P	Heater Power Supply.
A5, C8	GND	G	Ground.
A6	HEATER5	AO	12-bit VDAC5/IDAC5 Output.
A7	HEATER6	AO	12-bit VDAC6/IDAC6 Output.
A8	HEATER7	AO	12-bit VDAC7/IDAC7 Output.
B1, B3, G3	NC	—	No Connection.
B2	VDD	P	3.3V Power Supply.
B4	HEATER0	AO	12-bit VDAC0/IDAC0 Output.
B5	HEATER4	AO	12-bit VDAC4/IDAC4 Output.
B6	MON1	AO	Multiplexed Monitoring Output. Compliance voltage: 0V to 2.5V.
B7	MON0	AO	Multiplexed Monitoring Output. Compliance voltage: 0V to 2.5V.
B8	REFGND	G	Reference Ground. Connect to GND.
C1	PVDD0	P	200mA/300mA 12-bit IDAC0 Power Supply.
C2	IBIAS0	AO	200mA/300mA 12-bit IDAC0 Output.
C3	MULTI_IO10	I/O	Same as MULTI_IO0.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
C4	MULTI_IO9	I/O	Same as MULTI_IO0.
C5	A0	I	I^2C Address Pin/I^2C-SPI Selection.
C6	MULTI_IO0	I/O	Support Current Source Input, Current Sink Input, GPIO.
C7	HEATER11	AO	12-bit VDAC11/IDAC11 Output.
D1	PVDD1	P	200mA/300mA 12-bit IDAC1 Power Supply.
D2	IBIAS1	AO	200mA/300mA 12-bit IDAC1 Output.
D3	MULTI_IO8	I/O	Same as MULTI_IO0.
D4	MULTI_IO7	I/O	Same as MULTI_IO0.
D5	MULTI_IO6	I/O	Same as MULTI_IO0.
D6	MULTI_IO5	I/O	Same as MULTI_IO0.
D7	HEATER10	AO	12-bit VDAC10/IDAC10 Output.
E1	PVDD2	P	200mA/300mA 12-bit IDAC2 Power Supply.
E2	IBIAS2	AO	200mA/300mA 12-bit IDAC2 Output.
E3	MULTI_IO1	I/O	Same as MULTI_IO0.
E4	MULTI_IO2	I/O	Same as MULTI_IO0.
E5	MULTI_IO3	I/O	Same as MULTI_IO0.
E6	MULTI_IO4	I/O	Same as MULTI_IO0.
E7	EN_IBIAS3	I	IBIAS3 Enable Control.
E8	HEATER9	AO	12-bit VDAC9/IDAC9 Output.
F1	PVDD3	P	200mA/300mA 12-bit IDAC3 Power Supply.
F2	IBIAS3	AO	200mA/300mA 12-bit IDAC3 Output.
F3	LOS	O	Push-Pull Output. Fault Indication of Heater Current Source Open, Heater Voltage Output Short, IBIAS Open and Short and Over-Temperature Events.
F4	DGND	P	Digital Ground.
F5	MULTI_IO11/CSN	I/O	Same as MULTI_IO0/SPI Interface Chip Selection Signal.
F6	RSTN	I	Reset Pin. External reset, low effectiveness.
F7	EN_IBIAS2	I	IBIAS2 Enable Control.
F8	HEATER8	AO	12-bit VDAC8/IDAC8 Output.
G1	EN_IBIAS1	I	IBIAS1 Enable Control.
G2	EN_IBIAS0	I	IBIAS0 Enable Control.
G4	SCL/SCK	I	I^2C Clock/SPI Clock.
G5	VIO	P	IO Power Supply.
G6	SDO	O	SPI Data Output.
G7	SDA/SDI	I/O	I^2C Data Port /SPI Data Input.
G8	VDD	P	3.3V Power Supply.

NOTE: I: input, O: output, I/O: input or output, AO: analog output, G: ground, P: power for the circuit.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, V_{PVDD} = 1.8V, V_{DRIVE} = 3.3V, T_J = -40℃ to +105℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
VDD Under-Voltage Lockout Threshold	V_{UVLO_R}	V_{DD} rising	2.4	2.5	2.6	V
	V_{UVLO_F}	V_{DD} falling	2.3	2.38	2.5	V
Power-Up Blanking Time	t_{BLANK}			36		ms
IBIAS Current Source (12-Bit DAC)						
Output Current	I_{IBIAS}	IBIAS GAIN = 1	0		200	mA
		IBIAS GAIN = 1.5			300	mA
Resolution				12		Bit
PVDD Voltage			1.5		V_{DD}	V
Dropout Voltage		I_{BIAS} = 200mA × 95%, V_{IBIAS} = 1.55V		0.10	0.16	V
		I_{BIAS} = 300mA × 95%, V_{IBIAS} = 1.55V		0.16	0.25	V
IBIAS Accuracy		I_{BIAS} = 100mA, V_{IBIAS} = 1.55V	-2		2	%
Integral Nonlinearity		Code (1) = 100 - 4095 @+25℃		±3		LSB
Differential Nonlinearity		Code (1) = 100 - 4095 @+25℃	-1		1	LSB
IBIAS Noise	I_{NOISE}	V_{PVDD} = 1.6V, I_{BIAS} = 100mA, 10Hz to 10kHz		3.3		μA_{RMS}
IBIAS Full Temperature Drift	V_{IBIAS_DRIFT}	I_{BIAS} = 100mA		55		ppm/℃
Pull-Down Resistor	R_{PD}			6.5		Ω
IBias Open Detection Threshold		V_{PVDD}-V_{IBIAS} falling		60		mV
IBias short Detection Threshold		V_{IBIAS} falling		600		mV
Heater (12-Bit DAC)						
Current Output Mode						
VDRIVE Voltage Range			2.7		5.5	V
Resolution				12		Bit
Heater Current Source Full Scale Range			0		30	mA
Heater Voltage Tolerance			0		V_{DRIVE} - 0.2	V
Heater Current Source Accuracy		I_{HEATER} = 20mA	-2		2	%
Integral Nonlinearity		Code (1) = 100 - 4095 @+25℃		±3		LSB
Differential Nonlinearity		Code (1) = 100 - 4095 @+25℃	-1		1	LSB
Heater Noise		I_{HEATER} = 20mA		0.8		μA_{RMS}
Heater Full Temperature Drift		I_{HEATER} = 20mA		45		ppm/℃
Heater Current Source Open Detection Threshold		V_{DRV}-V_{HEATER} falling		45		mV
Voltage Output Mode						
VDRIVE Voltage Range		DAC normal operating voltage range	2.7		V_{DD}	V
VDAC Voltage Output Full Scale Range (12-Bit DAC)		VDAC gain = 1	0		2.5	V
		VDAC gain = 2 (2)	0		5	V
VDAC Voltage Sink or Source Current Over Full Scale Range					40	mA
Resolution				12		Bit
Integral Nonlinearity		Code (1) = 20 - 4095 @+25℃		±1		LSB
Differential Nonlinearity		Code (1) = 20 - 4095 @+25℃	-1		1	LSB
VDAC Voltage Accuracy		Code (1) = 4095 @ +25℃	-0.6		0.6	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, V_{PVDD} = 1.8V, V_{DRIVE} = 3.3V, T_J = -40℃ to +105℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VDAC Voltage Full Temperature Drift		T_J = -40℃ to +105℃		10		ppm/℃
VDAC Noise		V_{HEATER} = 2V		30		μV_{RMS}
VDAC Capacitive Load					500	pF
VDAC Output Short Current Detection Threshold				70		mA
MUTI_IO (3)						
Current Range			0		5	mA
Voltage Range (4)		Type A Source	V_{DD} - 1.4		V_{DD} - 0.3	V
		Type B Sink (1:32)	0.42		1.23	V
Monitor Output (MON)						
Current Accuracy		I_{MULTI_IOx} = 3mA	-3		3	%
		I_{MULTI_IOx} = 150μA (1:32)	-4		4	%
Current Temperature Drift		I_{MULTI_IOx} = 3mA		±0.1		%
		I_{MULTI_IOx} = 150μA (1:32)		±0.2		%
Current Noise		I_{MULTI_IOx} = 3mA		18		nA_{RMS}
Leakage Current		V_{MON} = 1V		10		nA
On-Resistance	R_{DS}	V_{MON} = 1V		25		Ω
Digital PIN Signals (RST_N, EN_IBIASX, SDA,SCL, MULTI_IOX)						
Input High Threshold			0.7 × V_{IO}			V
Input Low Threshold					0.3 × V_{IO}	V
Control Timing						
EN_IBIAS De-assert Time		EN_IBIAS de-assert to bias off		2		μs
EN_IBIAS Assert Time		EN_IBIAS assert to bias on at bias setting level		125		μs
Thermal Detection						
Thermal Alert Threshold				140		℃
Thermal Shutdown Threshold				160		℃
Thermal Shutdown Hysteresis				20		℃

NOTES:

1. Code is the value of HEATERx_MSB<<8+HEATERx_LSB.
2. V_{DRIVE} = 5.5V.
3. $V_{MULTI_IO} \leq V_{IO}$.
4. Guaranteed by design and simulation.

I²C INTERFACE TIMING CHARACTERISTICS (1) (2)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Standard mode	+25℃			100	kHz
		Fast mode	+25℃			400	kHz
		Fast mode plus	+25℃			1	MHz
LOW Period of the SCL Clock	t_{LOW}	Standard mode	+25℃	4.7			μs
		Fast mode	+25℃	1.3			μs
		Fast mode plus	+25℃	0.5			μs
HIGH Period of the SCL Clock	t_{HIGH}	Standard mode	+25℃	4.0			μs
		Fast mode	+25℃	600			ns
		Fast mode plus	+25℃	260			ns
Bus Free Time between a STOP and a START Conditions	t_{BUF}	Standard mode	+25℃	4.7			μs
		Fast mode	+25℃	1.3			μs
		Fast mode plus	+25℃	0.5			μs
Hold Time for a Repeated START Condition	$t_{hd;STA}$	Standard mode	+25℃	4.0			μs
		Fast mode	+25℃	600			ns
		Fast mode plus	+25℃	260			ns
Setup Time for a Repeated START Condition	$t_{su;STA}$	Standard mode	+25℃	4.7			μs
		Fast mode	+25℃	600			ns
		Fast mode plus	+25℃	260			ns
Data Setup Time	$t_{su;DAT}$	Standard mode	+25℃	250			ns
		Fast mode	+25℃	100			ns
		Fast mode plus	+25℃	50			ns
Data Hold Time	$t_{hd;DAT}$	Standard mode	+25℃	0.05		3.45	μs
		Fast mode	+25℃	0.05		0.9	μs
		Fast mode plus	+25℃	0		0.33	μs
Rise Time of SCL Signal	t_{RCL}	Standard mode	+25℃	$20 + 0.1C_B$		1000	ns
		Fast mode	+25℃	$20 + 0.1C_B$		300	ns
		Fast mode plus	+25℃	10		120	ns
Fall Time of SCL Signal	t_{FCL}	Standard mode	+25℃	$20 + 0.1C_B$		300	ns
		Fast mode	+25℃	$20 + 0.1C_B$		300	ns
		Fast mode plus	+25℃	10		120	ns
Rise Time of SDA Signal	t_{RDA}	Standard mode	+25℃	$20 + 0.1C_B$		1000	ns
		Fast mode	+25℃	$20 + 0.1C_B$		300	ns
		Fast mode plus	+25℃	10		120	ns
Fall Time of SDA Signal	t_{FDA}	Standard mode	+25℃	$20 + 0.1C_B$		300	ns
		Fast mode	+25℃	$20 + 0.1C_B$		300	ns
		Fast mode plus	+25℃	10		120	ns

I²C INTERFACE TIMING CHARACTERISTICS (1) (2) (continued)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Setup Time for STOP Condition	$t_{su;STO}$	Standard mode	+25℃	4.0			μs
		Fast mode	+25℃	600			ns
		Fast mode plus	+25℃	260			ns
Capacitive Load for SDA and SCL	C_B	Standard mode	+25℃			0.4	nF
		Fast mode	+25℃			0.2	
		Fast mode plus	+25℃			0.1	

NOTES:

1. Industry standard I²C timing characteristics according to I²C-Bus Specification. Not tested in production.
2. Once SDA keeps low for more than 2.5ms, the I²C timeout of SGM41290 will reset.

I²C INTERFACE TIMING DIAGRAM

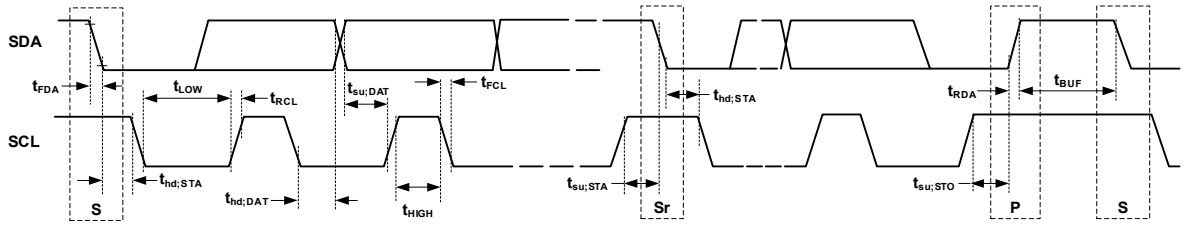


Figure 2. Serial Interface Timing for F/S-Mode

SPI TIMING CHARACTERISTICS

(V_{DD} = 3.3V, V_{PVDD} = 1.8V, V_{DRIVE} = 2.7V, T_J = -40℃ to +105℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
CSN Low Level to the First SCLK Setup Time	t_{CSSC}	6			ns
SCLK Cycle Time	t_{SCLK}	100			ns
SCLK High Time	t_{SPWH}	50			ns
SCLK Low Time	t_{SPWL}	50			ns
Data Setup Time	t_{DIST}	10			ns
Data Hold Time	t_{DIHD}	10			ns
CSN High Level Pulse	t_{CSH}	2			t_{SCLK}
Last SCLK falling Edge to the CSN High Level	t_{SCCS}	2			t_{SCLK}
Command Decoding Time	$t_{SDECODE}$	200			ns
Effective Setup Time from SCLK Rising Edge to DOUT	t_{DOPD}			34	ns
CSN Low Level to DOUT Drive	t_{CSDOD}			20	ns
CSN High Level to DOUT Hi-Z	t_{CSDOZ}			40	ns

SPI TIMING DIAGRAM

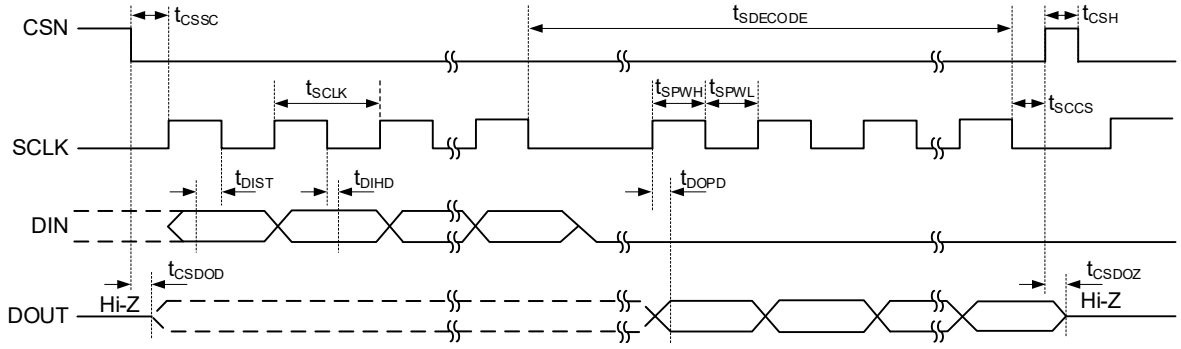
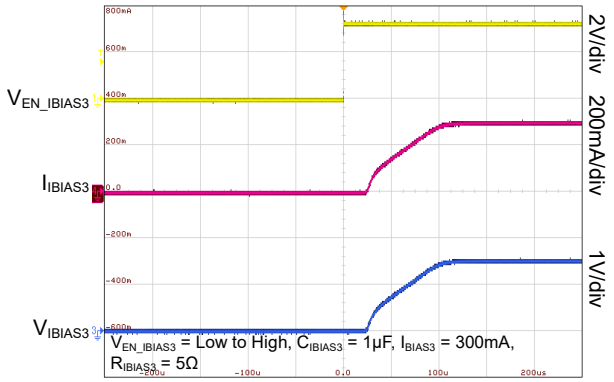


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

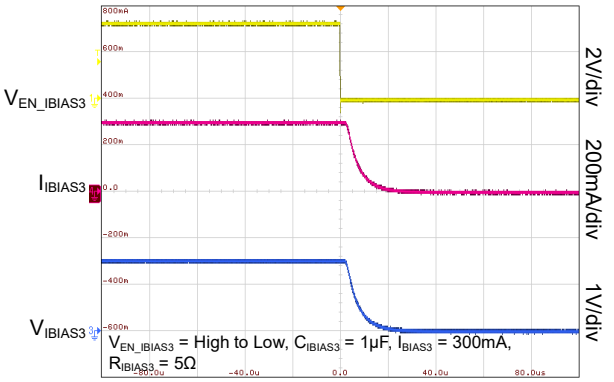
T_J = +25℃, V_{DD} = V_{DRIVE} = V_{IO} = 3.3V, V_{PVDD} = 1.8V, unless otherwise noted.

IBIAS Startup



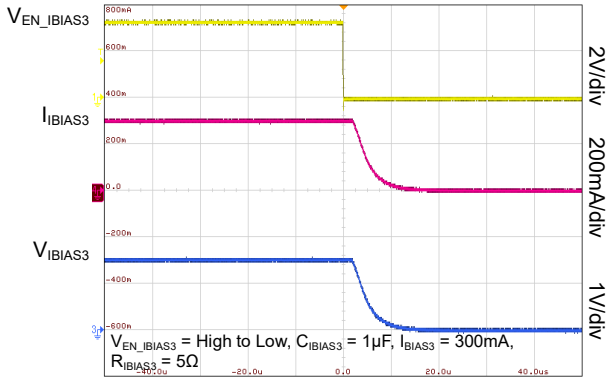
Time (50μs/div)

IBIAS Shutdown



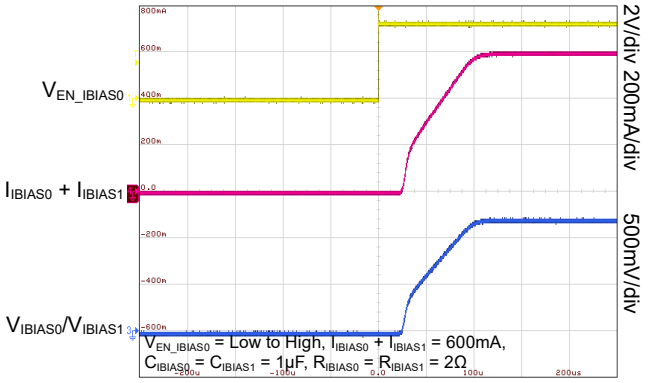
Time (20μs/div)

EN_IBIAS Fast Turn-Off



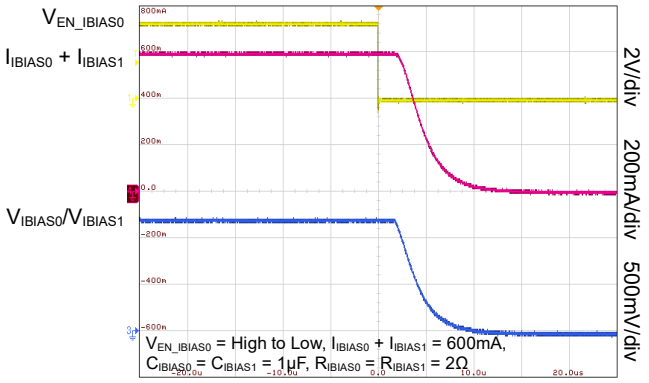
Time (10μs/div)

Shared EN_IBIAS Enable



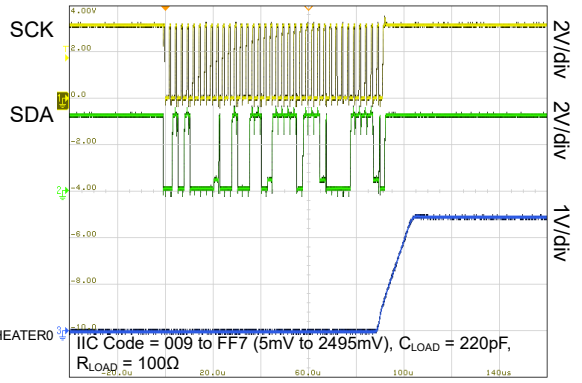
Time (50μs/div)

Shared EN_IBIAS Disable



Time (5μs/div)

VHEATER Ramp Up

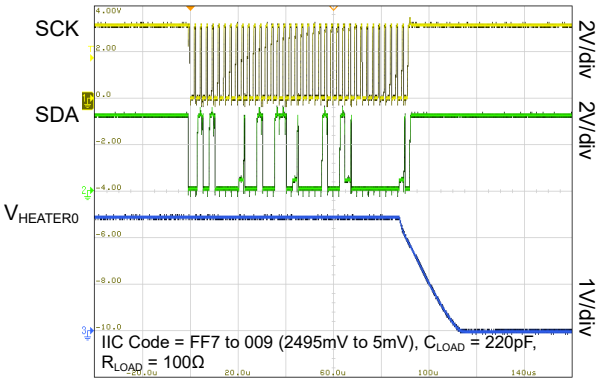


Time (20μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

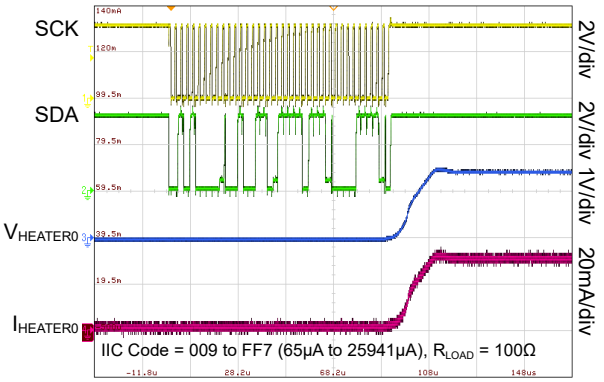
T_J = +25℃, V_{DD} = V_{DRIVE} = V_{IO} = 3.3V, V_{PVDD} = 1.8V, unless otherwise noted.

V_{HEATER} Ramp Down



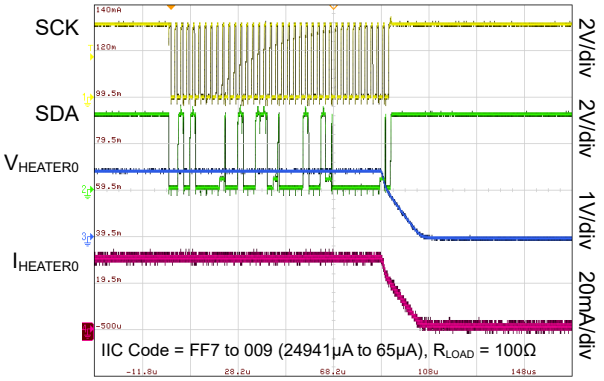
Time (20μs/div)

I_{HEATER} Ramp Up



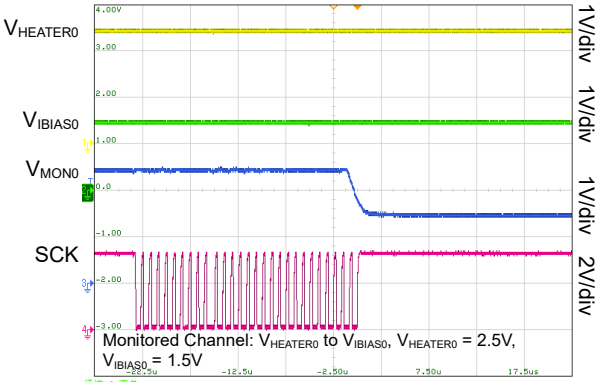
Time (20μs/div)

I_{HEATER} Ramp Down



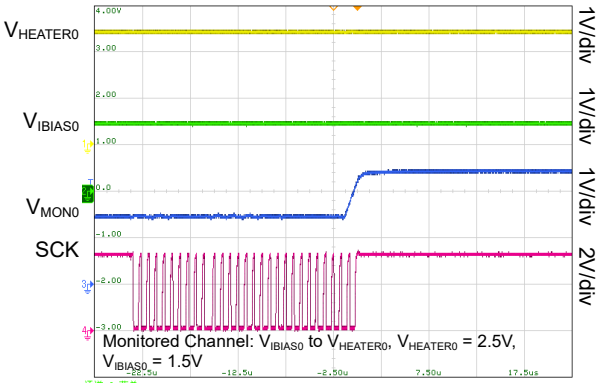
Time (20μs/div)

Internal Voltage Signal Polling Detection



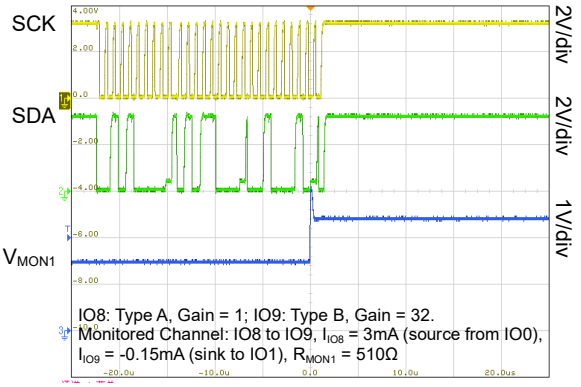
Time (5μs/div)

Internal Voltage Signal Polling Detection



Time (5μs/div)

Internal Current Signal Polling Detection

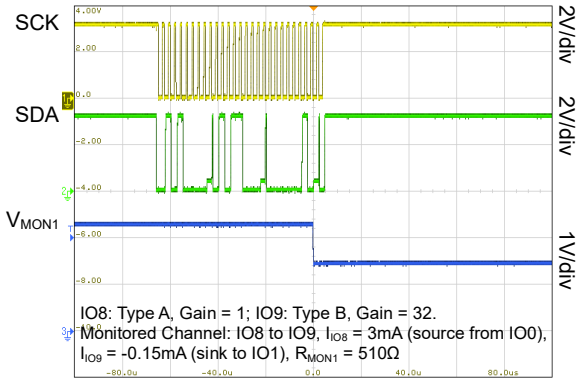


Time (5μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{DD} = V_{DRIVE} = V_{IO} = 3.3V, V_{PVDD} = 1.8V, unless otherwise noted.

Internal Current Signal Polling Detection



Time (20μs/div)

FUNCTIONAL BLOCK DIAGRAM

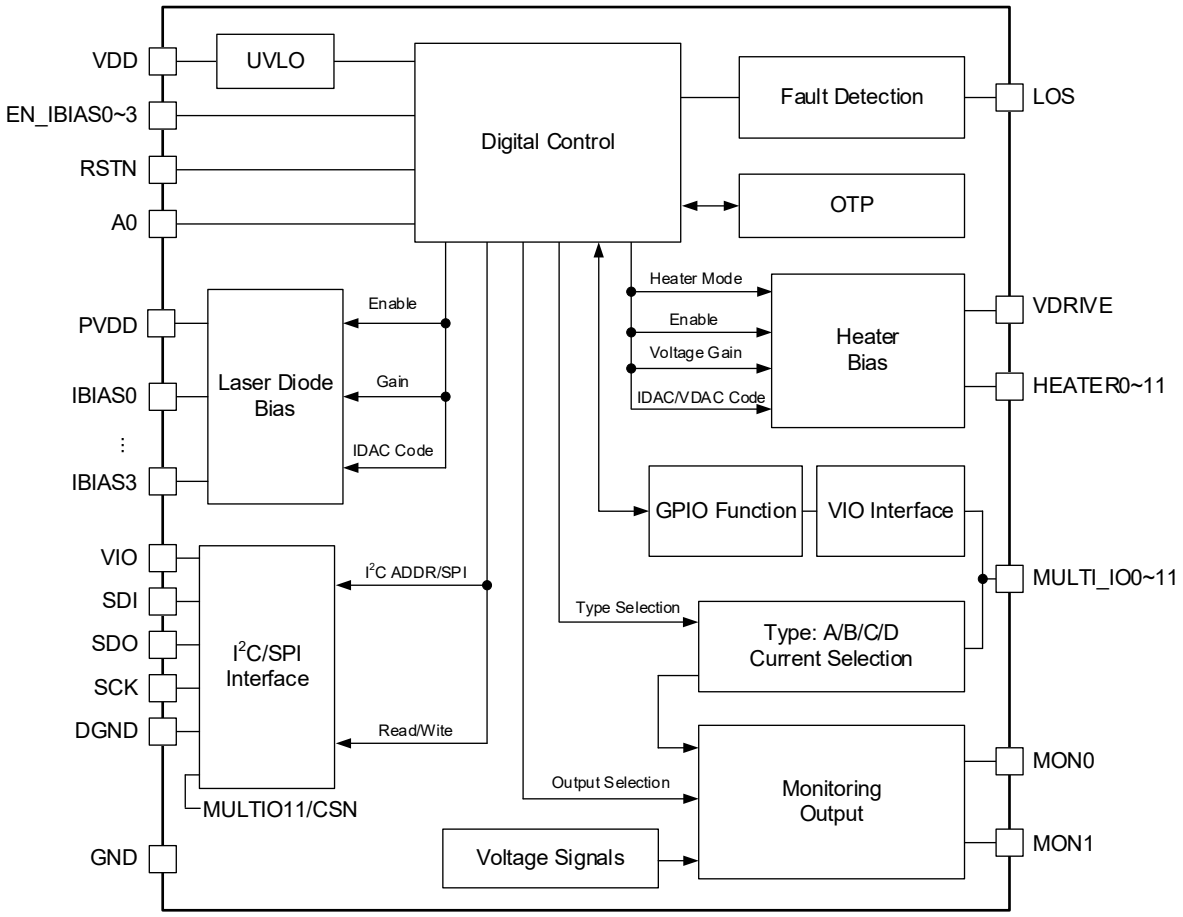


Figure 4. Block Diagram

DETAILED DESCRIPTION

HEATERx Pin Mode Configuration

The HEATERx pin has two modes: voltage DAC and current DAC (default). The output mode is configured by the register HEATER_MODE (0x24h). Heater0~11 is divided into three groups: Heater0~3, Heater4~7, and Heater8~11. Different groups can be configured to output current or voltage independently, and the same group can only be configured to the same output mode.

HEATERx Enable and Disable

To start a HEATER, the following two conditions should be met:

1. The VDD power supply must be above the voltage threshold for 36ms.
2. Software configuration HEATERx_EN = 1.

The 12 bit HEATERx data won't change even if the HEATERx is shut down by the software configuration.

Programming HEATER Current

The current in each channel is programmed independently with 12-bit DAC linear codes for current mode. The HEATERx current is calculated with the following equation:

$$Code = HEATERx_MSB \times 2^8 + HEATERx_LSB$$

where HEATERx_MSB, HEATERx_LSB and Code are all in decimal.

$$I_{HEATERx} = 30mA \times (Code/4095)$$

where Code is from 0 to 4095.

Programming HEATER Voltage

The voltage of each channel is programmed with 12-bit DAC linear codes for voltage mode. The HEATERx voltage is calculated with the following equation:

$$Code=HEATERx_MSB \times 2^8 + HEATERx_LSB$$

where HEATERx_MSB, HEATERx_LSB and Code are all in decimal.

$$V_{HEATERx} = k \times 2.5V \times (Code/4095)$$

where k is VDAC gain (1 or 2), and code is from 0 to 4095.

IBIASx Enable and Disable

To enable a 200mA/300mA IBIAS, the following conditions must be met:

1. The VDD power supply must be above voltage threshold.
2. The corresponding EN_BIASx pin is the logical high level.
3. Software configuration IBIASx_EN = 1.

The IBIAS current can be turned off if one of the above three conditions is not met. Among them, the software turns off the IBIAS and the data register remains the original value.

Programming IBIAS Current

The current is programmed independently with 12-bit DAC linear codes. The IBIASx current is calculated with the following equation:

$$Code = IBIASx_MSB \times 2^8 + IBIASx_LSB$$

where IBIASx_MSB, IBIASx_LSB and Code are all in decimal.

$$I_{BIASx} = k \times 200mA \times (Code/4095)$$

where k is current gain (1 or 1.5), and code is from 0 to 4095.

EN_IBIASx Fast Shutdown

Pull the EN_IBIASx pin low to quickly turn off the IBIAS current, and configure IBIASx_SW2GND = 1 (the default configuration after power cycle) to quickly drain the charge from the output pin. Each IBIAS current has its own EN_IBIASx pin. The IBIAS0/1 channel can also be controlled with EN_IBIAS0 through the configuration register SHARE_EN_IBIAS01 = 1. The register SHARE_EN_IBIAS23 = 1 is configured to control the IBIAS2/3 channel with EN_IBIAS2.

Alarm Function

1. Over-temperature alarm. Once the chip temperature exceeds 135℃, the OT_ALERT bit is set to 1. Otherwise, if OT_INT_EN = 1, the over-temperature fault interrupt is enabled. Note that only if LOS_EN = 1, the LOS pin can indicate the over-temperature fault interrupt.

2. Heater open/short alarm. Once Heater0~11 pin is open/short, the corresponding Heaterx_OPEN_FLAG or Heaterx_Short_FLAG bit is set to 1. Otherwise, if Heaterx_INT_EN = 1, the heater open/short fault interrupt is enabled. Note that only if LOS_EN = 1, the LOS pin can indicate the heater open/short fault interrupt.

DETAILED DESCRIPTION (continued)

3. IBIAS open/short alarm. Once IBIAS0~3 pin is open/short, the corresponding IBIASx_OPEN_FLAG or IBIASx_Short_FLAG bit is set to 1. Otherwise, if IBIASx_INT_EN = 1, the heater open/short fault interrupt is enabled. Note that only if LOS_EN = 1, the LOS pin can indicate the IBIAS open/short fault interrupt.

MULTI_IOx Pin Function

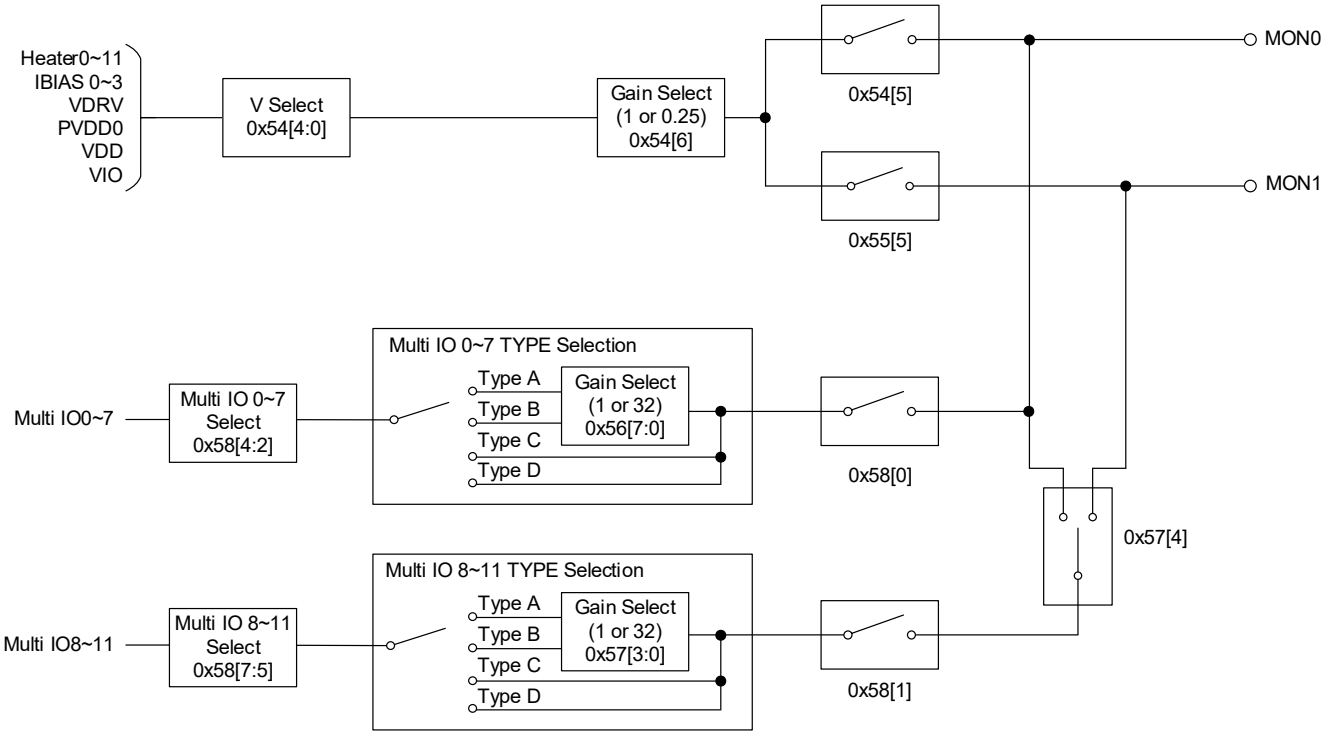


Figure 5. Channel Select of MON0/1 Logic Diagram

MULTI_IOx Pin Applications

There are 5 different applications which are programmed by I^2C interface for MULTI_IOx pin. Please refer to Figure 5 for more detail.

Type A: The input signal is a current sink, with the MPD anode grounded and the cathode connected to MULTI_IOx.

Type B: The input signal is a current source, with the MPD cathode connected to the power supply VDD and the anode connected to MULTI_IOx.

Type C: The input is a current source, which is directly connected to MON0/1 through a switch without passing through a current mirror.

Type D: Input the current source to an internal 500Ω resistor and send the MULTI_IOx voltage to MON0/1.

Type E: GPIO function.

For Type A and Type B, register MON_GAIN32 can be set to select a current mirror ratio of 1 or 32 for output. Each IO corresponds to an independent current source, solving the probability of negative pressure occurrence.

DETAILED DESCRIPTION (continued)

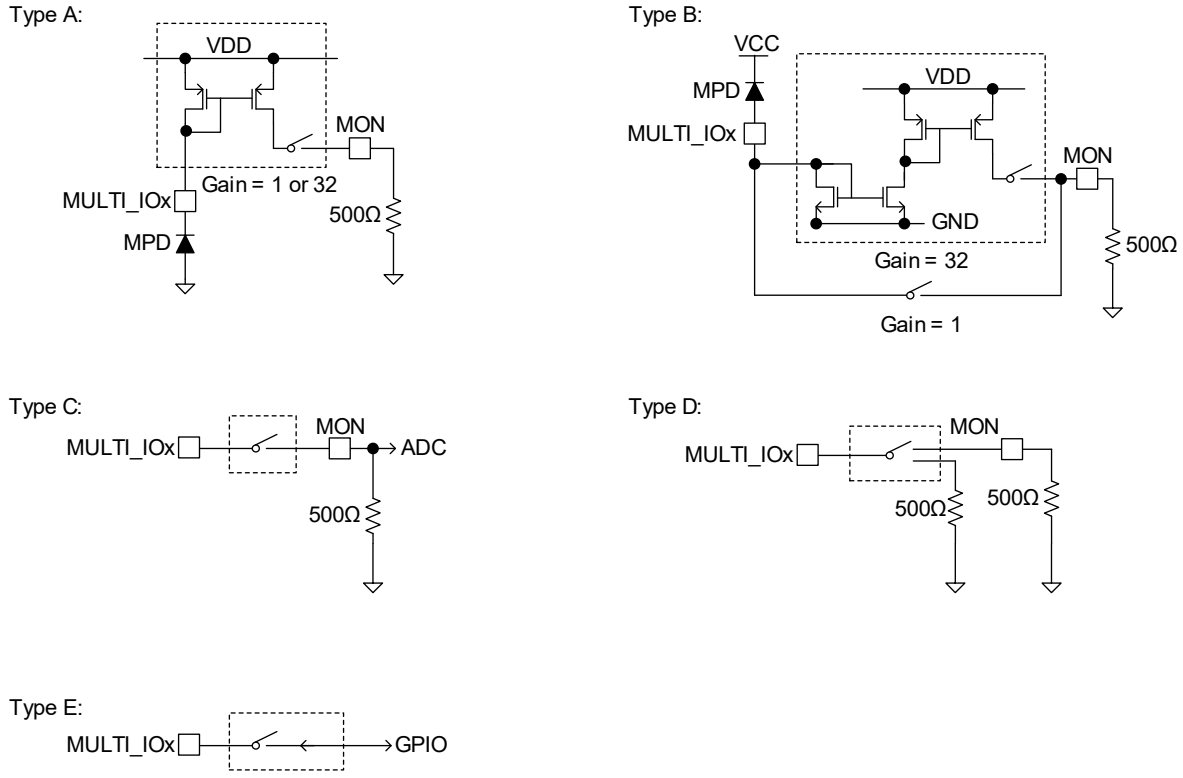


Figure 6. MULTI_IOx Pin Applications

For Type A~D, 12 channel outputs are sent to MON0 and MON1 through current testing channels. MULT-IO0~7 can only be sent to MON0 for measurement, and MULT-IO8~11 can be sent to either MON0 or MON1, which is set by register MON_CTRL (REG0x57) and MON_MSEL (REG0x58). Note that if Type B current mirror ratio of 1 is selected, the internal circuit of Type B is the same as Type C.

Voltage Monitor

Internal signals such as HEATERx/IBIASx output and power can also be sent to MON0 or MON1 for measurement. For detailed configuration, please refer to registers MON_VSEL0 and MON_VSEL1. A built-in voltage buffer is provided to improve drive capability, which can drive external minimum 500Ω resistance, and the buffer gain is 1 or 0.25.

DETAILED DESCRIPTION (continued)

Serial Peripheral Interface (SPI)

When the A0 pin is left floating or pulled up to VDD, the SGM41290 switches to SPI communication mode. The SPI interface consists of four signals: CSN, SCLK, SDI, and SDO. The SGM41290 supports the transmission mode with CPOL=0 and CPHA=1, transmitting data to SDO at the rising edge of SCLK and sampling SDI data at the falling edge of SCLK.

Chip Select (CSN)

The CSN pin is used to select the target device for communication. Pulling the CSN pin low selects the device, and it must remain low throughout the entire communication process. After communication ends, wait for at least 2 t_{SCLK} before pulling CSN high.

Serial Clock (SCLK)

The SCLK input serves as the clock signal, which is critical for synchronous serial data transmission. After communication ends and CSN is pulled high, any input on SCLK will be ignored by the device, regardless of its state.

Serial Data Input (SDI)

After the CSN pin is pulled low, the device receives data from the host through SDI. Following the end of communication and pulling CSN high, any input on SDI will be ignored by the device, regardless of the input state.

Serial Data Output (SDO)

After the CSN pin is pulled low, SDO exits the high-impedance state. During communication, data is read from the device in MSB-first order (most significant bit first). Following the end of communication and pulling CSN high, the SDO output enters a high-impedance state, regardless of the state of the SCLK signal.

SPI Read and Write Operations

Table 1. SPI Read/Write Commands

Command	Description	First Byte	Second Byte	Third Byte
		OPCODE1	OPCODE2	OPCODE3
RREG	Read registers	1000 1010 (0x8A)	aaaa aaaa	nnnn nnnn
WREG	Write registers	1010 0101 (0xA5)	aaaa aaaa	nnnn nnnn

The RREG command is used to read registers. OPCODE1 specifies the read-register instruction, OPCODE2 defines the starting address of the first register to be read, and OPCODE3 indicates the number of registers to read minus one (value range: 0 to 255), supporting continuous reading of up to 256 registers.

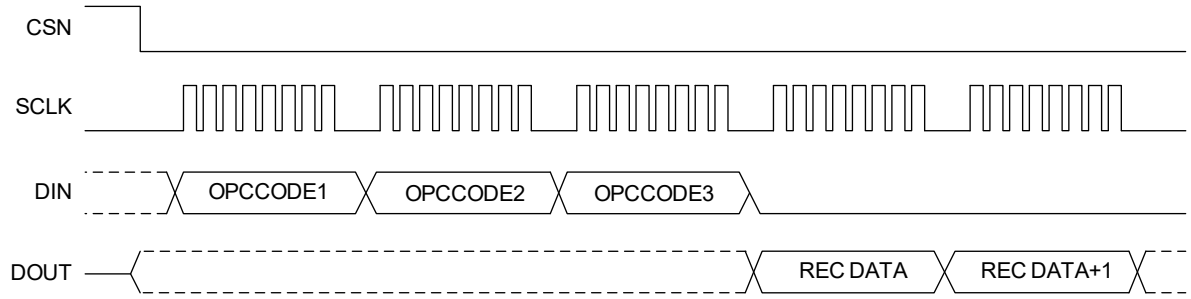


Figure 7. RREG

DETAILED DESCRIPTION (continued)

The WREG command is used to write registers. OPCODE1 specifies the write-register instruction, OPCODE2 defines the starting address of the first register to be written, and OPCODE3 indicates the number of registers to write minus one (value range: 0 to 255), supporting continuous writing to up to 256 registers.

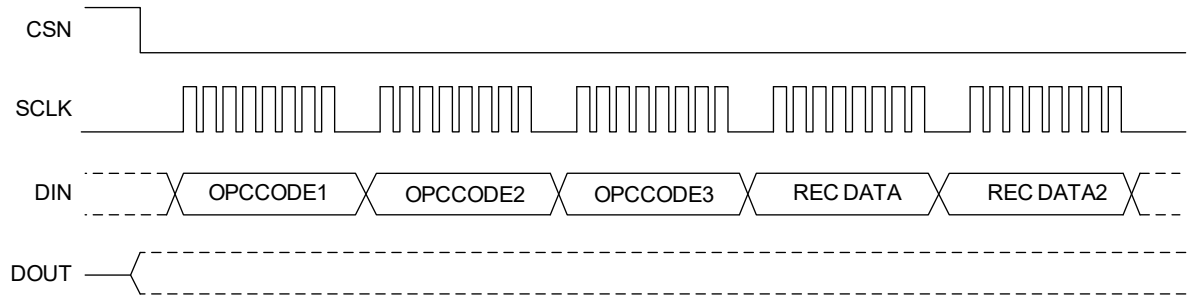


Figure 8. WREG

REGISTER MAP

I²C Slave Address Selection

SGM41290 supports I²C or SPI interfaces. When A0 is floating or pulled up, the SPI interface can be selected. When A0 is grounded or connected to a pull-down resistor, the I²C interface is selected.

I²C Address (MSB)							LSB	8-Bit Write Value (Hex)	R_{ADDR} (kΩ)	Note
0	1	0	1	0	0	0	R/~W	0x50	0	
0	1	0	1	0	0	1	R/~W	0x52	20	
0	1	0	1	0	1	0	R/~W	0x54	40.2	
0	1	0	1	0	1	1	R/~W	0x56	60.4	
0	1	0	1	1	0	0	R/~W	0x58	80.6	
0	1	0	1	1	0	1	R/~W	0x5A	100	
0	1	0	1	1	1	0	R/~W	0x5C	115	
0	1	0	1	1	1	1	R/~W	0x5E	NC or pull-up to VDD	Enable SPI interface

NOTES:

1. Seven different slave addresses can be selected through the resistor R_{ADDR} (E96 1% resistor is recommended) between A0 and GND. The recommended resistance values refer to the table above.
2. When A0 is floating or pulled up, the SPI interface can be selected.

I²C Register Address

Bit Types:

R/W: Read/Write bit(s)

R: Read only bit(s)

W: Write only bit(s)

W1CLR: Write 1 clear bit(s)

Addr	Byte Name	Bit No.	Default	RW	Function
REG0x00	SOFT_RST Register	1:1	00H	W1CLR	Software Reset
REG0x01	CHIP_ID Register	7:0	21H	R	Version ID and Chip ID
REG0x02	SYSTEM STAT0 Register	0:0	00H	W1CLR	Over-Temperature Alarm
REG0x03	EN_BIAS PIN STAT0 Register	3:0	00H	R	EN IBIAS3-0 Pin Status
REG0x04	INT_CTRL0 Register	1:0	00H	R	LOS Pin Output Status and Over-Temperature Fault Interrupt Enable
REG0x05	GER_CTR Register	1:0	0CH	R/W	The GPIO Register Value Lock and I²C Address Increment
REG0x06	Reserved	7:0	00H	R	Reserved
REG0x07	INT_CTRL1 Register	7:0	00H	R/W	Heater7-0 Open/ Short Fault Interrupt Enable
REG0x08	INT_CTRL2 Register	3:0	00H	R/W	Heater11-8 Open/ Short Fault Interrupt Enable
REG0x09	INT_CTRL3 Register	3:0	00H	R/W	IBIAS3-0 Open/Short Fault Interrupt Enable
REG0x0A	HEATER OPEN STAT0 Register	7:0	00H	W1CLR	Heater7-0 Open Circuit Status (In Current Output Mode)
REG0x0B	HEATER OPEN STAT1 Register	3:0	00H	W1CLR	Heater11-8 Open Circuit Status (In Current Output Mode)
REG0x0C	HEATER SHORT STAT0 Register	7:0	00H	W1CLR	Heater7-0 Short Circuit Status (In Voltage Output Mode)
REG0x0D	HEATER SHORT STAT1 Register	3:0	00H	W1CLR	Heater11-8 Short Circuit Status (In Voltage Output Mode)
REG0x0E	IBIAS STAT0 Register	7:0	00H	W1CLR	IBIAS3-0 Open Circuit Status and Short Circuit Status
REG0x10	IBIAS_CTRL0 Register	3:0	00H	R/W	IBIAS3-0 Enable
REG0x11	IBIAS_CTRL1 Register	7:0	2FH	R/W	EN_IBIAS Pin Control Register
REG0x12	IBIAS_CTRL2 Register	7:4	F0H	R/W	EN_BIAS3-0 Switch to Ground Function Enable

REGISTER MAP (continued)

I²C Register Address (continued)

Addr	Byte Name	Bit No.	Default	RW	Function
REG0x13	IBIAS0_LSB Register	7:0	00H	R/W	12bit IBIAS0 Data
REG0x14	IBIAS0_MSB Register	3:0	00H	R/W	
REG0x15	IBIAS1_LSB Register	7:0	00H	R/W	12bit IBIAS1 Data
REG0x16	IBIAS1_MSB Register	3:0	00H	R/W	
REG0x17	IBIAS2_LSB Register	7:0	00H	R/W	12bit IBIAS2 Data
REG0x18	IBIAS2_MSB Register	3:0	00H	R/W	
REG0x19	IBIAS3_LSB Register	7:0	00H	R/W	12bit IBIAS3 Data
REG0x1A	IBIAS3_MSB Register	3:0	00H	R/W	
REG0x1B	IBIAS_CLR Register	0:0	00H	W1CLR	Write 1 to Automatically Clear all Data of IBIAS
REG0x1C	IBIAS_OUT_CTRL Register	0:0	01H	W1CLR	The IBIAS CODE Output Current Update Control
REG0x1D	IBIAS_GAIN_CTRL Register	3:0	00H	R/W	The Current Gain of IBIAS0-3
REG0x20	HEATER_EN0 Register	7:0	00H	R/W	Heater7-0 Enable
REG0x21	HEATER_EN1 Register	3:0	00H	R/W	Heater11-8 Enable
REG0x22	HEATER_GAIN0 Register	7:0	00H	R/W	Heater7-0 Voltage Range Selection
REG0x23	HEATER_GAIN1 Register	3:0	00H	R/W	Heater11-8 Voltage Range Selection
REG0x24	HEATER_MODE Register	2:0	00H	R/W	Heater8~11/ 4~7/ 0~3 Mode Selection
REG0x25	Reserved	7:0	00H	R	Reserved
REG0x26	HEATER0_LSB Register	7:0	00H	R/W	12bit Heater0 Data
REG0x27	HEATER0_MSB Register	3:0	00H	R/W	
REG0x28	HEATER1_LSB Register	7:0	00H	R/W	12bit Heater1 Data
REG0x29	HEATER1_MSB Register	3:0	00H	R/W	
REG0x2A	HEATER2_LSB Register	7:0	00H	R/W	12bit Heater2 Data
REG0x2B	HEATER2_MSB Register	3:0	00H	R/W	
REG0x2C	HEATER3_LSB Register	7:0	00H	R/W	12bit Heater3 Data
REG0x2D	HEATER3_MSB Register	3:0	00H	R/W	
REG0x2E	HEATER4_LSB Register	7:0	00H	R/W	12bit Heater4 Data
REG0x2F	HEATER4_MSB Register	3:0	00H	R/W	
REG0x30	HEATER5_LSB Register	7:0	00H	R/W	12bit Heater5 Data
REG0x31	HEATER5_MSB Register	3:0	00H	R/W	
REG0x32	HEATER6_LSB Register	7:0	00H	R/W	12bit Heater6 Data
REG0x33	HEATER6_MSB Register	3:0	00H	R/W	
REG0x34	HEATER7_LSB Register	7:0	00H	R/W	12bit Heater7 Data
REG0x35	HEATER7_MSB Register	3:0	00H	R/W	
REG0x36	HEATER8_LSB Register	7:0	00H	R/W	12bit Heater8 Data
REG0x37	HEATER8_MSB Register	3:0	00H	R/W	
REG0x38	HEATER9_LSB Register	7:0	00H	R/W	12bit Heater9 Data
REG0x39	HEATER9_MSB Register	3:0	00H	R/W	
REG0x3A	HEATER10_LSB Register	7:0	00H	R/W	12bit Heater10 Data
REG0x3B	HEATER10_MSB Register	3:0	00H	R/W	
REG0x3C	HEATER11_LSB Register	7:0	00H	R/W	12bit Heater11 Data
REG0x3D	HEATER11_MSB Register	3:0	00H	R/W	

REGISTER MAP (continued)

I²C Register Address (continued)

Addr	Byte Name	Bit No.	Default	RW	Function
REG0x40	MULTI_IO_CTRL0 Register	5:0	24H	R/W	MULTI_IO1-0 Configuration
REG0x41	MULTI_IO_CTRL1 Register	5:0	24H	R/W	MULTI_IO3-2 Configuration
REG0x42	MULTI_IO_CTRL2 Register	5:0	24H	R/W	MULTI_IO5-4 Configuration
REG0x43	MULTI_IO_CTRL3 Register	5:0	24H	R/W	MULTI_IO7-6 Configuration
REG0x44	MULTI_IO_CTRL4 Register	5:0	24H	R/W	MULTI_IO9-8 Configuration
REG0x45	MULTI_IO_CTRL5 Register	5:0	24H	R/W	MULTI_IO11-10 Configuration
REG0x46	GPIO_OE0 Register	7:0	00H	R/W	GPIO7-0 Output Enable
REG0x47	GPIO_OE1 Register	3:0	00H	R/W	GPIO11-8 Output Enable
REG0x48	GPIO_IE0 Register	7:0	00H	R/W	GPIO7-0 Input Enable
REG0x49	GPIO_IE1 Register	3:0	00H	R/W	GPIO11-8 Input Enable
REG0x4A	GPIO_OUT0 Register	7:0	00H	R/W	GPIO7-0 Output Level
REG0x4B	GPIO_OUT1 Register	3:0	00H	R/W	GPIO11-8 Output Level
REG0x4C	GPIO_IN0 Register	7:0	00H	R	GPIO7-0 Input Level
REG0x4D	GPIO_IN1 Register	3:0	00H	R	GPIO11-8 Input Level
REG0x4E	GPIO_OD0 Register	7:0	00H	R/W	GPIO7-0 Open-Drain Output Enable
REG0x4F	GPIO_OD1 Register	3:0	00H	R/W	GPIO11-8 Open-Drain Output Enable
REG0x50	GPIO_PP0 Register	7:0	00H	R/W	Mode Selection with GPIO3-0 as Input Pin
REG0x51	GPIO_PP1 Register	7:0	00H	R/W	Mode Selection with GPIO7-4 as Input Pin
REG0x52	GPIO_PP2 Register	7:0	00H	R/W	Mode Selection with GPIO11-8 as Input Pin
REG0x53	GPIO_DR Register	1:0	00H	R/W	Output Driver Capability Selection, Available to all GPIOS
REG0x54	MON_VSEL0 Register	6:0	40H	R/W	Voltage Gain Selection The internal voltage signal is sent to MON0. Select the Internal Voltage Signal to MON0 or MON1.
REG0x55	MON_VSEL1 Register	5:5	00H	R/W	The internal voltage signal is sent to MON1
REG0x56	MON_GAIN32 Register	7:0	00H	R/W	MULTI_IO7-0 Current Gain Selection
REG0x57	MON_CTRL Register	4:0	00H	R/W	Send MULTI_IO8~11 to MON0 or to MON1 MULTI_IO11-8 Current Gain Selection.
REG0x58	MON_MSEL Register	7:0	00H	R/W	Select one of MULTI_IO11~8/ 7-0 to send to MON0/1 Enable MULTI_IO8~11 sent to MON0/1. Enable MULTI_IO7~0 sent to MON0.
REG0xA4	MISC_CTRL1 Register	1:0	00H	R/W	SPI SDO/I²C SDA Driver Ability Configuration

NOTE: Registers at other addresses not separately mentioned in the register map are reserved and read-only.

REGISTER MAP (continued)

REG0x00: SOFT_RST Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	000000	R	Reserved
D[1]	SOFT_RST	0	W1CLR	Software Reset
D[0]	Reserved	0	R	Reserved

REG0x01: CHIP_ID Register [Reset = 0x21]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	VER_ID	0010	R	Version ID
D[3:0]	CHIP_ID	0001	R	Chip ID

REG0x02: SYSTEM STAT0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:1]	Reserved	0000000	R	Reserved
D[0]	OT_ALERT	0	W1CLR	Over-Temperature Alarm (write 1 clear status bit) 0 = No alarm (default) 1 = Alarm

REG0x03: EN_BIAS PIN STAT0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	00	R	Reserved
D[3]	ST_EN_IBIAS3	0	R	EN IBIAS3 Pin Status 0 = Low (default) 1 = High
D[2]	ST_EN_IBIAS2	0	R	EN IBIAS2 Pin Status 0 = Low (default) 1 = High
D[1]	ST_EN_IBIAS1	0	R	EN IBIAS1 Pin Status 0 = Low (default) 1 = High
D[0]	ST_EN_IBIAS0	0	R	EN IBIAS0 Pin Status 0 = Low (default) 1 = High

REG0x04: INT_CTRL 0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	00000	R	Reserved
D[1]	OT_INT_EN	0	R/W	Over-Temperature Fault Interrupt Enable 0 = Disable interrupt 1 = Enable interrupt
D[0]	LOS_OE	0	R/W	LOS Pin Output Status 0 = Disable (default) 1 = Enable

REGISTER MAP (continued)

REG0x05: GER_CTR Register [Reset = 0x0C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	000011	R	Reserved
D[1]	IO_LOCK	0	R/W	The GPIO register value cannot be overwritten after MULTI_IO is locked. 0 = Not locked (default) 1 = Locked
D[0]	I^2C_INC	0	R/W	I^2C Address Increment 0 = Recursion (default) 1 = Not incrementing

REG0x06: Reserved Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	00000000	R	Reserved

REG0x07: INT_CTRL 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Heater7_INT_EN	0	R/W	Heater7 Open/Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt
D[6]	Heater6_INT_EN	0	R/W	Heater6 Open/Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt
D[5]	Heater5_INT_EN	0	R/W	Heater5 Open/Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt
D[4]	Heater4_INT_EN	0	R/W	Heater4 Open/Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt
D[3]	Heater3_INT_EN	0	R/W	Heater3 Open/Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt
D[2]	Heater2_INT_EN	0	R/W	Heater2 Open/Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt
D[1]	Heater1_INT_EN	0	R/W	Heater1 Open/Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt
D[0]	Heater0_INT_EN	0	R/W	Heater0 Open/Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt

REG0x08: INT_CTRL 2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	reserved	0	R	Reserved
D[3]	Heater11_INT_EN	0	R/W	Heater11 Open/ Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt
D[2]	Heater10_INT_EN	0	R/W	Heater10 Open/ Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt
D[1]	Heater9_INT_EN	0	R/W	Heater9 Open/ Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt
D[0]	Heater8_INT_EN	0	R/W	Heater8 Open/ Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt

REGISTER MAP (continued)

REG0x09: INT_CTRL 3 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	reserved	0	R	Reserved
D[3]	IBIAS3_INT_EN	0	R/W	IBIAS3 Open/Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt
D[2]	IBIAS2_INT_EN	0	R/W	IBIAS2 Open/Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt
D[1]	IBIAS1_INT_EN	0	R/W	IBIAS1 Open/Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt
D[0]	IBIAS0_INT_EN	0	R/W	IBIAS0 Open/Short Fault Interrupt Enable 0 = Disable interrupt (default) 1 = Enable interrupt

REG0x0A: HEATER OPEN STAT0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Heater7_OPEN_Flag	0	W1CLR	In Current Output Mode 1 = Heater7 open 0 = Heater7 not open
D[6]	Heater6_OPEN_Flag	0	W1CLR	In Current Output Mode 1 = Heater6 open 0 = Heater6 not open
D[5]	Heater5_OPEN_Flag	0	W1CLR	In Current Output Mode 1 = Heater5 open 0 = Heater5 not open
D[4]	Heater4_OPEN_Flag	0	W1CLR	In Current Output Mode 1 = Heater4 open 0 = Heater4 not open
D[3]	Heater3_OPEN_Flag	0	W1CLR	In Current Output Mode 1 = Heater3 open 0 = Heater3 not open
D[2]	Heater2_OPEN_Flag	0	W1CLR	In Current Output Mode 1 = Heater2 open 0 = Heater2 not open
D[1]	Heater1_OPEN_Flag	0	W1CLR	In Current Output Mode 1 = Heater1 open 0 = Heater1 not open
D[0]	Heater0_OPEN_Flag	0	W1CLR	In Current Output Mode 1 = Heater0 open 0 = Heater0 not open

REG0x0B: HEATER OPEN STAT1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3]	Heater11_OPEN_Flag	0	W1CLR	In Current Output Mode 1 = Heater11 open 0 = Heater11 not open
D[2]	Heater10_OPEN_Flag	0	W1CLR	In Current Output Mode 1 = Heater10 open 0 = Heater10 not open
D[1]	Heater9_OPEN_Flag	0	W1CLR	In Current Output Mode 1 = Heater9 open 0 = Heater9 not open
D[0]	Heater8_OPEN_Flag	0	W1CLR	In Current Output Mode 1 = Heater8 open 0 = Heater8 not open

REGISTER MAP (continued)

REG0x0C: HEATER SHORT STAT0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Heater7_Short_Flag	0	W1CLR	In Voltage Output Mode 1 = Heater7 short 0 = Heater7 not short
D[6]	Heater6_Short_Flag	0	W1CLR	In Voltage Output Mode 1 = Heater6 short 0 = Heater6 not short
D[5]	Heater5_Short_Flag	0	W1CLR	In Voltage Output Mode 1 = Heater5 short 0 = Heater5 not short
D[4]	Heater4_Short_Flag	0	W1CLR	In Voltage Output Mode 1 = Heater4 short 0 = Heater4 not short
D[3]	Heater3_Short_Flag	0	W1CLR	In Voltage Output Mode 1 = Heater3 short 0 = Heater3 not short
D[2]	Heater2_Short_Flag	0	W1CLR	In Voltage Output Mode 1 = Heater2 short 0 = Heater2 not short
D[1]	Heater1_Short_Flag	0	W1CLR	In Voltage Output Mode 1 = Heater1 short 0 = Heater1 not short
D[0]	Heater0_Short_Flag	0	W1CLR	In Voltage Output Mode 1 = Heater0 short 0 = Heater0 not short

REG0x0D: HEATER SHORT STAT1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3]	Heater11_short_Flag	0	W1CLR	In Voltage Output Mode 1 = Heater11 short 0 = Heater11 not short
D[2]	Heater10_short_Flag	0	W1CLR	In Voltage Output Mode 1 = Heater10 short 0 = Heater10 not short
D[1]	Heater9_short_Flag	0	W1CLR	In Voltage Output Mode 1 = Heater9 short 0 = Heater9 not short
D[0]	Heater8_short_Flag	0	W1CLR	In Voltage Output Mode 1 = Heater8 short 0 = Heater8 not short

REG0x0E: IBIAS STAT0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	IBIAS3_OPEN_Flag	0	W1CLR	1 = IBIAS3 open 0 = IBIAS3 not open
D[6]	IBIAS2_OPEN_Flag	0	W1CLR	1 = IBIAS2 open 0 = IBIAS2 not open
D[5]	IBIAS1_OPEN_Flag	0	W1CLR	1 = IBIAS1 open 0 = IBIAS1 not open
D[4]	IBIAS0_OPEN_Flag	0	W1CLR	1 = IBIAS0 open 0 = IBIAS0 not open
D[3]	IBIAS3_Short_Flag	0	W1CLR	1 = IBIAS3 short 0 = IBIAS3 not short
D[2]	IBIAS2_Short_Flag	0	W1CLR	1 = IBIAS2 short 0 = IBIAS2 not short
D[1]	IBIAS1_Short_Flag	0	W1CLR	1 = IBIAS1 short 0 = IBIAS1 not short
D[0]	IBIAS0_Short_Flag	0	W1CLR	1 = IBIAS0 short 0 = IBIAS0 not short

REGISTER MAP (continued)

REG0x10: IBIAS_CTRL0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3]	IBIAS3_EN	0	R/W	IBIAS3 Enable 0 = Disable (default) 1 = Enable
D[2]	IBIAS2_EN	0	R/W	IBIAS2 Enable 0 = Disable (default) 1 = Enable
D[1]	IBIAS1_EN	0	R/W	IBIAS1 Enable 0 = Disable (default) 1 = Enable
D[0]	IBIAS0_EN	0	R/W	IBIAS0 Enable 0 = Disable (default) 1 = Enable

REG0x11: IBIAS_CTRL1 Register [Reset = 0x2F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	SHARE_EN_IBIAS23	0	R/W	The two IBIAS share the EN_IBIAS2 pin, and EN_IBIAS2 can shut down IBIAS2~IBIAS3. 0 = Not shared (default) 1 = Shared use
D[6]	Reserved	0	R	Reserved
D[5]	IBIAS_EN_ALL	1	R/W	All the IBIAS share the IBIAS_EN_ALL bit, and IBIAS_EN_ALL can shut down all channels. 0 = Shutdown all channels 1 = Shutdown depends on IBIAS_EN BITs (default),
D[4]	SHARE_EN_IBIAS01	0	R/W	The two IBIAS share the EN_IBIAS0 pin, and EN_IBIAS0 can shut down IBIAS0~IBIAS1. 0 = Not shared (default) 1 = Shared use
D[3]	PIN_IBIAS3_EN	1	R/W	EN_IBIAS3 Pin Enable 0 = Do not turn off 1 = Turn off (default)
D[2]	PIN_IBIAS2_EN	1	R/W	EN_IBIAS2 Pin Enable 0 = Do not turn off 1 = Turn off (default)
D[1]	PIN_IBIAS1_EN	1	R/W	EN_IBIAS1 Pin Enable 0 = Do not turn off 1 = Turn off (default)
D[0]	PIN_IBIAS0_EN	1	R/W	EN_IBIAS0 Pin Enable 0 = Do not turn off 1 = Turn off (default)

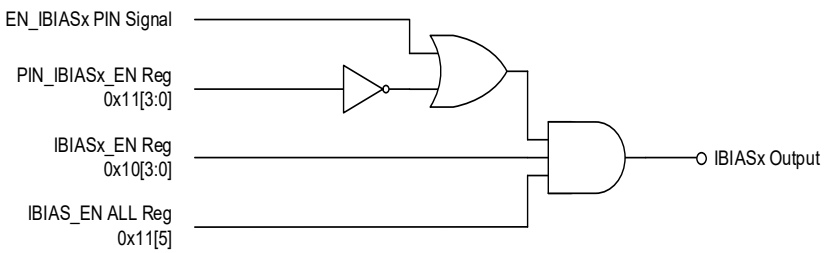


Figure 9. IBIAS Output Logic Diagram

REGISTER MAP (continued)

REG0x12: IBIAS_CTRL2 Register [Reset = 0xF0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	IBIAS3_SW2GND	1	R/W	EN_BIAS3 Switch to Ground Function Enabled 0 = Disable, EN_IBIAS only turns off the output current 1 = Enable, EN_IBIAS turns off the output current, and pulls the output to the ground (default)
D[6]	IBIAS2_SW2GND	1	R/W	EN_BIAS2 Switch to Ground Function Enabled 0 = Disable, EN_IBIAS only turns off the output current 1 = Enable, EN_IBIAS turns off the output current, and pulls the output to the ground (default)
D[5]	IBIAS1_SW2GND	1	R/W	EN_BIAS1 Switch to Ground Function Enabled 0 = Disable, EN_IBIAS only turns off the output current 1 = Enable, EN_IBIAS turns off the output current, and pulls the output to the ground (default)
D[4]	IBIAS0_SW2GND	1	R/W	EN_BIAS0 Switch to Ground Function Enabled 0 = Disable, EN_IBIAS only turns off the output current 1 = Enable, EN_IBIAS turns off the output current, and pulls the output to the ground (default)
D[3:0]	Reserved	0000	R	Reserved

REG0x13: IBIAS0_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	IBIAS0_DATA[7:0]	00000000	R/W	Low Byte IBIAS0 Data

REG0x14: IBIAS0_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	IBIAS0_DATA[11:8]	0000	R/W	High 4-Bit IBIAS0 Data

REG0x15: IBIAS1_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	IBIAS1_DATA[7:0]	00000000	R/W	Low Byte IBIAS1 Data

REG0x16: IBIAS1_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	IBIAS1_DATA[11:8]	0000	R/W	High 4-Bit IBIAS1 Data

REGISTER MAP (continued)

REG0x17: IBIAS2_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	IBIAS2_DATA[7:0]	00000000	R/W	Low Byte IBIAS2 Data

REG0x18: IBIAS2_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	IBIAS2_DATA[11:8]	0000	R/W	High 4-Bit IBIAS2 Data

REG0x19: IBIAS3_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	IBIAS3_DATA[7:0]	00000000	R/W	Low Byte IBIAS4 Data

REG0x1A: IBIAS3_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	IBIAS3_DATA[11:8]	0000	R/W	High 4-Bit IBIAS4 Data

REG0x1B: IBIAS_CLR Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	0000000	R	Reserved
D[0]	IBIAS_CLR	0	W1CLR	Write 1 to Automatically Clear all Data of IBIAS

REG0x1C: IBIAS_OUT_CTRL Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	0000000	R	Reserved
D[0]	IBIAS_OUT_CTRL	1	W/R	The IBIAS CODE Output Current Update Control 0 = Output current is updated only when MSB is written 1 = The output current is updated when the LSB or MSB register is written (default)

NOTE: This register does not support read-back. It can be written after confirming that communication is normal. In addition, this register allows multiple writes.

REGISTER MAP (continued)

REG0x1D: IBIAS_GAIN_CTRL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3]	IBIAS3_Gain	0	R/W	IBIAS3 Current Gain 0 = Current gain is 1 (default) 1 = Current gain is 1.5
D[2]	IBIAS2_Gain	0	R/W	IBIAS2 Current Gain 0 = Current gain is 1 (default) 1 = Current gain is 1.5
D[1]	IBIAS1_Gain	0	R/W	IBIAS1 Current Gain 0 = Current gain is 1 (default) 1 = Current gain is 1.5
D[0]	IBIAS0_Gain	0	R/W	IBIAS0 Current Gain 0 = Current gain is 1 (default) 1 = Current gain is 1.5

REG0x20: HEATER_EN0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	HEATER7_EN	0	R/W	0 = Heater7 disable (default) 1 = Heater7 enable
D[6]	HEATER6_EN	0	R/W	0 = Heater6 disable (default) 1 = Heater6 enable
D[5]	HEATER5_EN	0	R/W	0 = Heater5 disable (default) 1 = Heater5 enable
D[4]	HEATER4_EN	0	R/W	0 = Heater4 disable (default) 1 = Heater4 enable
D[3]	HEATER3_EN	0	R/W	0 = Heater3 disable (default) 1 = Heater3 enable
D[2]	HEATER2_EN	0	R/W	0 = Heater2 disable (default) 1 = Heater2 enable
D[1]	HEATER1_EN	0	R/W	0 = Heater1 disable (default) 1 = Heater1 enable
D[0]	HEATER0_EN	0	R/W	0 = Heater0 disable (default) 1 = Heater0 enable

REG0x21: HEATER_EN1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3]	HEATER11_EN	0	R/W	0 = Heater11 disable (default) 1 = Heater11 enable
D[2]	HEATER10_EN	0	R/W	0 = Heater10 disable (default) 1 = Heater10 enable
D[1]	HEATER9_EN	0	R/W	0 = Heater9 disable (default) 1 = Heater9 enable
D[0]	HEATER8_EN	0	R/W	0 = Heater8 disable (default) 1 = Heater8 enable

REGISTER MAP (continued)

REG0x22: HEATER_GAIN0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	HEATER7_GAIN	0	R/W	Heater7 Gain Selection 0 = Voltage Gain = 1, 0~2.5V (default) 1 = Voltage Gain = 2, 0~5V
D[6]	HEATER6_GAIN	0	R/W	Heater6 Gain Selection 0 = Voltage Gain = 1, 0~2.5V (default) 1 = Voltage Gain = 2, 0~5V
D[5]	HEATER5_GAIN	0	R/W	Heater5 Gain Selection 0 = Voltage Gain = 1, 0~2.5V (default) 1 = Voltage Gain = 2, 0~5V
D[4]	HEATER4_GAIN	0	R/W	Heater4 Gain Selection 0 = Voltage Gain = 1, 0~2.5V (default) 1 = Voltage Gain = 2, 0~5V
D[3]	HEATER3_GAIN	0	R/W	Heater3 Gain Selection 0 = Voltage Gain = 1, 0~2.5V (default) 1 = Voltage Gain = 2, 0~5V
D[2]	HEATER2_GAIN	0	R/W	Heater2 Gain Selection 0 = Voltage Gain = 1, 0~2.5V (default) 1 = Voltage Gain = 2, 0~5V
D[1]	HEATER1_GAIN	0	R/W	Heater1 Gain Selection 0 = Voltage Gain = 1, 0~2.5V (default) 1 = Voltage Gain = 2, 0~5V
D[0]	HEATER0_GAIN	0	R/W	Heater0 Gain Selection 0 = Voltage Gain = 1, 0~2.5V (default) 1 = Voltage Gain = 2, 0~5V

REG0x23: HEATER_GAIN1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3]	HEATER11_GAIN	0	R/W	Heater11 Gain Selection 0 = Voltage Gain = 1, 0~2.5V (default) 1 = Voltage Gain = 2, 0~5V
D[2]	HEATER10_GAIN	0	R/W	Heater10 Gain Selection 0 = Voltage Gain = 1, 0~2.5V (default) 1 = Voltage Gain = 2, 0~5V
D[1]	HEATER9_GAIN	0	R/W	Heater9 Gain Selection 0 = Voltage Gain = 1, 0~2.5V (default) 1 = Voltage Gain = 2, 0~5V
D[0]	HEATER8_GAIN	0	R/W	Heater8 Gain Selection 0 = Voltage Gain = 1, 0~2.5V (default) 1 = Voltage Gain = 2, 0~5V

REG0x24: HEATER_MODE Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:3]	Reserved	00000	R	Reserved
D[2]	HEATER2_MODE	0	R/W	Heater8~11 Mode Selection 0 = IDAC mode (default) 1 = VDAC mode
D[1]	HEATER1_MODE	0	R/W	Heater4~7 Mode Selection 0 = IDAC mode (default) 1 = VDAC mode
D[0]	HEATER0_MODE	0	R/W	Heater0~3 Mode Selection 0 = IDAC mode (default) 1 = VDAC mode

REGISTER MAP (continued)

REG0x25: Reserved Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	00000000	R	Reserved

REG0x26: HEATER0_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	HEATER0_DATA[7:0]	00000000	R/W	Low Byte Heater0 Data

REG0x27: HEATER0_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	HEATER0_DATA[11:8]	0000	R/W	High 4-Bit Heater0 Data

REG0x28: HEATER1_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	HEATER1_DATA[7:0]	00000000	R/W	Low Byte Heater1 Data

REG0x29: HEATER1_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	HEATER1_DATA[11:8]	0000	R/W	High 4-Bit Heater1 Data

REG0x2A: HEATER2_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	HEATER2_DATA[7:0]	00000000	R/W	Low Byte Heater2 Data

REG0x2B: HEATER2_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	HEATER2_DATA[11:8]	0000	R/W	High 4-Bit Heater2 Data

REGISTER MAP (continued)

REG0x2C: HEATER3_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	HEATER3_DATA[7:0]	00000000	R/W	Low Byte Heater3 Data

REG0x2D: HEATER3_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	HEATER3_DATA[11:8]	0000	R/W	High 4-Bit Heater3 Data

REG0x2E: HEATER4_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	HEATER4_DATA[7:0]	00000000	R/W	Low Byte Heater4 Data

REG0x2F: HEATER4_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	HEATER4_DATA[11:8]	0000	R/W	High 4-Bit Heater4 Data

REG0x30: HEATER5_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	HEATER5_DATA[7:0]	00000000	R/W	Low Byte Heater5 Data

REG0x31: HEATER5_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	HEATER5_DATA[11:8]	0000	R/W	High 4-Bit Heater5 Data

REG0x32: HEATER6_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	HEATER6_DATA[7:0]	00000000	R/W	Low Byte Heater6 Data

REGISTER MAP (continued)

REG0x33: HEATER6_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	HEATER6_DATA[11:8]	0000	R/W	High 4-Bit Heater6 Data

REG0x34: HEATER7_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	HEATER7_DATA[7:0]	00000000	R/W	Low Byte Heater7 Data

REG0x35: HEATER7_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	HEATER7_DATA[11:8]	0000	R/W	High 4-Bit Heater7 Data

REG0x36: HEATER8_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	HEATER8_DATA[7:0]	00000000	R/W	Low Byte Heater8 Data

REG0x37: HEATER8_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	HEATER8_DATA[11:8]	0000	R/W	High 4-Bit Heater8 Data

REG0x38: HEATER9_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	HEATER9_DATA[7:0]	00000000	R/W	Low Byte Heater9 Data

REG0x39: HEATER9_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	HEATER9_DATA[11:8]	0000	R/W	High 4-Bit Heater9 Data

REGISTER MAP (continued)

REG0x3A: HEATER10_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	HEATER10_DATA[7:0]	00000000	R/W	Low Byte Heater10 Data

REG0x3B: HEATER10_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	HEATER10_DATA[11:8]	0000	R/W	High 4-Bit Heater10 Data

REG0x3C: HEATER11_LSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	HEATER11_DATA[7:0]	00000000	R/W	Low Byte Heater11 Data

REG0x3D: HEATER11_MSB Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3:0]	HEATER11_DATA[11:8]	0000	R/W	High 4-Bit Heater11 Data

REG0x40: MULTI_IO_CTRL0 Register [Reset = 0x24]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R	Reserved
D[5:3]	MIO1_CON	100	R/W	MULTI_IO1 Configuration 000 = Type A: Current sink input 001 = Type B: Current source input 010 = Type C: The current source input is directly sent to the MON without mirroring 011 = Type D: The current source is input to the internal resistor 100 = Type E: GPIO (default)
D[2:0]	MIO0_CON	100	R/W	MULTI_IO0 Configuration 000 = Type A: Current sink input 001 = Type B: Current source input 010 = Type C: The current source input is directly sent to the MON without mirroring 011 = Type D: The current source is input to the internal resistor 100 = Type E: GPIO (default)

REGISTER MAP (continued)

REG0x41: MULTI_IO_CTRL1 Register [Reset = 0x24]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R	Reserved
D[5:3]	MIO3_CON	100	R/W	MULTI_IO3 Configuration 000 = Type A: Current sink input 001 = Type B: Current source input 010 = Type C: The current source input is directly sent to the MON without mirroring 011 = Type D: The current source is input to the internal resistor 100 = Type E: GPIO (default)
D[2:0]	MIO2_CON	100	R/W	MULTI_IO2 Configuration 000 = Type A: Current sink input 001 = Type B: Current source input 010 = Type C: The current source input is directly sent to the MON without mirroring 011 = Type D: The current source is input to the internal resistor 100 = Type E: GPIO (default)

REG0x42: MULTI_IO_CTRL2 Register [Reset = 0x24]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R	Reserved
D[5:3]	MIO5_CON	100	R/W	MULTI_IO5 Configuration 000 = Type A: Current sink input 001 = Type B: Current source input 010 = Type C: The current source input is directly sent to the MON without mirroring 011 = Type D: The current source is input to the internal resistor 100 = Type E: GPIO (default)
D[2:0]	MIO4_CON	100	R/W	MULTI_IO4 Configuration 000 = Type A: Current sink input 001 = Type B: Current source input 010 = Type C: The current source input is directly sent to the MON without mirroring 011 = Type D: The current source is input to the internal resistor 100 = Type E: GPIO (default)

REG0x43: MULTI_IO_CTRL3 Register [Reset = 0x24]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R	Reserved
D[5:3]	MIO7_CON	100	R/W	MULTI_IO7 Configuration 000 = Type A: Current sink input 001 = Type B: Current source input 010 = Type C: The current source input is directly sent to the MON without mirroring 011 = Type D: The current source is input to the internal resistor 100 = Type E: GPIO (default)
D[2:0]	MIO6_CON	100	R/W	MULTI_IO6 Configuration 000 = Type A: Current sink input 001 = Type B: Current source input 010 = Type C: The current source input is directly sent to the MON without mirroring 011 = Type D: The current source is input to the internal resistor 100 = Type E: GPIO (default)

REGISTER MAP (continued)

REG0x44: MULTI_IO_CTRL4 Register [Reset = 0x24]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R	Reserved
D[5:3]	MIO9_CON	100	R/W	MULTI_IO9 Configuration 000 = Type A: Current sink input 001 = Type B: Current source input 010 = Type C: The current source input is directly sent to the MON without mirroring 011 = Type D: The current source is input to the internal resistor 100 = Type E: GPIO (default)
D[2:0]	MIO8_CON	100	R/W	MULTI_IO8 Configuration 000 = Type A: Current sink input 001 = Type B: Current source input 010 = Type C: The current source input is directly sent to the MON without mirroring 011 = Type D: The current source is input to the internal resistor 100 = Type E: GPIO (default)

REG0x45: MULTI_IO_CTRL5 Register [Reset = 0x24]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R	Reserved
D[5:3]	MIO11_CON	100	R/W	MULTI_IO11 Configuration 000 = Type A: Current sink input 001 = Type B: Current source input 010 = Type C: The current source input is directly sent to the MON without mirroring 011 = Type D: The current source is input to the internal resistor 100 = Type E: GPIO (default)
D[2:0]	MIO10_CON	100	R/W	MULTI_IO10 Configuration 000 = Type A: Current sink input 001 = Type B: Current source input 010 = Type C: The current source input is directly sent to the MON without mirroring 011 = Type D: The current source is input to the internal resistor 100 = Type E: GPIO (default)

REGISTER MAP (continued)

REG0x46: GPIO_OE0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	GPIO7_OE	0	R/W	GPIO7 Output Enable 0 = Disable (default) 1 = Enabled
D[6]	GPIO6_OE	0	R/W	GPIO6 Output Enable 0 = Disable (default) 1 = Enabled
D[5]	GPIO5_OE	0	R/W	GPIO5 Output Enable 0 = Disable (default) 1 = Enabled
D[4]	GPIO4_OE	0	R/W	GPIO4 Output Enable 0 = Disable (default) 1 = Enabled
D[3]	GPIO3_OE	0	R/W	GPIO3 Output Enable 0 = Disable (default) 1 = Enabled
D[2]	GPIO2_OE	0	R/W	GPIO2 Output Enable 0 = Disable (default) 1 = Enabled
D[1]	GPIO1_OE	0	R/W	GPIO1 Output Enable 0 = Disable (default) 1 = Enabled
D[0]	GPIO0_OE	0	R/W	GPIO0 Output Enable 0 = Disable (default) 1 = Enabled

REG0x47: GPIO_OE1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3]	GPIO11_OE	0	R/W	GPIO11 Output Enable 0 = Disable (default) 1 = Enabled
D[2]	GPIO10_OE	0	R/W	GPIO10 Output Enable 0 = Disable (default) 1 = Enabled
D[1]	GPIO9_OE	0	R/W	GPIO9 Output Enable 0 = Disable (default) 1 = Enabled
D[0]	GPIO8_OE	0	R/W	GPIO8 Output Enable 0 = Disable (default) 1 = Enabled

REGISTER MAP (continued)

REG0x48: GPIO_IE0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	GPIO7_IE	0	R/W	GPIO7 Input Enable 0 = Disable (default) 1 = Enabled
D[6]	GPIO6_IE	0	R/W	GPIO6 Input Enable 0 = Disable (default) 1 = Enabled
D[5]	GPIO5_IE	0	R/W	GPIO5 Input Enable 0 = Disable (default) 1 = Enabled
D[4]	GPIO4_IE	0	R/W	GPIO4 Input Enable 0 = Disable (default) 1 = Enabled
D[3]	GPIO3_IE	0	R/W	GPIO3 Input Enable 0 = Disable (default) 1 = Enabled
D[2]	GPIO2_IE	0	R/W	GPIO2 Input Enable 0 = Disable (default) 1 = Enabled
D[1]	GPIO1_IE	0	R/W	GPIO1 Input Enable 0 = Disable (default) 1 = Enabled
D[0]	GPIO0_IE	0	R/W	GPIO0 Input Enable 0 = Disable (default) 1 = Enabled

REG0x49: GPIO_IE1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3]	GPIO11_IE	0	R/W	GPIO11 Input Enable 0 = Disable (default) 1 = Enabled
D[2]	GPIO10_IE	0	R/W	GPIO10 Input Enable 0 = Disable (default) 1 = Enabled
D[1]	GPIO9_IE	0	R/W	GPIO9 Input Enable 0 = Disable (default) 1 = Enabled
D[0]	GPIO8_IE	0	R/W	GPIO8 Input Enable 0 = Disable (default) 1 = Enabled

REGISTER MAP (continued)

REG0x4A: GPIO_OUT0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	GPIO7_OUT	0	R/W	GPIO7 Output 0 = Output Low (default) 1 = Output High
D[6]	GPIO6_OUT	0	R/W	GPIO6 Output 0 = Output Low (default) 1 = Output High
D[5]	GPIO5_OUT	0	R/W	GPIO5 Output 0 = Output Low (default) 1 = Output High
D[4]	GPIO4_OUT	0	R/W	GPIO4 Output 0 = Output Low (default) 1 = Output High
D[3]	GPIO3_OUT	0	R/W	GPIO3 Output 0 = Output Low (default) 1 = Output High
D[2]	GPIO2_OUT	0	R/W	GPIO2 Output 0 = Output Low (default) 1 = Output High
D[1]	GPIO1_OUT	0	R/W	GPIO1 Output 0 = Output Low (default) 1 = Output High
D[0]	GPIO0_OUT	0	R/W	GPIO0 Output 0 = Output Low (default) 1 = Output High

REG0x4B: GPIO_OUT1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3]	GPIO11_OUT	0	R/W	GPIO11 Output 0 = Output Low (default) 1 = Output High
D[2]	GPIO10_OUT	0	R/W	GPIO10 Output 0 = Output Low (default) 1 = Output High
D[1]	GPIO9_OUT	0	R/W	GPIO9 Output 0 = Output Low (default) 1 = Output High
D[0]	GPIO8_OUT	0	R/W	GPIO8 Output 0 = Output Low (default) 1 = Output High

REGISTER MAP (continued)

REG0x4C: GPIO_IN0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	GPIO7_IN	0	R	GPIO7 Input Status Detection 0 = Input Low (default) 1 = Input High
D[6]	GPIO6_IN	0	R	GPIO6 Input Status Detection 0 = Input Low (default) 1 = Input High
D[5]	GPIO5_IN	0	R	GPIO5 Input Status Detection 0 = Input Low (default) 1 = Input High
D[4]	GPIO4_IN	0	R	GPIO4 Input Status Detection 0 = Input Low (default) 1 = Input High
D[3]	GPIO3_IN	0	R	GPIO3 Input Status Detection 0 = Input Low (default) 1 = Input High
D[2]	GPIO2_IN	0	R	GPIO2 Input Status Detection 0 = Input Low (default) 1 = Input High
D[1]	GPIO1_IN	0	R	GPIO1 Input Status Detection 0 = Input Low (default) 1 = Input High
D[0]	GPIO0_IN	0	R	GPIO0 Input Status Detection 0 = Input Low (default) 1 = Input High

REG0x4D: GPIO_IN1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3]	GPIO11_IN	0	R	GPIO11 Input Status Detection 0 = Input Low (default) 1 = Input High
D[2]	GPIO10_IN	0	R	GPIO10 Input Status Detection 0 = Input Low (default) 1 = Input High
D[1]	GPIO9_IN	0	R	GPIO9 Input Status Detection 0 = Input Low (default) 1 = Input High
D[0]	GPIO8_IN	0	R	GPIO8 Input Status Detection 0 = Input Low (default) 1 = Input High

REGISTER MAP (continued)

REG0x4E: GPIO_OD0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	GPIO7_OD	0	R/W	GPIO7 Open-Drain Output Enable 0 = Disable (default) 1 = Enable
D[6]	GPIO6_OD	0	R/W	GPIO6 Open-Drain Output Enable 0 = Disable (default) 1 = Enable
D[5]	GPIO5_OD	0	R/W	GPIO5 Open-Drain Output Enable 0 = Disable (default) 1 = Enable
D[4]	GPIO4_OD	0	R/W	GPIO4 Open-Drain Output Enable 0 = Disable (default) 1 = Enable
D[3]	GPIO3_OD	0	R/W	GPIO3 Open-Drain Output Enable 0 = Disable (default) 1 = Enable
D[2]	GPIO2_OD	0	R/W	GPIO2 Open-Drain Output Enable 0 = Disable (default) 1 = Enable
D[1]	GPIO1_OD	0	R/W	GPIO1 Open-Drain Output Enable 0 = Disable (default) 1 = Enable
D[0]	GPIO0_OD	0	R/W	GPIO0 Open-Drain Output Enable 0 = Disable (default) 1 = Enable

REG0x4F: GPIO_OD1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R	Reserved
D[3]	GPIO11_OD	0	R/W	GPIO11 Open-Drain Output Enable 0 = Disable (default) 1 = Enable
D[2]	GPIO10_OD	0	R/W	GPIO10 Open-Drain Output Enable 0 = Disable (default) 1 = Enable
D[1]	GPIO9_OD	0	R/W	GPIO9 Open-Drain Output Enable 0 = Disable (default) 1 = Enable
D[0]	GPIO8_OD	0	R/W	GPIO8 Open-Drain Output Enable 0 = Disable (default) 1 = Enable

REGISTER MAP (continued)

REG0x50: GPIO_PP0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	GPIO3_PP[1:0]	00	R/W	Mode Selection with GPIO3 as Input Pin 00 = High resistance (default) 01 = Weak pull-down 10 = Weak pull-up 11 = Hold
D[5:4]	GPIO2_PP[1:0]	00	R/W	Mode Selection with GPIO2 as Input Pin 00 = High resistance (default) 01 = Weak pull-down 10 = Weak pull-up 11 = Hold
D[3:2]	GPIO1_PP[1:0]	00	R/W	Mode Selection with GPIO1 as Input Pin 00 = High resistance (default) 01 = Weak pull-down 10 = Weak pull-up 11 = Hold
D[1:0]	GPIO0_PP[1:0]	00	R/W	Mode Selection with GPIO0 as Input Pin 00 = High resistance (default) 01 = Weak pull-down 10 = Weak pull-up 11 = Hold

REG0x51: GPIO_PP1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	GPIO7_PP[1:0]	00	R/W	Mode Selection with GPIO7 as Input Pin 00 = High resistance (default) 01 = Weak pull down 10 = Weak pull-up 11 = Hold
D[5:4]	GPIO6_PP[1:0]	00	R/W	Mode Selection with GPIO6 as Input Pin 00 = High resistance (default) 01 = Weak pull-down 10 = Weak pull-up 11 = Hold
D[3:2]	GPIO5_PP[1:0]	00	R/W	Mode Selection with GPIO5 as Input Pin 00 = High resistance (default) 01 = Weak pull-down 10 = Weak pull-up 11 = Hold
D[1:0]	GPIO4_PP[1:0]	00	R/W	Mode Selection with GPIO4 as Input Pin 00 = High resistance (default) 01 = Weak pull-down 10 = Weak pull-up 11 = Hold

REGISTER MAP (continued)

REG0x52: GPIO_PP2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	GPIO11_PP[1:0]	00	R/W	Mode Selection with GPIO11 as Input Pin 00 = High resistance (default) 01 = Weak pull-down 10 = Weak pull-up 11 = Hold
D[5:4]	GPIO10_PP[1:0]	00	R/W	Mode Selection with GPIO10 as Input Pin 00 = High resistance (default) 01 = Weak pull-down 10 = Weak pull-up 11 = Hold
D[3:2]	GPIO9_PP[1:0]	00	R/W	Mode Selection with GPIO9 as Input Pin 00 = High resistance (default) 01 = Weak pull-down 10 = Weak pull-up 11 = Hold
D[1:0]	GPIO8_PP[1:0]	00	R/W	Mode Selection with GPIO8 as Input Pin 00 = High resistance (default) 01 = Weak pull-down 10 = Weak pull-up 11 = Hold

REG0x53: GPIO_DR Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	000000	R	Reserved
D[1:0]	DR[1:0]	00	R/W	Output Driver Capability Selection, Available to all GPIOs 00 = 2mA (default) 01 = 4mA 10 = 8mA 11 = 16mA

REGISTER MAP (continued)

REG0x54: MON_VSEL0 Register [Reset = 0x40]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R	Reserved
D[6]	GAIN	1	R/W	Voltage Gain Selection 0 = Voltage gain = 1 1 = Voltage gain = 1/4 (default)
D[5]	EN	0	R/W	0 = Disable internal voltage signal monitor function via MON0(default) 1 = Enable internal voltage signal monitor function via MON0
D[4:0]	VSEL[4:0]	00000	R/W	Select the Internal Voltage Signal to MON0 or MON1 00000 = N/A 00001 = Heater0 output voltage 00010 = Heater1 output voltage 00011 = Heater2 output voltage 00100 = Heater3 output voltage 00101 = Heater4 output voltage 00110 = Heater5 Output voltage 00111 = Heater6 output voltage 01000 = Heater7 output voltage 01001 = Heater8 output voltage 01010 = Heater9 output voltage 01011 = Heater10 output voltage 01100 = Heater11 output voltage 01101 = IBIAS0 output voltage 01110 = IBIAS1 output voltage 01111 = IBIAS2 output voltage 10000 = IBIAS3 output voltage 10001 = VDRIVE 10010 = PVDD0 10011 = VDD 10100 = VIO Others = N/A

REG0x55: MON_VSEL1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R	Reserved
D[5]	EN	0	R/W	0 = Disable internal voltage signal monitor function via MON1 1 = Enable internal voltage signal monitor function via MON1
D[4:0]	Reserved	00000	R	Reserved

REGISTER MAP (continued)

REG0x56: MON_GAIN32 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	MIO_GAIN32_LOW8[7]	0	R/W	MULTI_IO7 Current Gain Selection 0 = Gain = 1 (default) 1 = Gain = 32
D[6]	MIO_GAIN32_LOW8[6]	0	R/W	MULTI_IO6 Current Gain Selection 0 = Gain = 1 (default) 1 = Gain = 32
D[5]	MIO_GAIN32_LOW8[5]	0	R/W	MULTI_IO5 Current Gain Selection 0 = Gain = 1 (default) 1 = Gain = 32
D[4]	MIO_GAIN32_LOW8[4]	0	R/W	MULTI_IO4 Current Gain Selection 0 = Gain = 1 (default) 1 = Gain = 32
D[3]	MIO_GAIN32_LOW8[3]	0	R/W	MULTI_IO3 Current Gain Selection 0 = Gain = 1 (default) 1 = Gain = 32
D[2]	MIO_GAIN32_LOW8[2]	0	R/W	MULTI_IO2 Current Gain Selection 0 = Gain = 1 (default) 1 = Gain = 32
D[1]	MIO_GAIN32_LOW8[1]	0	R/W	MULTI_IO1 Current Gain Selection 0 = Gain = 1 (default) 1 = Gain = 32
D[0]	MIO_GAIN32_LOW8[0]	0	R/W	MULTI_IO0 Current Gain Selection 0 = Gain = 1 (default) 1 = Gain = 32

REG0x57: MON_CTRL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000	R	Reserved
D[4]	MIO_HIGH4_MON0	0	R/W	1 = Send MULTI_IO8~11 to MON0 0 = Send MULTI_IO8~11 to MON1 (default)
D[3]	MIO8_GAIN32_HIGH4[3]	0	R/W	MULTI_IO11 Current Gain Selection 0 = Gain = 1 (default) 1 = Gain = 32
D[2]	MIO8_GAIN32_HIGH4[2]	0	R/W	MULTI_IO10 Current Gain Selection 0 = Gain = 1 (default) 1 = Gain = 32
D[1]	MIO8_GAIN32_HIGH4[1]	0	R/W	MULTI_IO9 Current Gain Selection 0 = Gain = 1 (default) 1 = Gain = 32
D[0]	MIO8_GAIN32_HIGH4[0]	0	R/W	MULTI_IO8 Current Gain Selection 0 = Gain = 1 (default) 1 = Gain = 32

REGISTER MAP (continued)

REG0x58: MON_MSEL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	SEL_MUX1[2:0]	000	R/W	Select one of MULTI_IO11~8 sent to MON0/1 000 = MULTI_IO8 is sent to MON0/1 001 = MULTI_IO9 is sent to MON0/1 010 = MULTI_IO10 is sent to MON0/1 011 = MULTI_IO11 is sent to MON0/1 100 = N/A 101 = N/A 110 = N/A 111 = N/A
D[4:2]	SEL_MUX0[2:0]	000	R/W	Select one of MULTI_IO7~0 to send to MON0 0: MULTI_IO0 to MON0 000 = MULTI_IO0 is sent to MON0 001 = MULTI_IO1 is sent to MON0 010 = MULTI_IO2 is sent to MON0 011 = MULTI_IO3 is sent to MON0 100 = MULTI_IO4 is sent to MON0 101 = MULTI_IO5 is sent to MON0 110 = MULTI_IO6 is sent to MON0 111 = MULTI_IO7 is sent to MON0
D[1]	EN_MUX1	0	R/W	Enable MULTI_IO8~11 sent to MON0/1
D[0]	EN_MUX0	0	R/W	Enable MULTI_IO7~0 sent to MON0

REG0xA4: MISC_CTRL1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	000000	R	Reserved
D[1:0]	SPI_DR	00	R/W	SPI SDO/I^2C SDA Driver Ability Configuration 00 = 2mA (default) 01 = 4mA 10 = 8mA 11 = 16mA

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JUNE 2026 – REV.A to REV.A.1 **Page**

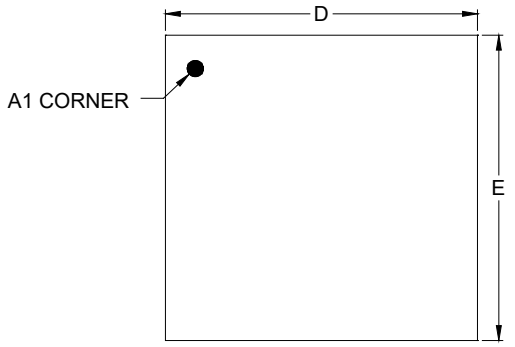
Updated the MULTI_IOx Pin Applications and Figure 6 15-16
Updated the REG0x12 27

Changes from Original to REV.A (SEPTEMBER 2025) **Page**

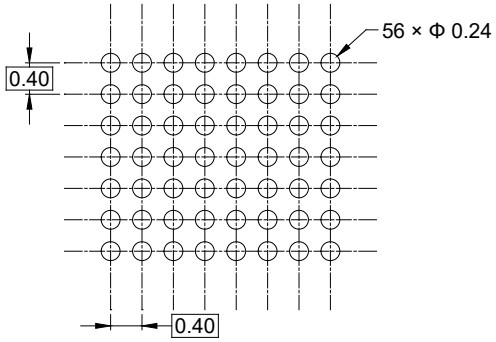
Changed from product preview to production data ..... All

PACKAGE OUTLINE DIMENSIONS

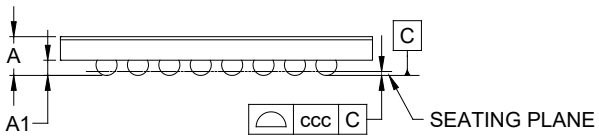
WLCSP-3.98×3.89-56B



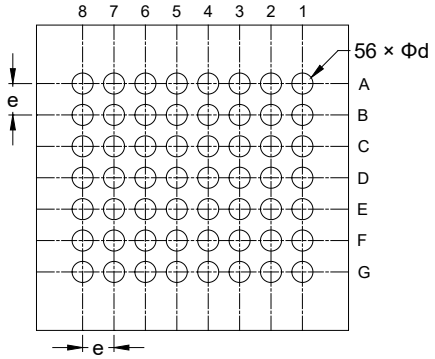
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



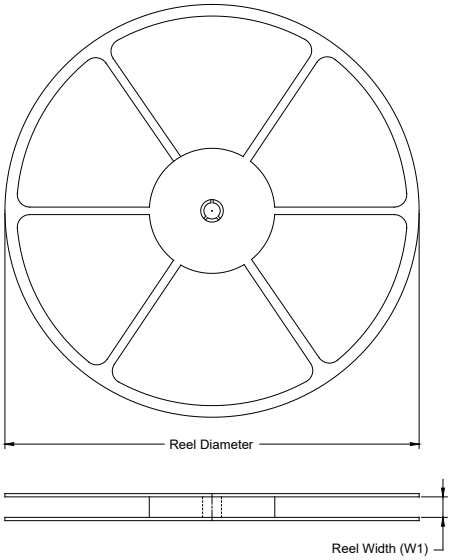
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.532
A1	0.174	-	0.214
D	3.945	-	4.005
E	3.860	-	3.920
d	0.238	-	0.298
e	0.400 BSC		
ccc	0.050		

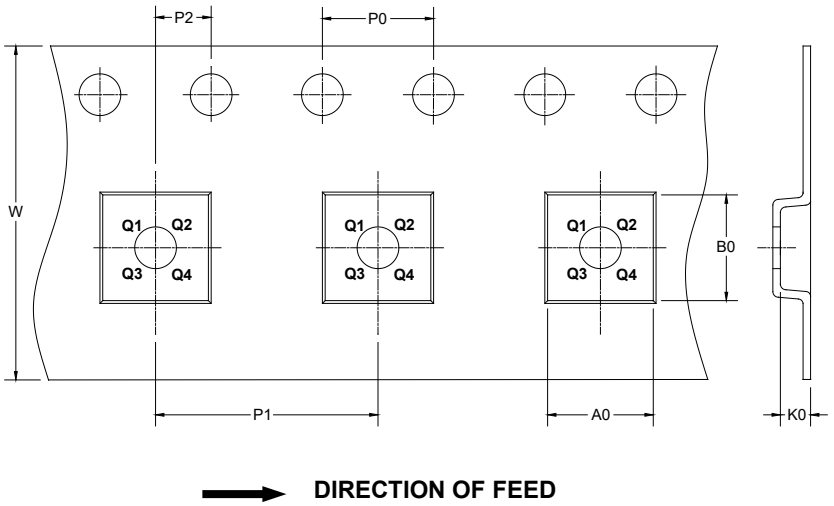
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



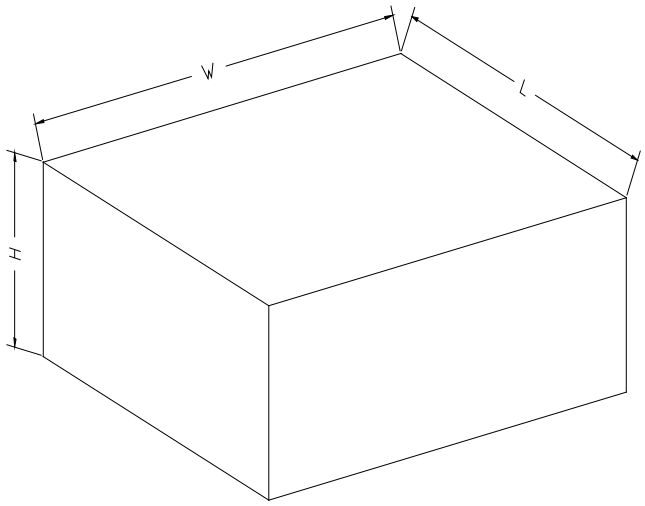
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	MPQ	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-3.98×3.89-56B	13"	7000	12.4	4.23	4.23	0.78	4.0	8.0	2.0	12.0	Q1
WLCSP-3.98×3.89-56B	7"	1000	12.4	4.23	4.23	0.78	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002