SGM38049
Triple Output AMOLED Display Power Supply

GENERAL DESCRIPTION

The SGM38049 is designed for powering AMOLED displays which requires V_{ELVDD}, V_{ELVSS} and V_{AVDD}. The device integrates a positive Buck-Boost converter with Single Inductor Dual Output (SIDO) topology for ELVDD and AVDD, and one inverting Buck-Boost converter for ELVSS.

The SGM38049 generates two positive and one negative precision regulated voltage power sources AVDD, ELVDD and ELVSS. The positive output ELVDD is programmable from 2.6V to 5V with 100mV per step, and the negative output ELVSS is programmable from -0.3V to -9.2V with 100mV per step. The combined ELVDD and ELVSS output capability is up to 250mA. The AVDD is programmable from 2.7V to 3.6V with 100mV per step and 30mA output capability.

The SGM38049 is available in a Green WLCSP-1.72×2.2-20B package. It operates over an ambient temperature range of -40℃ to +85℃.

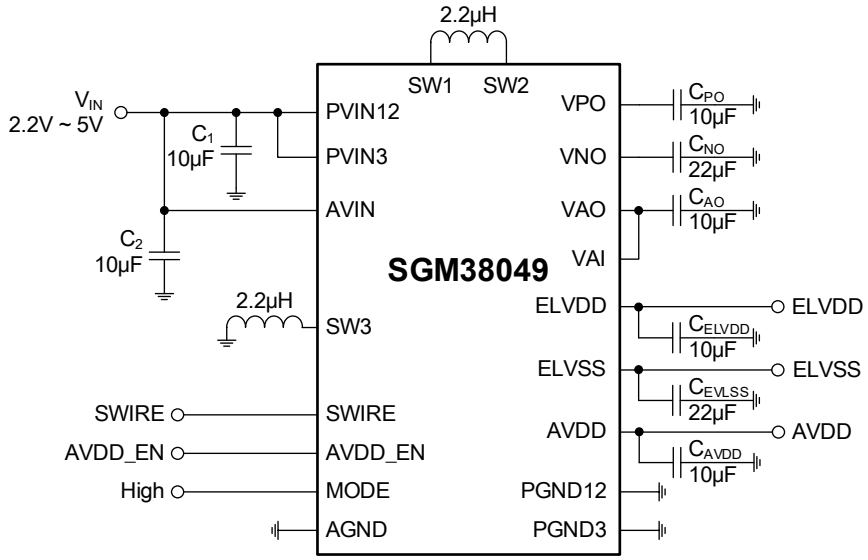
FEATURES

- **High Efficiency in Wide Output Loading Range**
- **Pulse-Skip Operation in Light Load Condition**
- **Positive Buck-Boost Converter with SIDO Topology**
- **Programmable Outputs with SWIRE Interface**
  V_{ELVDD} = 2.6V to 5.0V (100mV/Step, ±0.5% Accuracy)
  V_{ELVSS} = -0.3V to -9.2V (100mV/Step, ±0.5% Accuracy)
  V_{AVDD} = 2.7V to 3.6V (100mV/Step, ±0.5% Accuracy)
- **250mA Output Current @V_{IN} = 2.7V, V_{ELVSS} = -6V**
- **200mA Output Current @V_{IN} = 2.7V, V_{ELVSS} = -9V**
- **30mA Output Current for AVDD**
- **Configurable Active Discharge**
- **Internal Soft-Start to Limit Inrush Current**
- **Over-Temperature Protection (OTP)**
- **Over-Current Protection (OCP)**
- **Short-Circuit Protection (SCP)**
- **Available in a Green WLCSP-1.72×2.2-20B Package**

APPLICATIONS

Tiny Size AMOLED Displays
Wearable AMOLED Products

TYPICAL APPLICATION



MODE = Low, VAI = External Power Supply, connect VAI to external power supply;
MODE = High, VAI = VAO, connect VAI to VAO;
MODE = Floating, VAI = VPO, connect VAI to VPO.

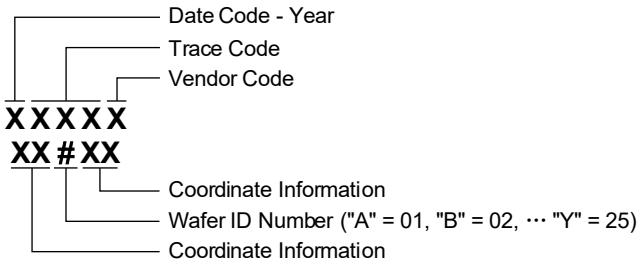
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM38049	WLCSP-1.72×2.2-20B	-40℃ to +85℃	SGM38049YG/TR	38049 XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

PVIN12, PVIN3, AVIN, VAI Voltages ..... -0.3V to 6V
SWIRE, AVDD_EN, MODE Voltages ..... -0.3V to 6V
VAO, VPO, AVDD, ELVDD Voltages ..... -0.3V to 6V
SW1, SW2 Voltages ..... -0.3V to 6V
SW1, SW2 Voltages (Transient: 10ns) ..... -1V to 7V
VNO, ELVSS Voltages ..... -10V to 0.3V
SW3 Voltage ..... -10V to 6V
SW3 Voltage (Transient: 10ns) ..... -12V to 7V
Package Thermal Resistance
WLCSP-1.72×2.2-20B, θ_{JA} ..... 41.5℃/W
WLCSP-1.72×2.2-20B, θ_{JB} ..... 6.6℃/W
WLCSP-1.72×2.2-20B, θ_{JC} ..... 17.5℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±3000V
CDM ..... ±1500V

NOTES:
1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 2.2V to 5V
Operating Ambient Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

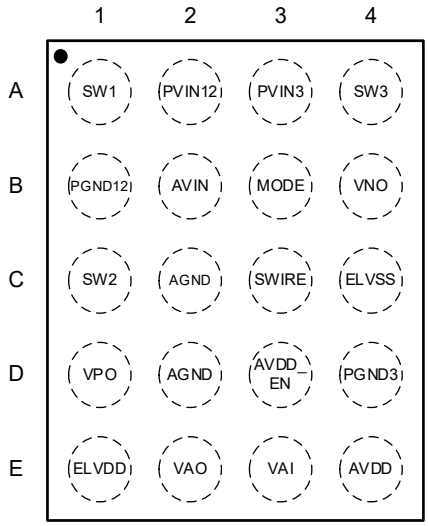
RECOMMENDED COMPONENTS OF TEST CIRCUITS

Table 1. Recommended BOM for Typical Applications

Reference	Value	Number	Electrical Spec	Part Number	Manufacturer
L_1, L_2	2.2μH	2	I_{TEMP} = 1.7A, I_{SAT} = 2.4A, 140mΩ, 201610	DFE201610E-2R2M=P2	Murata
C_1, C_2, C_{PO}, C_{AO}, C_{ELVDD}, C_{AVDD}	10μF	6	X5R, 6.3V, 0402	GRM155R60J106ME44D	Murata
C_{NO}, C_{ELVSS}	22μF	2	X5R, 16V, 0603	GRM188C61C226ME01	Murata

PIN CONFIGURATION

(TOP VIEW)



WLCSP-1.72×2.2-20B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1	SW1	I/O	Positive Buck-Boost Converter Switching Node 1.
A2	PVIN12	P	Positive Buck-Boost Converter Power Supply Input Pin.
A3	PVIN3	P	ELVSS Inverting Buck-Boost Converter Power Supply Input Pin.
A4	SW3	I/O	ELVSS Inverting Buck-Boost Converter Switching Node.
B1	PGND12	G	Positive Buck-Boost Converter Power Ground.
B2	AVIN	P	Analog Power Supply.
B3	MODE	I	Mode Select Pin. MODE = Low, VAI = External Power Supply, connect VAI to external power supply; MODE = High, VAI = VAO, connect VAI to VAO; MODE = Floating, VAI = VPO, connect VAI to VPO.
B4	VNO	O	ELVSS Inverting Buck-Boost Converter Output Pin.
C1	SW2	I/O	Positive Buck-Boost Converter Switching Node 2.
C2, D2	AGND	G	Analog Ground Pin.
C3	SWIRE	I	SWIRE Interface Input.
C4	ELVSS	O	Linear Regulator Output ELVSS.
D1	VPO	O	Positive Buck-Boost Converter Output 2.
D3	AVDD_EN	I	AVDD Enable Control Pin.
D4	PGND3	G	Inverting Buck-Boost Converter Power Ground.
E1	ELVDD	O	Linear Regulator Output ELVDD.
E2	VAO	O	Positive Buck-Boost Converter Output 1.
E3	VAI	P	Linear Regulator Output AVDD Power Supply Pin.
E4	AVDD	O	Linear Regulator Output AVDD.

NOTE: I = input, O = output, I/O = input/output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(T_J = +25℃, V_{IN} = 3.8V, SWIRE = AVDD_EN = V_{IN}, V_{AVDD} = 3.3V, V_{ELVDD} = 3.3V, V_{ELVSS} = -3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		2.2		5	V
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising, initial accuracy		2.1	2.2	V
		V_{IN} falling, initial accuracy		2	2.1	
VIN Supply Current (All Channels on) (1)	I_{Q_ALL}	V_{IN} = 2.2V to 5V, all channels on, VAI = external power (V_{VAI} = V_{AVDD} + 0.1V), switching, no load		28	55	μA
		V_{IN} = 2.2V to 5V, all channels on, VAI = VAO, switching, no load		35	60	
		V_{IN} = 2.2V to 5V, all channels on, VAI = VPO, switching, no load		33	60	
VIN Supply Current (AVDD on only) (1)	I_{Q_AVDD}	V_{IN} = 2.2V to 5V, AVDD on only, VAI = external power (V_{VAI} = V_{AVDD} + 0.1V), no load		3	12	μA
		V_{IN} = 2.2V to 5V, AVDD on only, VAI = VAO, no load		10	25	
		V_{IN} = 2.2V to 5V, AVDD on only, VAI = VPO, no load		12	25	
Shutdown Current	I_{OFF}	V_{IN} = 2.2V to 5V, all channel off, initial accuracy		0.3	1	μA
Thermal Shutdown Temperature (1)	T_{SD}	Junction temperature rising	140	145		℃
Thermal Shutdown Hysteresis (2)	T_{SD_HYS}		20	25		℃
Single Inductor Dual Output Positive Buck-Boost Converter (SIDO)						
Switching Frequency	f_{SW12}	PWM mode with spread spectrum	0.8	1	1.25	MHz
Inductor Current Limit	I_{PEAK12}	Peak current limit	1.1	1.7		A
Positive Output AVDD Voltage Range	V_{AVDD}	2.7V to 3.6V with 100mV/step, default 3.3V	2.7	3.3	3.6	V
Positive Output AVDD Voltage Initial Accuracy	V_{AVDD_ACC}	V_{PVIN12} = 2.2V to 5V, V_{AVDD} = 2.7V to 3.6V, no load	-0.5		0.5	%
AVDD Current Capability (2)	I_{AVDD_MAX}		30			mA
Short-Circuit Threshold in Operation	V_{SCP_AVDD}		80	85	90	%
Discharge Resistor of Positive Output	R_{DIS_AVDD}			33		Ω
Discharge Time of AVDD (1) (3)	t_{DIS_AVDD}			0.5		ms
AVDD Ripple (1)	V_{RIPPLE_AVDD}	V_{IN} = 2.2V to 5V, I_{AVDD} = 0mA to 30mA		10		mV_{PP}
AVDD_LDO Drop Voltage Requirement	V_{DROP_AVDD}	VAI = external power	100			mV
Load Transient (1)	$V_{LOADTRS_AVDD}$	V_{IN} = 2.2V to 5V, VAI = external power, V_{AVDD} = 3.3V, I_{AVDD} = 20μA to 10mA, t_R = t_F = 50μs		10		mV_{PP}
		V_{IN} = 2.2V to 5V, VAI = VAO, V_{AVDD} = 3.3V, I_{AVDD} = 20μA to 10mA, t_R = t_F = 50μs		10		
		V_{IN} = 2.2V to 5V, VAI = VPO, V_{AVDD} = 3.3V, I_{AVDD} = 20μA to 10mA, t_R = t_F = 50μs		10		
Line Transient (1)	$V_{LINETRS_AVDD}$	V_{IN} = 2.2V to 5V, VAI = external power, ΔV_{VAI} = 500mV, t_R = 10μs, t_F = 10μs, V_{AVDD} = 3.3V, I_{AVDD} = 0mA to 30mA		4		mV_{PP}
		V_{IN} = 2.2V to 5V, VAI = VAO, ΔV_{IN} = 900mV, t_R = 20μs, t_F = 6μs, V_{AVDD} = 3.3V, I_{AVDD} = 0mA to 30mA		10		
		V_{IN} = 2.2V to 5V, VAI = VPO, ΔV_{IN} = 900mV, t_R = 20μs, t_F = 6μs, V_{AVDD} = 3.3V, I_{AVDD} = 0mA to 30mA		12		
Load Regulation (1)	$V_{LOADREGU_AVDD}$	V_{IN} = 3.8V, V_{AVDD} = 3.3V, I_{AVDD} = 0mA to 30mA		0.1		%
Line Regulation (1)	$V_{LINEREGU_AVDD}$	V_{PVIN12} = 2.2V to 5V, V_{AVDD} = 3.3V, I_{AVDD} = 10mA		0.1		%
Positive Output ELVDD Voltage Range	V_{ELVDD}	2.6V to 5V with 100mV/step, default 3.3V	2.6	3.3	5	V
Positive Output ELVDD Voltage Initial Accuracy	V_{ELVDD_ACC}	V_{PVIN12} = 2.2V to 5V, V_{ELVDD} = 2.6V to 5V, no load	-0.5		0.5	%

ELECTRICAL CHARACTERISTICS (continued)

(T_J = +25℃, V_{IN} = 3.8V, SWIRE = AVDD_EN = V_{IN}, V_{AVDD} = 3.3V, V_{ELVDD} = 3.3V, V_{ELVSS} = -3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ELVDD Current Capability (2)	I_{ELVDD_MAX}	V_{IN} = 2.2V to 2.7V	100			mA
		V_{IN} = 2.7V to 5V	200			
Short-Circuit Threshold in Operation	V_{SCP_ELVDD}		80	85	90	%
Discharge Resistor of Positive Output	R_{DIS_ELVDD}			33		Ω
Discharge Time of ELVDD (1) (3)	t_{DIS_ELVDD}			0.5		ms
ELVDD Ripple (1)	V_{RIPPLE_ELVDD}	V_{PVIN12} = 2.2V to 5V, I_{ELVDD} = 0mA to 200mA		10		mV_{PP}
Load Transient (1)	$V_{LOADTRS_ELVDD}$	V_{IN} = 2.2V to 2.7V, I_{ELVDD} = 1mA to 100mA, t_R = t_F = 5ms		10		mV_{PP}
		V_{IN} = 2.7V to 5V, I_{ELVDD} = 1mA to 200mA, t_R = t_F = 5ms		10		
Line Transient (1)	$V_{LINETRS_ELVDD}$	V_{IN} = 2.2V to 2.7V, ΔV_{IN} = 900mV, t_R = 20μs, t_F = 6μs, I_{ELVDD} = 0mA to 100mA		15		mV_{PP}
		V_{IN} = 2.7V to 5V, ΔV_{IN} = 900mV, t_R = 20μs, t_F = 6μs, I_{ELVDD} = 0mA to 200mA		20		
Load Regulation (1)	$V_{LOADREGU_ELVDD}$	V_{IN} = 3.8V, V_{ELVDD} = 3.3V, I_{ELVDD} = 0mA to 200mA		0.1		%
Line Regulation (1)	$V_{LINEREGU_ELVDD}$	V_{PVIN12} = 2.2V to 5V, V_{ELVDD} = 3.3V, I_{ELVDD} = 1mA		0.1		%
Inverting Buck-Boost Converter ELVSS						
Switching Frequency	f_{SW3}	PWM mode with spread spectrum	0.8	1	1.25	MHz
Inductor Peak Current	I_{PEAK3}	Peak current limit	1.8	2.3		A
Negative Output Voltage Range	V_{ELVSS}	-9.2V to -0.3V with 100mV/step, default -3.3V	-9.2	-3.3	-0.3	V
Negative Output ELVSS Voltage Initial Accuracy	V_{ELVSS_ACC}	V_{PVIN3} = 2.2V to 5V, V_{ELVSS} = -0.3V to -0.5V, no load	-15		15	mV
		V_{PVIN3} = 2.2V to 5V, V_{ELVSS} = -0.5V to -4V, no load	-20		20	mV
		V_{PVIN3} = 2.2V to 5V, V_{ELVSS} = -4V to -9V, no load	-0.8		0.8	%
Negative Current Capability (2)	I_{ELVSS_MAX}	V_{IN} = 2.2V to 5V, V_{ELVSS} = -0.3V to -0.5V	100			mA
		V_{IN} = 2.2V to 2.7V, V_{ELVSS} = -0.5V to -9V	100			
		V_{IN} = 2.7V to 5V, V_{ELVSS} = -0.5V to -9V	200			
Short-Circuit Threshold in Operation	V_{SCP_ELVSS}		75	80	85	%
Discharge Resistor of Negative Output	R_{DIS_ELVSS}			65		Ω
Discharge Time of Negative Output (1) (3)	t_{DIS_ELVSS}			2.5		ms
ELVSS Ripple (1)	V_{RIPPLE_ELVSS}	V_{PVIN12} = 2.2V to 2.7V, I_{ELVDD} = 0mA to 100mA		10		mV_{PP}
		V_{PVIN12} = 2.7V to 5V, I_{ELVDD} = 0mA to 200mA		10		
Load Transient (1)	$V_{LOADTRS_ELVSS}$	V_{IN} = 2.2V to 2.7V, I_{ELVSS} = 1mA to 100mA, t_R = t_F = 5ms		10		mV_{PP}
		V_{IN} = 2.7V to 5V, I_{ELVSS} = 1mA to 200mA, t_R = t_F = 5ms		10		
Line Transient (1)	$V_{LINETRS_ELVSS}$	V_{IN} = 2.2V to 2.7V, ΔV_{IN} = 900mV, t_R = 20μs, t_F = 6μs, I_{ELVSS} = 0mA to 100mA		25		mV_{PP}
		V_{IN} = 2.7V to 5V, ΔV_{IN} = 900mV, t_R = 20μs, t_F = 6μs, I_{ELVSS} = 0mA to 200mA		20		
Load Regulation (1)	$V_{LOADREGU_ELVSS}$	V_{IN} = 3.8V, V_{ELVSS} = -3.3V, I_{ELVSS} = 0mA to 200mA		0.1		%
Line Regulation (1)	$V_{LINEREGU_ELVSS}$	V_{PVIN3} = 2.2V to 5V, V_{ELVSS} = -3.3V, I_{ELVSS} = 1mA		0.1		%
Logic Signals (SWIRE, AVDD_EN, MODE)						
Low Level Input Voltage	V_{IL}	V_{IN} = 2.2V to 5V			0.35	V
High Level Input Voltage	V_{IH}	V_{IN} = 2.2V to 5V	0.8			V
SWIRE and AVDD_EN Pull-Down Resistors	R_{ENPD}	Logic low		580		kΩ
SWIRE and AVDD_EN Pin Leakage Current	I_{LEAK_EN}	Logic high		25	50	nA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = +25℃, V_{IN} = 3.8V, SWIRE = AVDD_EN = V_{IN}, V_{AVDD} = 3.3V, V_{ELVDD} = 3.3V, V_{ELVSS} = -3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AVDD_EN Initialization Time (1) (4) (5)	t_{AINIT}			200	900	μs
SWIRE Initialization Time (1) (4) (5)	t_{SINIT}				250	
SWIRE Shutdown Time Period (1) (6)	t_{OFF}				75	
SWIRE Data Storage/Accept Time Period (1) (7)	t_{STORE}				75	
Short-Circuit Timer						
AVDD Short-Circuit Detection Time in Start-Up	$t_{VO1(SCP)}$			3.6		ms
AVDD Short-Circuit Detection Time in Operation				3		
ELVDD Short-Circuit Detection Time in Start-Up	$t_{VO2(SCP)}$			1.8		
ELVDD Short-Circuit Detection Time in Operation				1.2		
ELVSS Short-Circuit Detection Time in Start-Up	$t_{VO3(SCP)}$			2.6		
ELVSS Short-Circuit Detection Time in Operation				1.2		
Power Sequence (8)						
VPO Start-Up Time	t_{SS1}			0.5	2	ms
ELVDD Start-Up Time	t_{SS2}			0.5	2	
VNO/ELVSS Start-Up Time	t_{SS3}			1	4.5	
VAO Start-Up Time	t_{SS4}			0.5	2	
AVDD Start-Up Time	t_{SS5}			0.5	2	

NOTES:

1. Guaranteed by design and lab test.
2. Guaranteed by design.
3. Discharge time from 90% to 10%.
4. Tested with standard power-on sequence: pull EN high first, and then pull SWIRE high.
5. The host must pull AVDD_EN high for a minimum of 900μs and SWIRE high for a minimum of 250μs to ensure proper power-on.
6. The host must pull SWIRE low for a minimum of 75μs to ensure proper power-off.
7. The host must keep SWIRE high for 75μs after the pulse ends to terminate the current communication.
8. Soft-start time from 10% to 90%.

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SWIRE Interface					
Pulse High Level Time Period (1)	t_{HIGH}	2	10	20	μs
Pulse Low Level Time Period (1)	t_{LOW}	2	10	20	
SWIRE Rising Time	t_R			100	ns
SWIRE Falling Time	t_F			100	

NOTE:

1. Tested with standard power-on sequence: pull EN high first, and then pull SWIRE high.

TIMING DIAGRAM

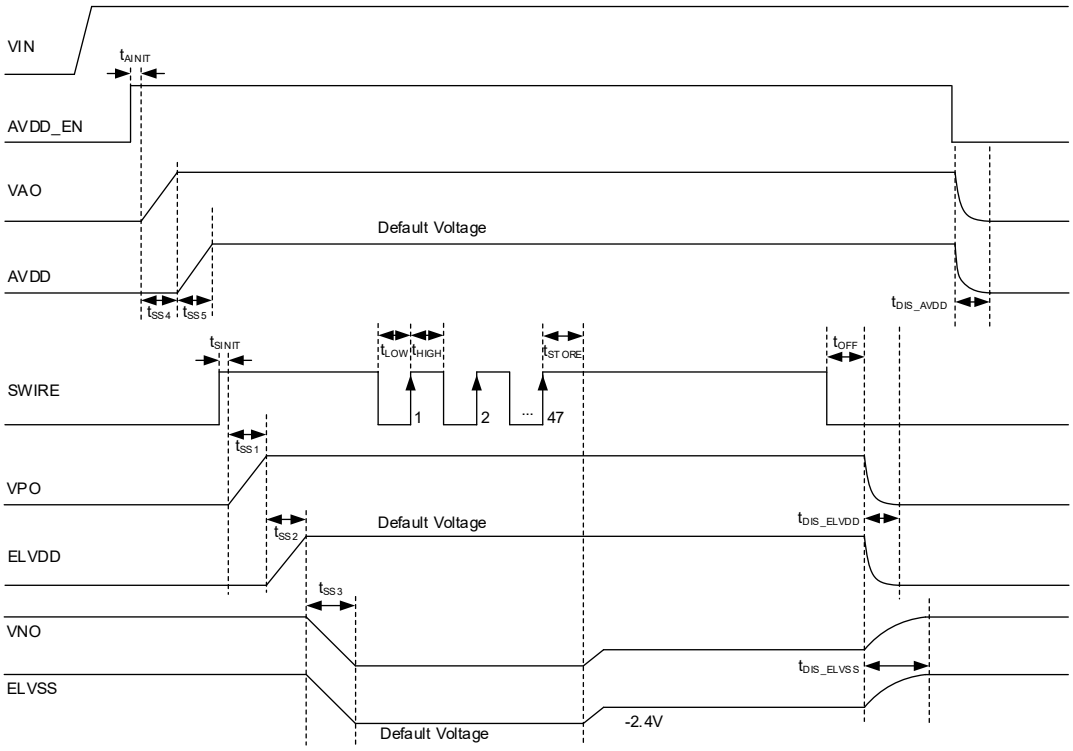


Figure 2. Timing Diagram (MODE = High, VAI = VAO)

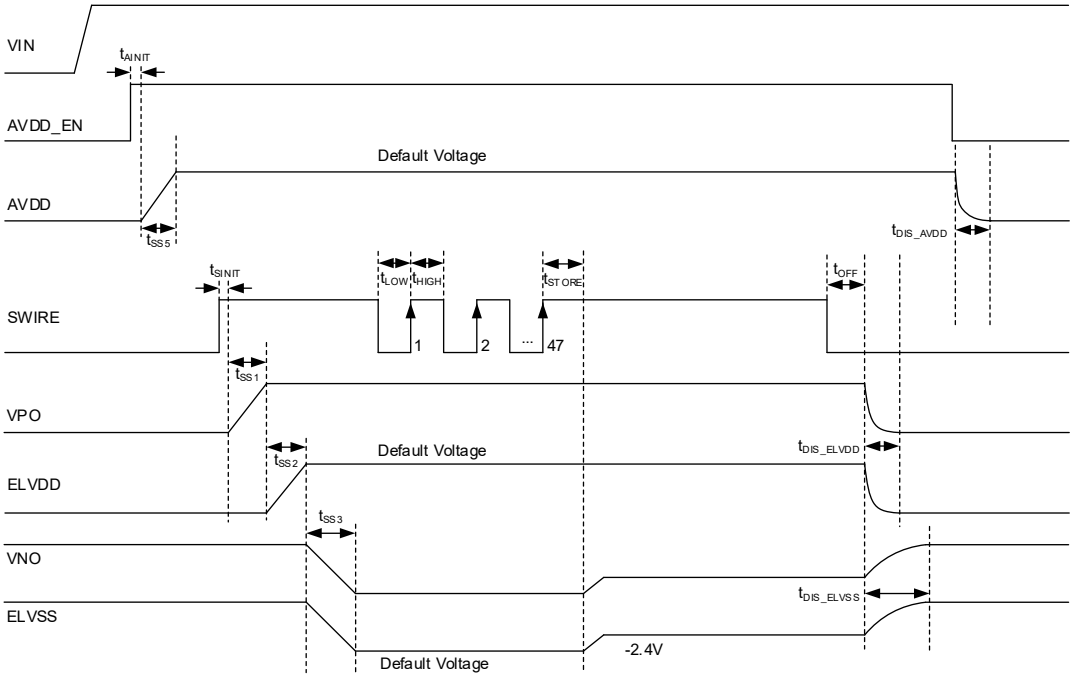


Figure 3. Timing Diagram (MODE = Low, VAI = External Power Supply)

TIMING DIAGRAM (continued)

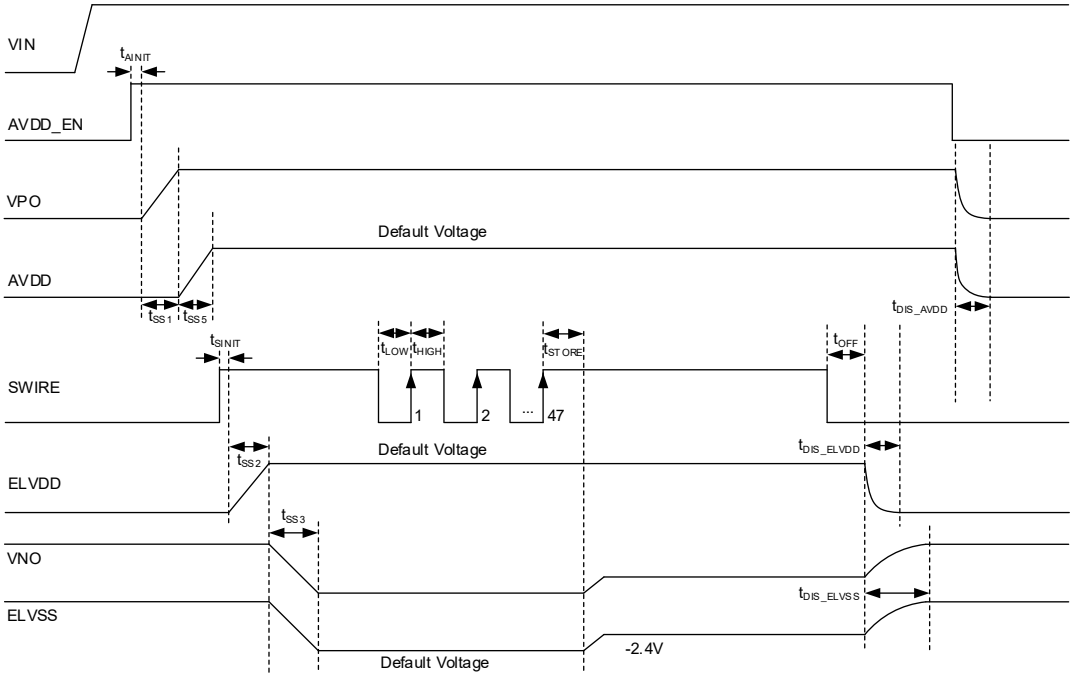
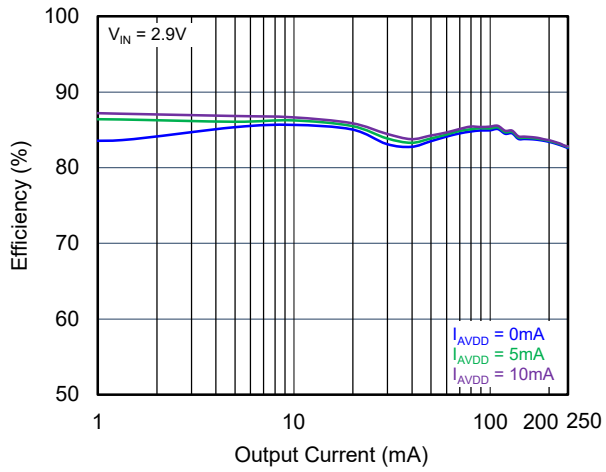


Figure 4. Timing Diagram (MODE = Floating, VAI = VPO)

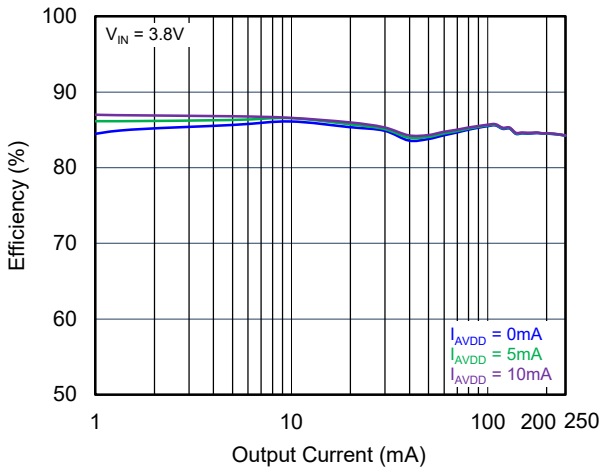
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8V, AVDD_EN = high, SWIRE = high, MODE = high, VAI = VAO, V_{AVDD} = 3.3V, V_{ELVDD} = 3.3V, V_{ELVSS} = -3.3V, unless otherwise noted.

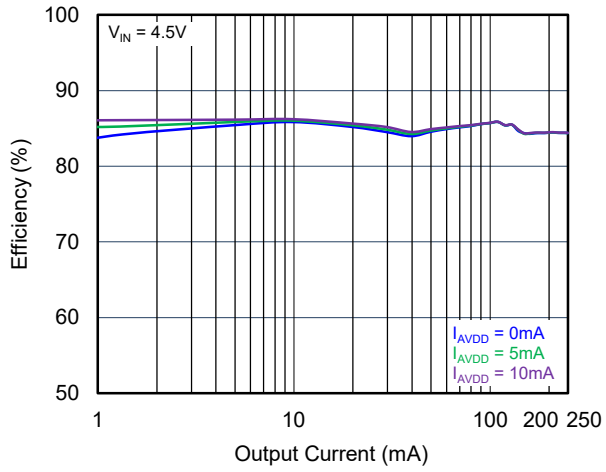
ELVDD and ELVSS Combined Efficiency vs. Output Current



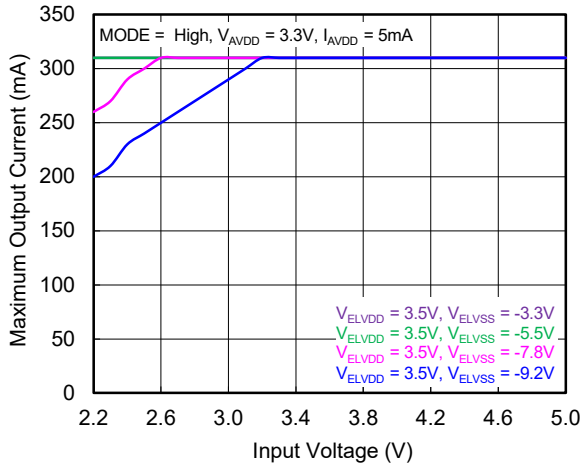
ELVDD and ELVSS Combined Efficiency vs. Output Current



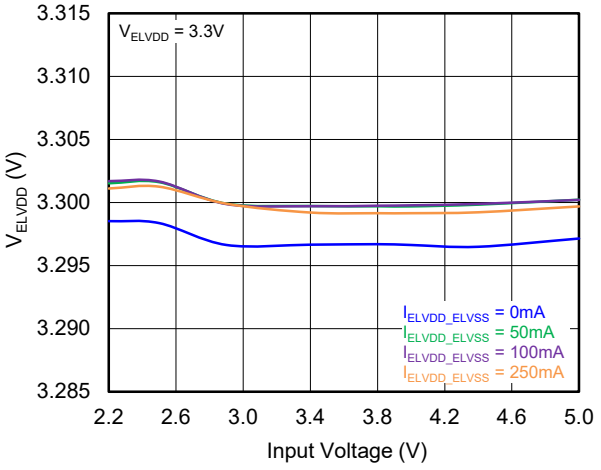
ELVDD and ELVSS Combined Efficiency vs. Output Current



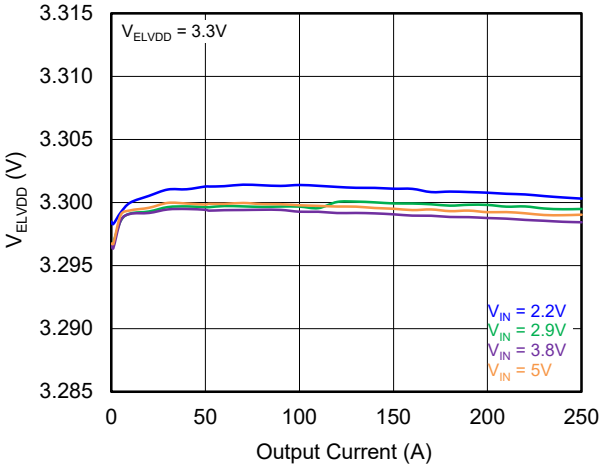
ELVDD and EVLSS Combined Maximum Output Current vs. Input Voltage



ELVDD Line Regulation



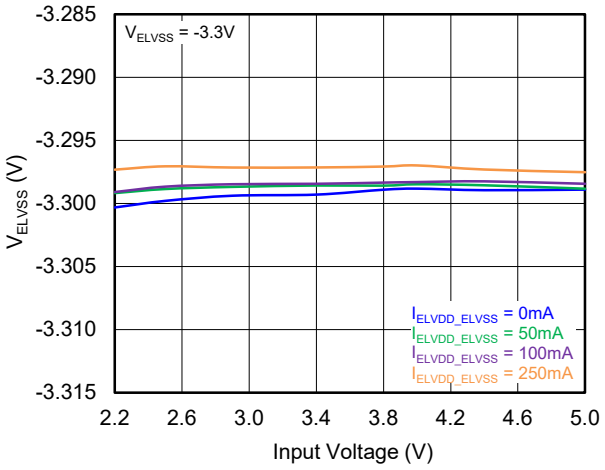
ELVDD Load Regulation



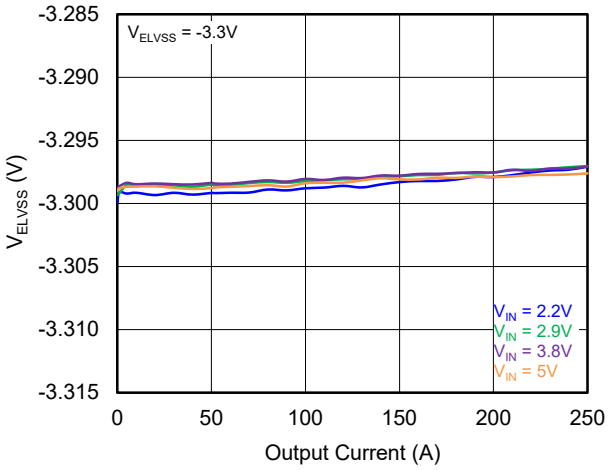
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.8V, AVDD_EN = high, SWIRE = high, MODE = high, VAI = VAO, V_{AVDD} = 3.3V, V_{ELVDD} = 3.3V, V_{ELVSS} = -3.3V, unless otherwise noted.

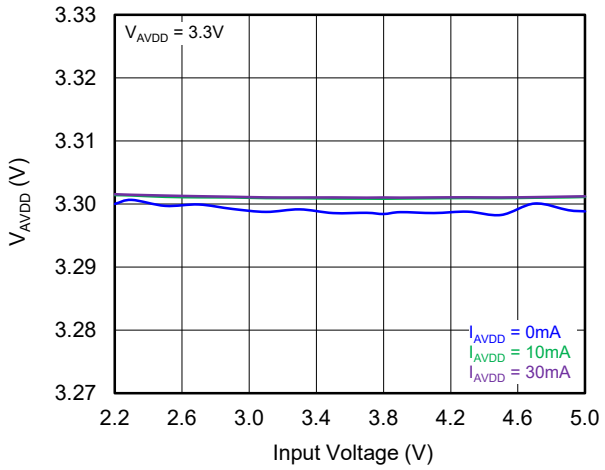
ELVSS Line Regulation



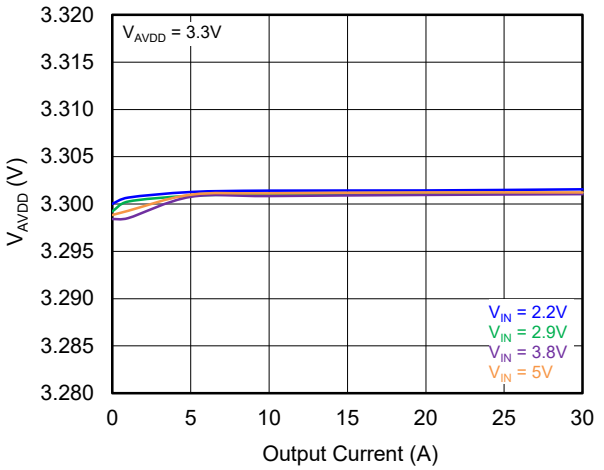
ELVSS Load Regulation



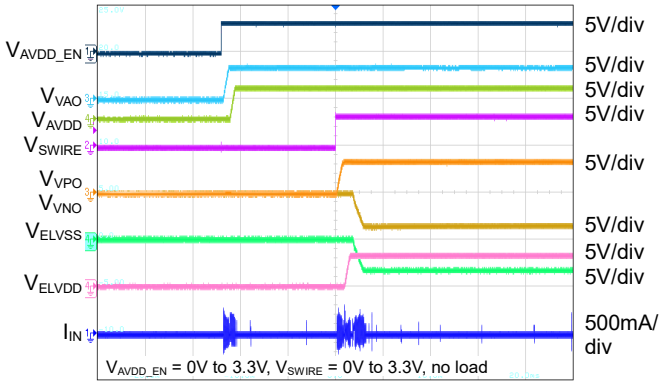
AVDD Line Regulation



AVDD Load Regulation

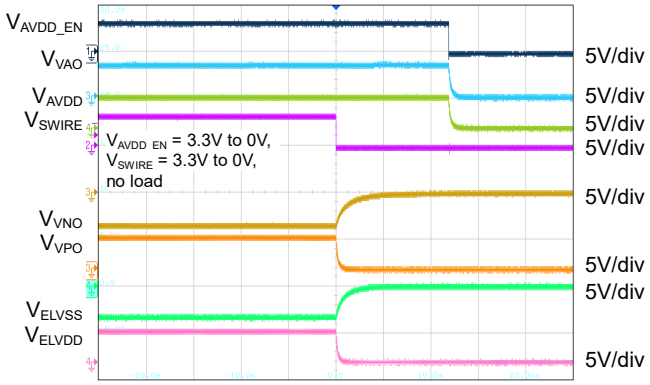


Startup Sequence - MODE = High, VAI = VAO



Time (5ms/div)

Shutdown Sequence - MODE = High, VAI = VAO

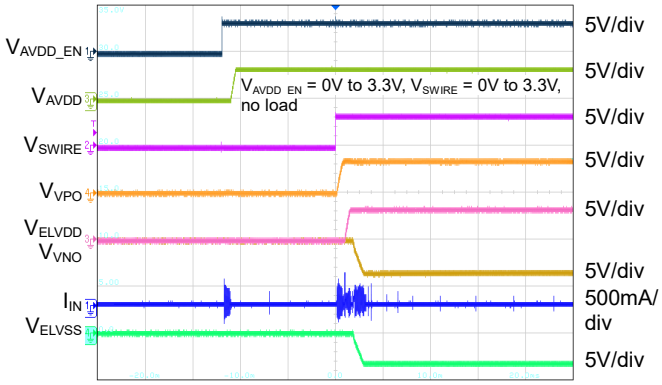


Time (5ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

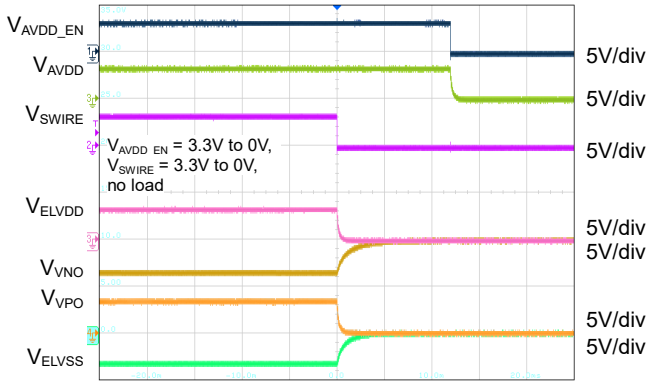
V_{IN} = 3.8V, AVDD_EN = high, SWIRE = high, MODE = high, VAI = VAO, V_{AVDD} = 3.3V, V_{ELVDD} = 3.3V, V_{ELVSS} = -3.3V, unless otherwise noted.

Startup Sequence - MODE = Low, VAI = External Power Supply



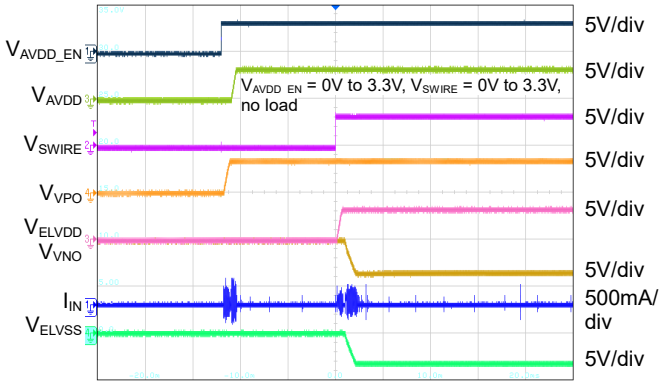
Time (5ms/div)

Shutdown Sequence - MODE = Low, VAI = External Power Supply



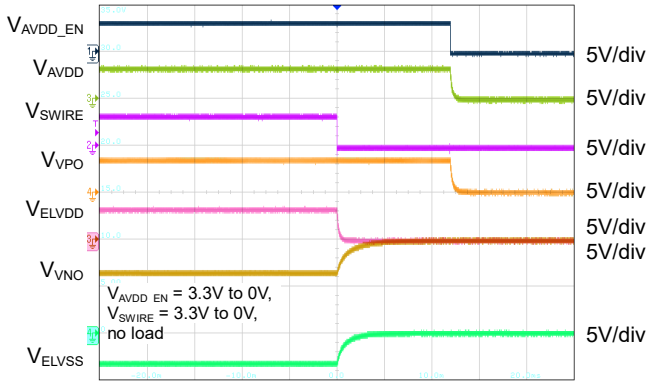
Time (5ms/div)

Startup Sequence - MODE = Floating, VAI = VPO



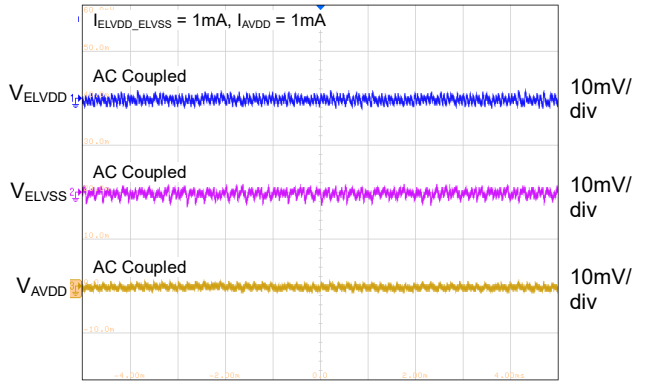
Time (5ms/div)

Shutdown Sequence - MODE = Floating, VAI = VPO



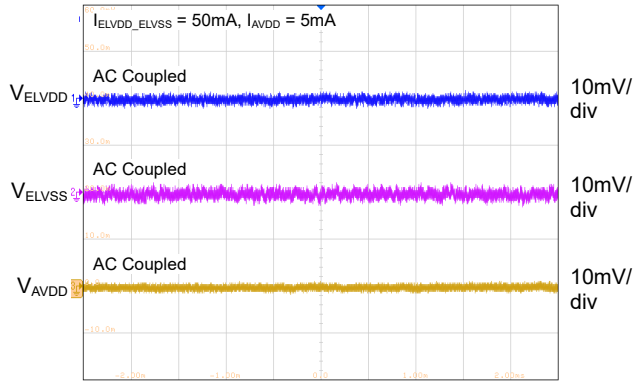
Time (5ms/div)

Output Ripple at Light Load



Time (1ms/div)

Output Ripple at Moderate Load

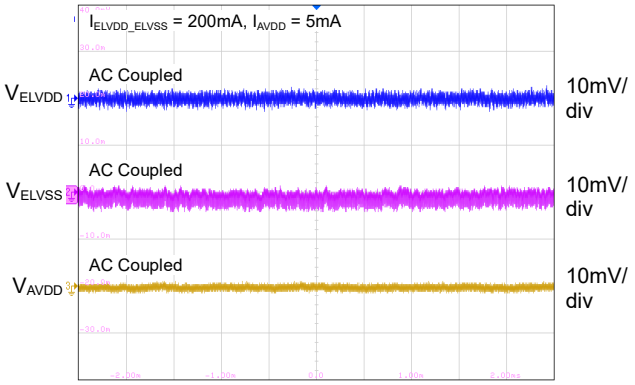


Time (500µs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

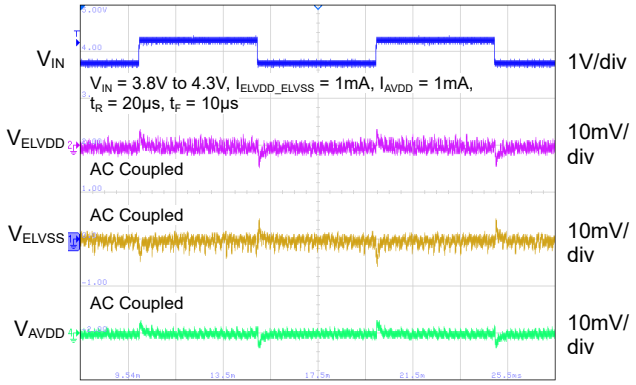
V_{IN} = 3.8V, AVDD_EN = high, SWIRE = high, MODE = high, VAI = VAO, V_{AVDD} = 3.3V, V_{ELVDD} = 3.3V, V_{ELVSS} = -3.3V, unless otherwise noted.

Output Ripple at Heavy Load



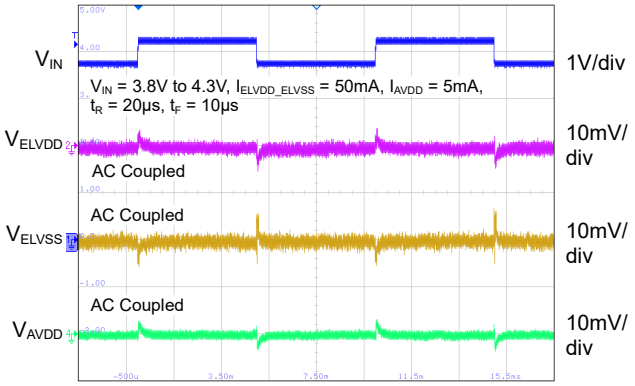
Time (500μs/div)

Line Transient at Light Load



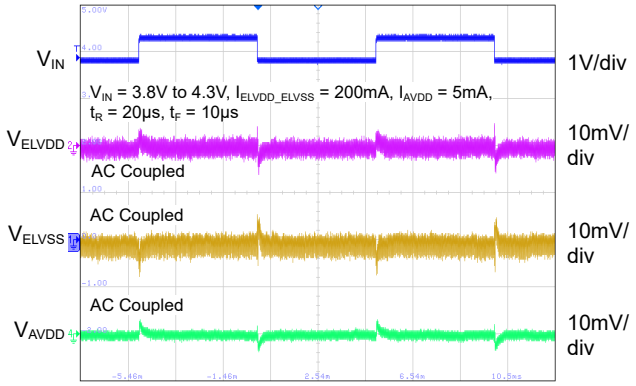
Time (2ms/div)

Line Transient at Moderate Load



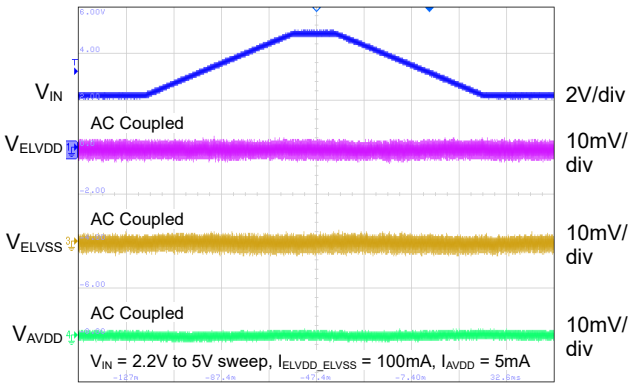
Time (2ms/div)

Line Transient at Heavy Load



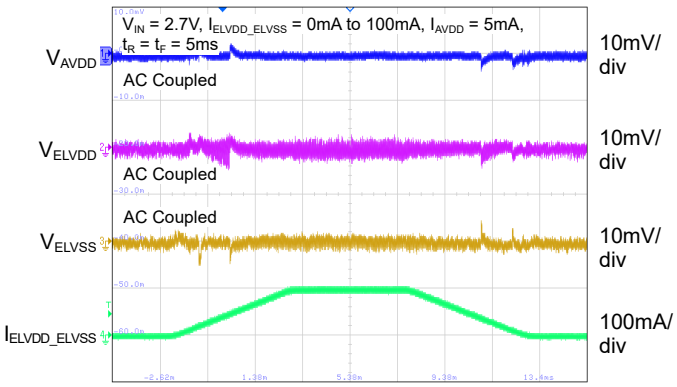
Time (2ms/div)

Line Sweep at Heavy Load



Time (20ms/div)

ELVDD and ELVSS Load Transient

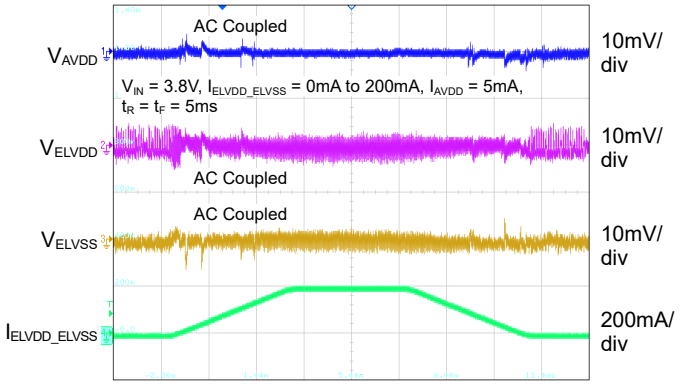


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

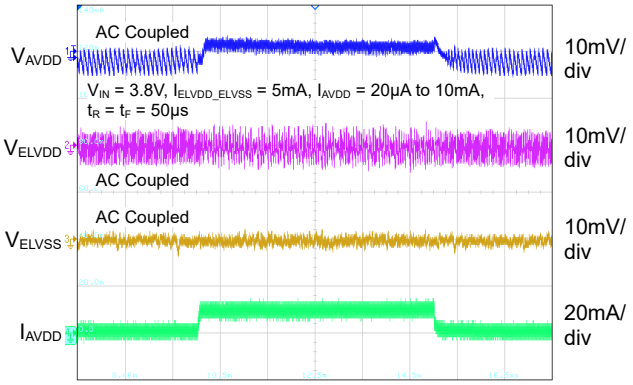
V_{IN} = 3.8V, AVDD_EN = high, SWIRE = high, MODE = high, VAI = VAO, V_{AVDD} = 3.3V, V_{ELVDD} = 3.3V, V_{ELVSS} = -3.3V, unless otherwise noted.

ELVDD and ELVSS Load Transient



Time (2ms/div)

AVDD Load Transient



Time (1ms/div)

FUNCTIONAL BLOCK DIAGRAM

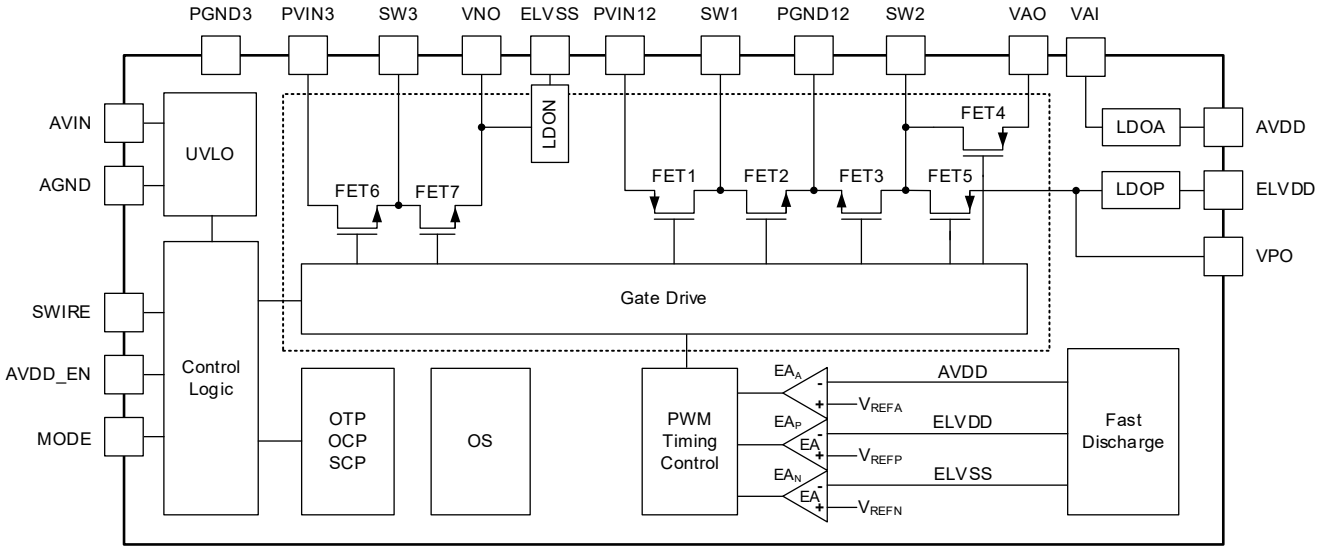


Figure 5. Functional Block Diagram

DETAILED DESCRIPTION

The device is dedicated approaches for providing triple outputs for AMOLED display panels.

Positive Buck-Boost Converter

The positive Buck-Boost Converter with SIDO topology operates with fixed 1MHz (TYP) frequency for AVDD and ELVDD.

A unique control scheme is developed for the SIDO to mitigate the loading cross-interference between the two rails, which is a common issue encountered when a single inductor is used to generate two positive outputs, AVDD and ELVDD.

The circuit maintains regulation on positive output rails without compromising performance in either Boost-inverter operation with any loading condition or Buck-inverter operation with almost any loading condition.

Inverting Buck-Boost Converter

The inverting Buck-Boost Converter operates with a peak-current-mode topology and fixed 1MHz (TYP) frequency for ELVSS.

Under-Voltage Lockout (UVLO)

The built-in under-voltage lockout function (UVLO) monitors the input voltage and disables the device when the input voltage is too low to operate.

Over-Temperature Protection (OTP)

The SGM38049 includes an OTP feature to prevent excessive power dissipation from overheating these devices. When junction temperature exceeds +145℃, the device stops switching and all the outputs are latched off.

Overload and Short-Circuit Protection (SCP)

The SGM38049 has an advanced short-circuit protection mechanism which prevents damage to these devices from unexpected applications. This device simultaneously monitors the inductor current and the LDO output current. If the load current exceeds the current limit of the LDO itself, or if the inductor current of the DC/DC exceeds its current limiting, the output load capacity will be restricted. If V_{ELVDD} falls below 85% (TYP) of the programmed output voltage longer than 1.2ms (TYP), the device stops switching and all the outputs are latched off. If V_{ELVSS} falls below 80% (TYP) of the programmed output voltage longer than 1.2ms (TYP), the device stops switching and all the outputs are latched off. If V_{AVDD} falls below 85% (TYP) of the programmed output voltage longer than 3ms (TYP), the device stops switching and all the outputs are latched off.

DETAILED DESCRIPTION (continued)

Soft-Start, Start-Up and Discharge

Pulling AVDD_EN high enables the AVDD.

Toggling SWIRE high starts the positive Buck-Boost converter and linear regulator ELVDD starts.

1.8ms (TYP) after Toggling SWIRE high, the negative Buck-Boost converter ELVSS starts.

All outputs starts with soft-start function to limit the inrush current. Figure 2 to Figure 4 show the start-up sequence of SGM38049.

The output discharge function can be controlled by the fast discharge control pulses. Please refer to the SWIRE Programming Tables. The fast discharge function for all outputs is enabled by default.

Device Reset

In order to reset the whole device, V_{IN} has to cycle below UVLO, or toggling SWIRE with SOFT RESET pulse (pulse 126), or Toggling both SWIRE and AVDD_EN low for t_{OFF}.

- A power cycle resets all settings to default values, and all latch off states lift.

- Toggling SWIRE with SOFT RESET pulse resets all the settings to default values.

- Toggling both SWIRE and AVDD_EN low for t_{OFF} reset all the settings to default values, and all latch off states lift.

AVDD Mode Select

VAI = VAO

If the MODE pin is pulled up to high level voltage, the VAI pin must be connected to VAO pin for the AVDD LDO power supply.

Toggling AVDD_EN high starts SIDO converter for VAO，and then the AVDD will be started with the programmed voltage.

VAI = External Power Supply

If the MODE pin is pulled down to low level voltage, the VAI pin must be connected to external power supply. An input capacitor should be placed close to the VAI pin. And the external power supply voltage must be at least 100mV higher than the AVDD voltage.

Toggling AVDD_EN high only starts the LDO for AVDD and the VAO output is absent.

VAI = VPO

If the MODE pin is floating, the VAI pin must be connected to VPO pin.

Toggling AVDD_EN high starts SIDO converter for VPO，and then the AVDD will be started with the programmed voltage.

The state detection of the MODE pin occurs only when AVDD_EN is pulled high, and remains latched after detection. It can only be reset when either power cycle or AVDD_EN power-down.

Digital Interface (SWIRE and AVDD_EN)

The positive output voltages V_{AVDD}, V_{ELVDD} and the negative output voltage V_{ELVSS} are allowed programming through the SWIRE digital interface in discrete steps.

Figure 2 to Figure 4 show examples for SGM38049 programming V_{ELVSS} to -2.4V. The SWIRE pin can be used as a standard enable pin if programming is not required.

The device starts with its default values if enabled. The SWIRE interface counts the rising edges and sets the new values as shown in Table 2 and Table 3. The settings are stored in a volatile memory.

Pulse 127 of SWIRE is a special pulse. The DDIC can send out all pulses in the programming tables directly if it can support 8 bit pulses (0 to 255). While if the DDIC can only support 7 bit pulses (0 to 127), and target pulse that bigger than 127 is used, the DDIC can send out the special pulse first to make the SWIRE interface to wait for next pulse (the difference number between the target pulse and the special pulse), then the target pulse is active. Sending the special pulse twice successively can clean itself. Example for 7-bit DDIC:

130 pulse of SWIRE: 127 + 3

160 pulse of SWIRE: 127 + 33

127 + 127 = Do Nothing.

The AVDD output with default voltage when pulling AVDD_EN high. However, the output voltage can be programmed by SWIRE before or after pulling AVDD_EN high. Pulling SWIRE Low would not affect the programmed AVDD output voltage (see Figure 2 to Figure 4) until pulling AVDD_EN low.

DETAILED DESCRIPTION (continued)

Table 2. SWIRE Programming 1

Pulse	Function Description
0 (no pulse programming)	Default settings
1 – 25	ELVDD output voltage setting (2.6V to 5V), as explained in Table 3
26 – 115	ELVSS output voltage setting (-0.3V to -9.2V), as explained in Table 3
116 – 125	AVDD output voltage setting (2.7V to 3.6V), as explained Table 3
126	Soft-reset, clear all settings and back to default state.
127	Pulse Accumulation Function: the actual effective configuration is pulse 127 plus the next pulse count.
128	All channel fast discharge is turned on.(default)
129	All channel fast discharge is turned off.
130	ELVSS Inverting Buck-Boost Converter with 2.2μH inductor (default)
131	ELVSS Inverting Buck-Boost Converter with 4.7μH inductor
132	Switching Frequency is changed to 1MHz. (default)
133	Switching Frequency is changed to 750kHz.
134	Switching Frequency is changed to 500kHz.
135	ELVSS PWM operation spread spectrum off（default）
136	ELVSS PWM operation spread spectrum on, spread spectrum range: 5%, spread spectrum frequency = 50Hz
137	ELVSS PWM operation spread spectrum on, spread spectrum range: 5%, spread spectrum frequency = 100Hz
138	ELVSS PWM operation spread spectrum on, spread spectrum range: 10%, spread spectrum frequency = 50Hz
139	ELVSS PWM operation spread spectrum on, spread spectrum range: 10%, spread spectrum frequency = 100Hz
140	Switching T_R/T_F rate setting: fast 4V/ns (default)
141	Reserved
142	Switching T_R/T_F rate setting: slow 1V/ns
143	EVLDD and ELVSS LDOs dropout voltage auto (default)
144	EVLDD and ELVSS LDOs dropout voltage 100mV
145	EVLDD and ELVSS LDOs dropout voltage 125mV
146	EVLDD and ELVSS LDOs dropout voltage 150mV
147	EVLDD and ELVSS LDOs dropout voltage 175mV
148	EVLDD and ELVSS LDOs dropout voltage 200mV
149	ELVSS Transient in fast mode (50μs/100mV)
150	ELVSS Transient in normal mode (default, 100μs/100mV)
151	ELVSS Transient in slow mode (200μs/100mV)
152	SCP & OTP ON (default)
153	SCP & OTP OFF

DETAILED DESCRIPTION (continued)

Table 3. SWIRE Programming 2

Pulse	V_{ELVDD} (V)	Pulse	V_{ELVSS} (V)	Pulse	V_{ELVSS} (V)	Pulse	V_{ELVSS} (V)	Pulse	V_{AVDD} (V)
0/no pulse	3.3	0/no pulse	-3.3	56	-3.3	87	-6.4	0/no pulse	3.3
1	2.6	26	-0.3	57	-3.4	88	-6.5	116	2.7
2	2.7	27	-0.4	58	-3.5	89	-6.6	117	2.8
3	2.8	28	-0.5	59	-3.6	90	-6.7	118	2.9
4	2.9	29	-0.6	60	-3.7	91	-6.8	119	3.0
5	3.0	30	-0.7	61	-3.8	92	-6.9	120	3.1
6	3.1	31	-0.8	62	-3.9	93	-7.0	121	3.2
7	3.2	32	-0.9	63	-4.0	94	-7.1	122	3.3
8	3.3	33	-1.0	64	-4.1	95	-7.2	123	3.4
9	3.4	34	-1.1	65	-4.2	96	-7.3	124	3.5
10	3.5	35	-1.2	66	-4.3	97	-7.4	125	3.6
11	3.6	36	-1.3	67	-4.4	98	-7.5		
12	3.7	37	-1.4	68	-4.5	99	-7.6		
13	3.8	38	-1.5	69	-4.6	100	-7.7		
14	3.9	39	-1.6	70	-4.7	101	-7.8		
15	4.0	40	-1.7	71	-4.8	102	-7.9		
16	4.1	41	-1.8	72	-4.9	103	-8.0		
17	4.2	42	-1.9	73	-5.0	104	-8.1		
18	4.3	43	-2.0	74	-5.1	105	-8.2		
19	4.4	44	-2.1	75	-5.2	106	-8.3		
20	4.5	45	-2.2	76	-5.3	107	-8.4		
21	4.6	46	-2.3	77	-5.4	108	-8.5		
22	4.7	47	-2.4	78	-5.5	109	-8.6		
23	4.8	48	-2.5	79	-5.6	110	-8.7		
24	4.9	49	-2.6	80	-5.7	111	-8.8		
25	5.0	50	-2.7	81	-5.8	112	-8.9		
		51	-2.8	82	-5.9	113	-9.0		
		52	-2.9	83	-6.0	114	-9.1		
		53	-3.0	84	-6.1	115	-9.2		
		54	-3.1	85	-6.2				
		55	-3.2	86	-6.3				

DETAILED DESCRIPTION (continued)

PCB Layout Guidelines

PCB layout is an important task in the power supply design. Good PCB layout minimizes EMI and allows very good output voltage regulation. For SGM38049, the following PCB layout guidelines are recommended.

• Keep the power ground plane on the top layer (all capacitor grounds and PGND pins must be connected together with one uninterrupted ground plane).

• AGND and PGND must be connected together on the same ground plane.

• Always avoid vias when possible. They have high inductance and resistance. If vias are necessary, always use more than one in parallel to decrease parasitics, especially for power lines.

• For high dv/dt signals (switch pin traces): keep copper to a minimum to prevent making unintentional parallel plate capacitors with other traces or to a ground plane. Best to route signal and return on same layer.

• For high di/dt signals: keep traces short, wide and closely spaced. This will reduce stray inductance and decrease the current loop area to help prevent EMI.

• Keep input capacitors close to the IC with low inductance traces.

• Keep output capacitors close to the IC with low inductance traces.

• Keep trace from switching node pin to inductor short if possible: it reduces EMI emissions and noise that may couple into other portions of the converter.

• Isolate analog signal paths from power paths.

REVISION HISTORY

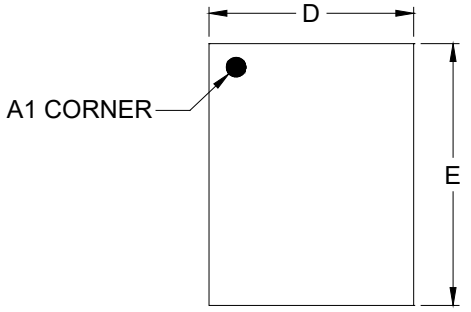
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JULY 2026 – REV.A to REV.A.1	Page
Changed Electrical Characteristics and Timing Requirements sections	6

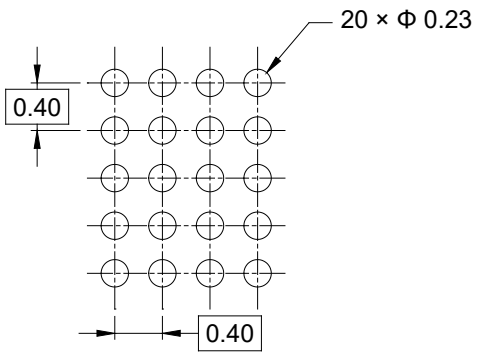
Changes from Original to REV.A (JUNE 2026)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

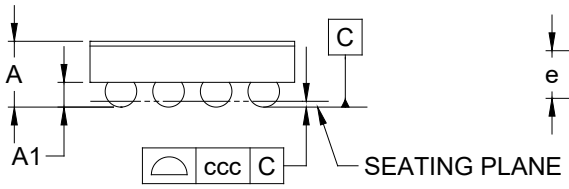
WLCSP-1.72×2.2-20B



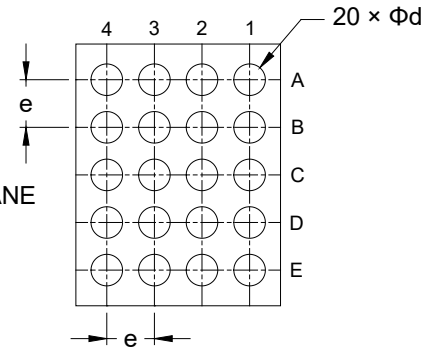
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



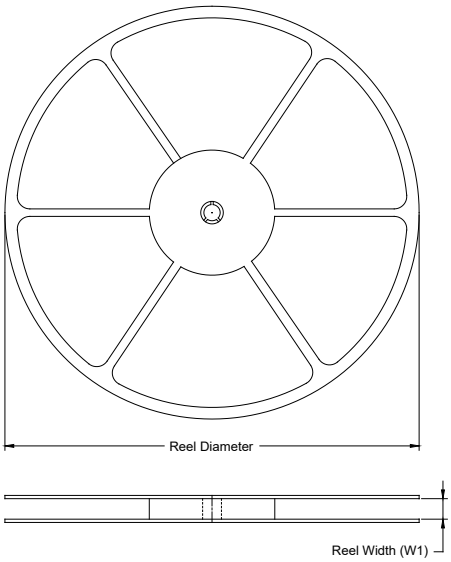
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.588
A1	0.188	-	0.228
D	1.690	-	1.750
E	2.170	-	2.230
d	0.235	-	0.295
e	0.400 BSC		
ccc	0.050		

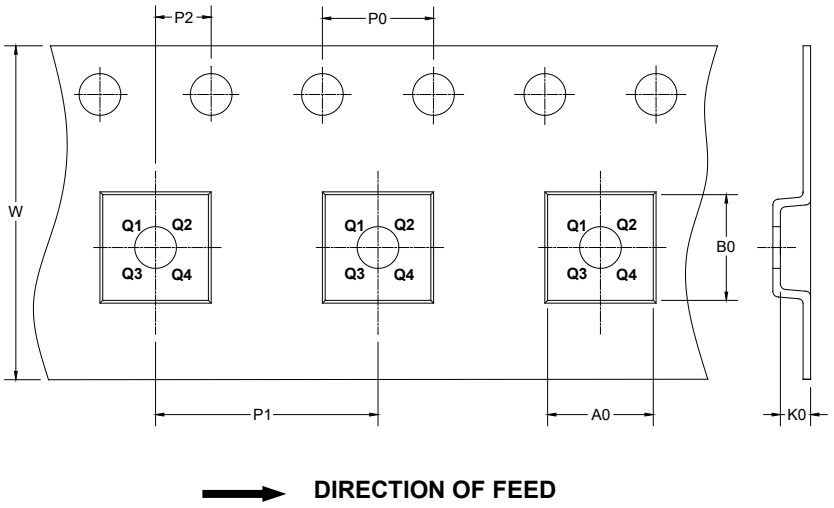
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



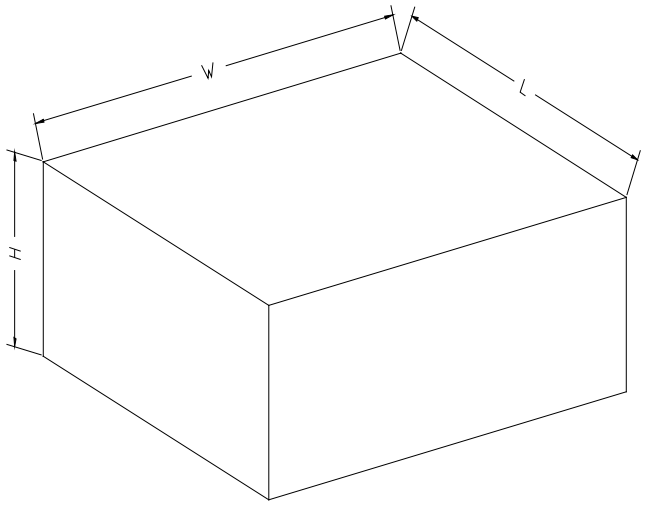
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.72×2.2-20B	7"	9.5	1.86	2.36	0.72	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002