SGM37601
40V High Efficiency Boost Converter with I²C Controlled 6-CH LED Driver

GENERAL DESCRIPTION

The SGM37601 is a high-efficiency LED driver designed specifically to provide backlight power for LED arrays in display applications. The SGM37601 supports up to 12 LEDs in series per string. It adopts peak current mode control, and the minimum LED string cathode voltage is regulated to an adequate operating headroom voltage, which produces sufficient voltage margin to guarantee the accuracy of the current.

The SGM37601 equips six internal current sinks for up to ±1.2% current matching, ensuring superior brightness uniformity across LED strings.

The LED current, switching frequency and dimming mode can be set via I²C interface. An internal 40V power switch with 155mΩ R_{DSON}, combined with peak-current-mode control, provides high efficiency performance and cycle-by-cycle over-current protection. The switching frequency can be programmed between 100kHz and 1.6MHz. The SGM37601 can achieve high efficiency and allows small component size.

The SGM37601 is available in Green TQFN-3.5×3.5-20L and TQFN-3×3-24L packages.

APPLICATIONS

LED Backlight for Tablet and Notebook

FEATURES

- **Wide Input Voltage: 2.8V to 24V**
- **High Output Voltage: up to 40V**
- **Programmable LED Current: 6mA to 25mA per Channel**
- **LED Current Accuracy ±2%, Matching ±1.2%**
- **Dimming Controls**
  - **Direct PWM up to 25kHz with Minimum 1% Duty**
  - **PWM to Analog:**
    Up to 2kHz @ 12-Bit Resolution
    Up to 4kHz @ 11-Bit Resolution
    Up to 8kHz @ 10-Bit Resolution
  - **PWM to Mixed:**
    Up to 2kHz @ 12-Bit Resolution
    Up to 4kHz @ 11-Bit Resolution
  - **PWM to Mixed-26kHz:**
    Up to 2kHz @ 12-Bit Resolution
    Up to 4kHz @ 11-Bit Resolution
    Up to 8kHz @ 10-Bit Resolution
- **Programmable LED Current, Switching Frequency, and Dimming Mode via I²C Interface**
- **Switching Frequency: 100kHz to 1.6MHz**
- **Advanced Switching Slew Rate Control**
- **Flexible Boost Converter Compensation (Internal/External)**
- **Programmable PFM Mode with User-Defined Frequency Scaling**
- **Programmable Fade-In/Fade-Out Timing**
- **Embedded Memory with MTP**
- **Protections:**
  - **LED String Open, LED OVP and Short Protection**
  - **Cycle-by-Cycle Over-Current Protection**
  - **Programmable Output Over-Voltage Protection (Default 36V)**
  - **Programmable Over-Temperature Protection**
- **Available in Green TQFN-3.5×3.5-20L and TQFN-3×3-24L Packages**

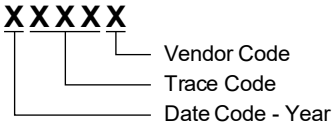
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM37601	TQFN-3.5×3.5-20L	-40℃ to +85℃	SGM37601YTRL20G/TR	SGM1RG YTRL20 XXXXX	Tape and Reel, 4000
	TQFN-3×3-24L	-40℃ to +85℃	SGM37601YTWY24G/TR	37601 YTWY24 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

TQFN-3.5×3.5-20L/TQFN-3×3-24L



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage ..... -0.3V to 26.5V
VIN, EN, PWM to AGND ..... -0.3V to 26.5V
SW, VOUT, LED1, LED2, LED3, LED4, LED5, LED6 to AGND ..... -0.3V to 42V
SDA, SCL, VDC, A0, COMP to AGND ..... -0.3V to 6V
Package Thermal Resistance
TQFN-3.5×3.5-20L, θ_{JA} ..... 33.4℃/W
TQFN-3.5×3.5-20L, θ_{JB} ..... 12.3℃/W
TQFN-3.5×3.5-20L, $\theta_{JC\ (TOP)}$ ..... 29.4℃/W
TQFN-3.5×3.5-20L, $\theta_{JC\ (BOT)}$ ..... 1.9℃/W
TQFN-3×3-24L, θ_{JA} ..... 34.7℃/W
TQFN-3×3-24L, θ_{JB} ..... 11.3℃/W
TQFN-3×3-24L, $\theta_{JC\ (TOP)}$ ..... 34.4℃/W
TQFN-3×3-24L, $\theta_{JC\ (BOT)}$ ..... 1.9℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Input Voltage ..... 2.8V to 24V
Operating Ambient Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

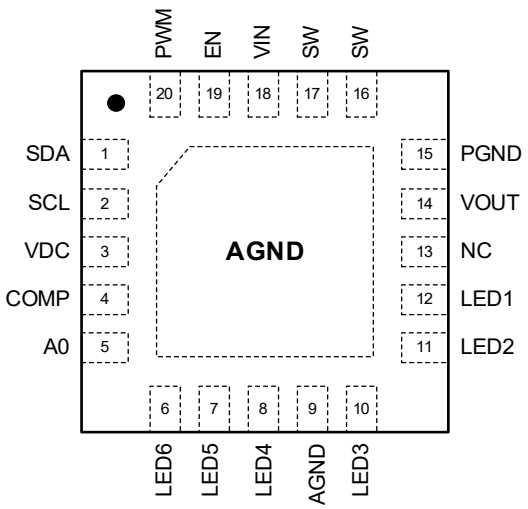
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

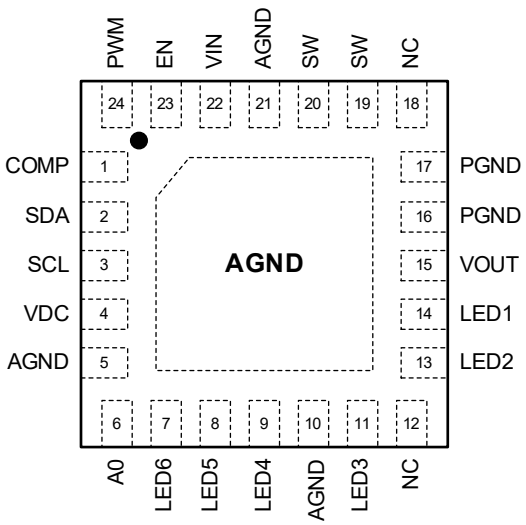
PIN CONFIGURATIONS

(TOP VIEW)



TQFN-3.5×3.5-20L

(TOP VIEW)



TQFN-3×3-24L

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
TQFN-3.5×3.5-20L	TQFN-3×3-24L			
1	2	SDA	I/O	I²C Interface Data Line.
2	3	SCL	I	I²C Interface Clock Line.
3	4	VDC	P	Internal Regulator Output Pin. A 1μF or larger ceramic capacitor should be used from VDC pin to AGND.
4	1	COMP	O	Boost Converter External Compensation Pin.
5	6	A0	I	7-Bit Device Address Selection Pin. This pin is used to assign the I²C address of the device. Pull A0 low to select address 0x36, and pull it high to select address 0x37.
6	7	LED6	P	LED6 Current Sink Pin.
7	8	LED5	P	LED5 Current Sink Pin.
8	9	LED4	P	LED4 Current Sink Pin.
9	5, 10, 21	AGND	G	Analog Ground Pin.
10	11	LED3	P	LED3 Current Sink Pin.
11	13	LED2	P	LED2 Current Sink Pin.
12	14	LED1	P	LED1 Current Sink Pin.
13	12, 18	NC	-	No Connection.
14	15	VOUT	P	Boost Converter Output Pin.
15	16, 17	PGND	G	Power Ground.
16, 17	19, 20	SW	P	Boost Converter Switching Pin.
18	22	VIN	P	Device Supply Input Pin.
19	23	EN	I	Active-High Enable Input Pin.
20	24	PWM	I	PWM Dimming Signal Input Pin.
Exposed Pad		AGND	G	Exposed Pad. To enhance heat dissipation, the exposed pad must be soldered to a large area on the PCB and connected to AGND.

NOTE: I = input, I/O = input or output, P = power, G = ground.

TYPICAL APPLICATION

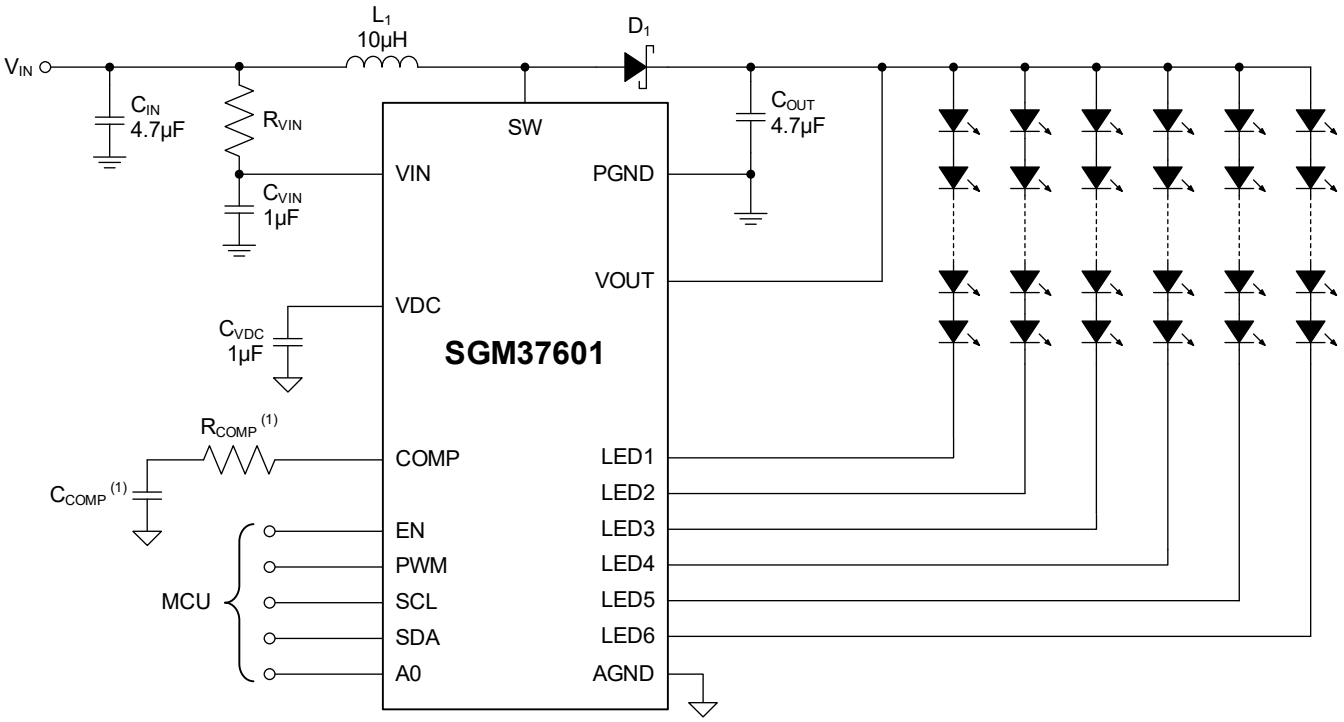


Figure 1. Typical Application Circuit

NOTE:

1. It is recommended to use differential RC values for low V_{IN} application. For 6P11S typical application, Boost switching frequency = 1.225MHz, I_{LED} = 25mA/channel, C_{OUT} = 4.7μF, L_1 = 10μH, while the recommended value for RC compensation network is shown below:

Case	V_{IN} Range (V)	R_{COMP} (kΩ)	C_{COMP} (nF)
Case 1: PWM Mode	7 to 21	20	1
Case 2: DC Mode	5 to 21	5.1	22

ELECTRICAL CHARACTERISTICS

(V_{IN} = 4.2V, T_J = +25℃, C_{VIN} = 1μF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Power Supply						
Input Supply Voltage	V_{IN}		2.8	4.2	24	V
Quiescent Current	I_Q	EN = high, f_{SW} = 300kHz, PWM = 50%		3.2		mA
		EN = high, SW no switching, PWM = 0%		1.7		mA
Shutdown Current	I_{SHDN}	V_{IN} = 4.2V, EN = low		2.6	5	μA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising		2.7		V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}			210		mV
Interface Characteristic						
EN, PWM, SCL, SDA and A0 Input Voltage	V_{IH}	V_{IN} = 4.2V	1.2			V
	V_{IL}	V_{IN} = 4.2V			0.6	
Internal Pull Low Resistor for EN, PWM	R_{PULL_LOW}			1		MΩ
Internal Pull Low Current for SCL and SDA	I_{IH_2}			0.01	1	μA
Output Low Level for SDA	V_{OL_SDA}	External pull-up current = 3mA		0.3	0.5	V
Output Leakage Current for SDA	V_{LK_DIO}	SDA pin voltage = 3.3V			1	μA
Boost Converter						
Switching Frequency Accuracy	f_{SW_ACC}	Boost operates at PWM mode, f_{SW} = 300kHz	-9		9	%
Switching Frequency Setting Range	f_{SW}	Boost operates at PWM mode	0.1		1.6	MHz
Maximum Duty Cycle	D_{MAX}	f_{SW} = 300kHz	90	95		%
Boost Switch R_{DSON}	R_{DSON}	V_{IN} = 4.2V		155		mΩ
Switching Current Limitation	I_{OCP}	NMOS peak current limit	2	2.5	3	A
Boost Minimum ON Time	t_{MON}			118		ns
VOUT Over-Voltage Limit	V_{OVP}	Setting by OVP[4:0] bits with 1V/step, default 36V, rising threshold, C_{OUT} = 4.7μF		36		V
LED Current						
Leakage Current of LEDx	I_{LK_LEDx}	V_{LEDx} = 36V, I_{LEDx} = 0mA		7	9	μA
LED Headroom Voltage	V_{LED_HR}	I_{LEDx} = 20mA	0.35	0.5		V
Maximum LED Current Setting	I_{LED_MAX}	LED 100% setting	6		25	mA
Minimum LED Current Setting	I_{LED_MIN}	Setting by dimming	100			μA
LED Current Accuracy	I_{LED_ACC}	PWM duty = 100%, I_{LEDx} = 20mA, PWM = 1kHz	-2		2	%
		PWM duty = 15%, I_{LEDx} = 20mA, PWM = 1kHz	-2.5		2.5	%
		PWM duty = 5%, I_{LEDx} = 20mA, PWM = 1kHz	-5		5	%
		PWM duty = 1%, I_{LEDx} = 20mA, PWM = 1kHz	-15		15	%
LED Current Matching	I_{LED_MAT}	PWM duty = 100%, I_{LEDx} = 20mA, PWM = 1kHz	-1.2		1.2	%
		PWM duty = 15%, I_{LEDx} = 20mA, PWM = 1kHz	-1.5		1.5	%
		PWM duty = 5%, I_{LEDx} = 20mA, PWM = 1kHz	-3		3	%
		PWM duty = 1%, I_{LEDx} = 20mA, PWM = 1kHz	-7		7	%
DC Dimming Resolution	Sres_2k	PWM < 2kHz		4096		Steps
	Sres_4k	PWM = 2kHz to 4kHz		2048		Steps
	Sres_8k	PWM = 4kHz to 8kHz		1024		Steps
	Sres_25k	PWM = 8kHz to 25kHz		512		Steps
PWM Minimum On/Off Time	t_{PWM_MIN}			400		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 4.2V, T_J = +25℃, C_{VIN} = 1μF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Protection						
OTP Rising Threshold	T_{OTP}	Setting by OTP_OPTION[1:0] bits, default 140℃		140		℃
OTP Hysteresis	T_{OTP_HYS}			20		℃
LED Open Falling Threshold	V_{LED_OPEN}			0.13		V
LED Short Rising Threshold	V_{LED_SHORT}			5.5		V
MTP						
Data Write Time	t_{WR}	Timing of write one page into MTP (12 byte)		50		ms
I²C Interface Timing						
Maximum I²C Clock Frequency	f_{SCL_MAX}		1	400	1000	kHz
Hold Time for START and Repeated START Condition	t_{HD_STA}		0.6			μs
SCL Clock Low Time	t_{LOW}		1.3			μs
SCL Clock High Time	t_{HIGH}		600			ns
Setup Time for a Repeated START Condition	t_{SU_STA}		600			ns
SDA Data Hold Time	t_{HD_DAT}		50			ns
SDA Data Setup Time	t_{SU_DAT}		100			ns
Setup Time for STOP Condition	t_{SU_STO}		600			ns
I²C Bus Free Time between a STOP and a START	t_{BUF}		1.3			μs
Capacitive Load for I²C Bus	C_B				400	pF

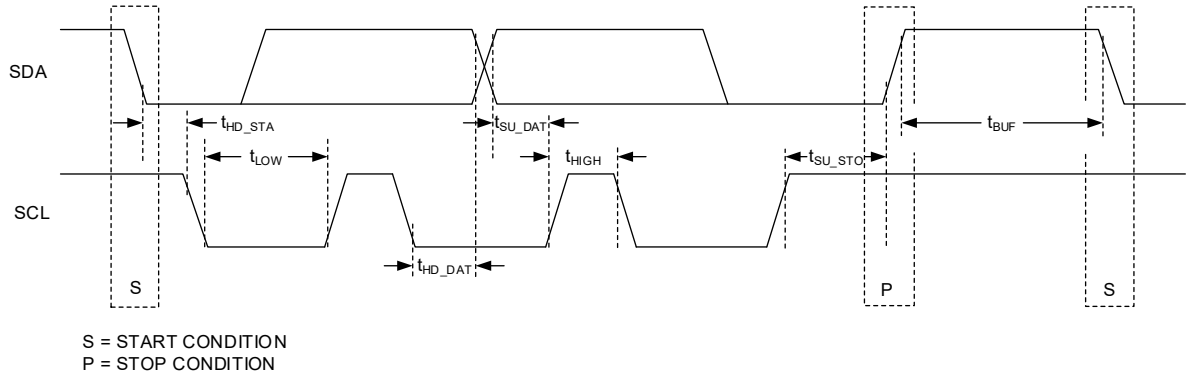
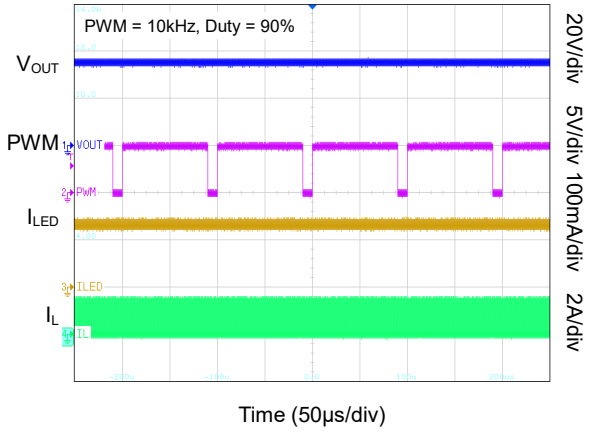


Figure 2. I²C Interface Timing Diagram

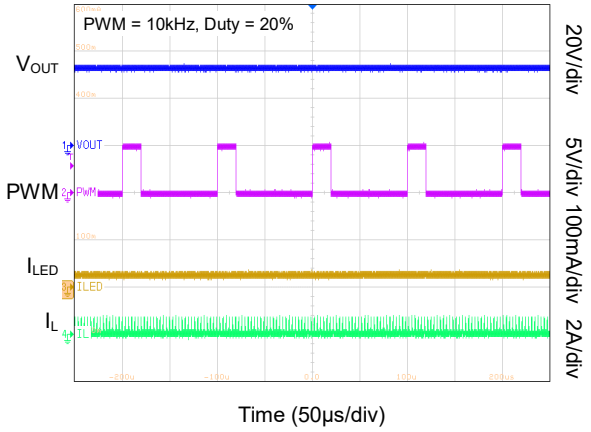
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, 12S6P LEDs, I_{LEDx} = 25mA/channel, I_{LED} = 6 × I_{LEDx}, L_1 = 10μH, C_{IN} = 4.7μF/50V, C_{OUT} = 4.7μF/50V, unless otherwise noted.

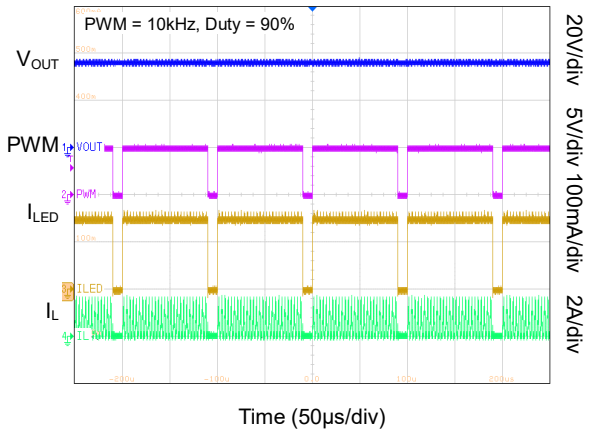
LED Dimming (DC Mode)



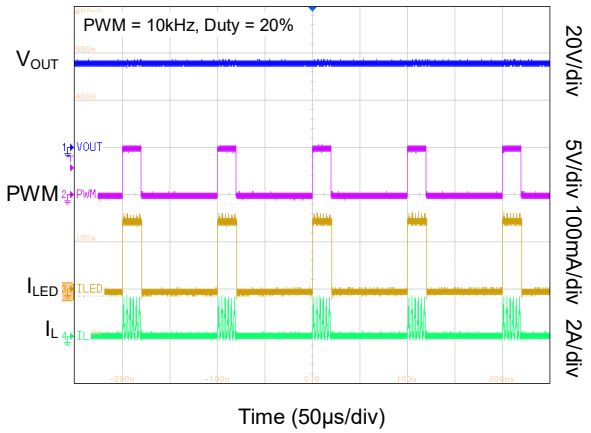
LED Dimming (DC Mode)



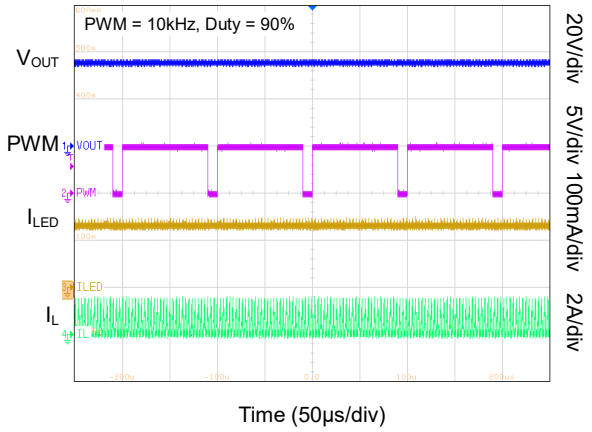
LED Dimming (PWM Mode)



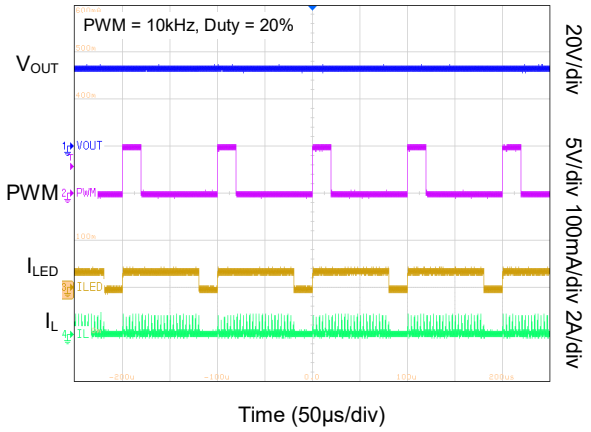
LED Dimming (PWM Mode)



LED Dimming (Mix Mode)



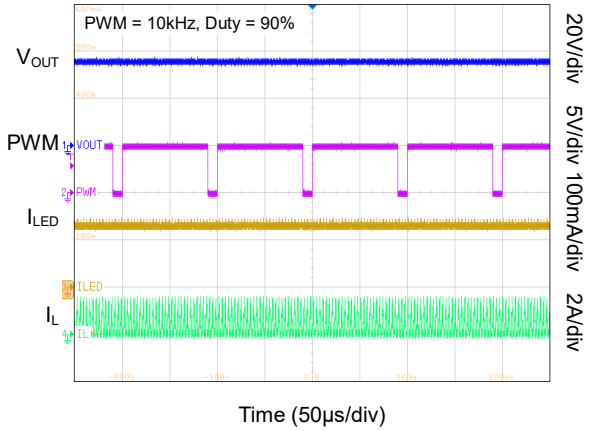
LED Dimming (Mix Mode)



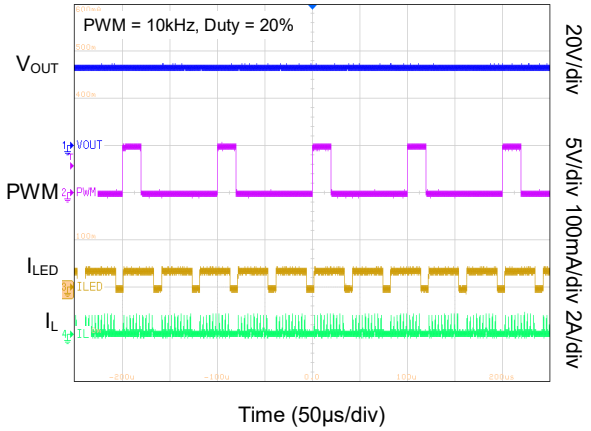
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, 12S6P LEDs, I_{LEDx} = 25mA/channel, I_{LED} = 6 × I_{LEDx}, L_1 = 10μH, C_{IN} = 4.7μF/50V, C_{OUT} = 4.7μF/50V, unless otherwise noted.

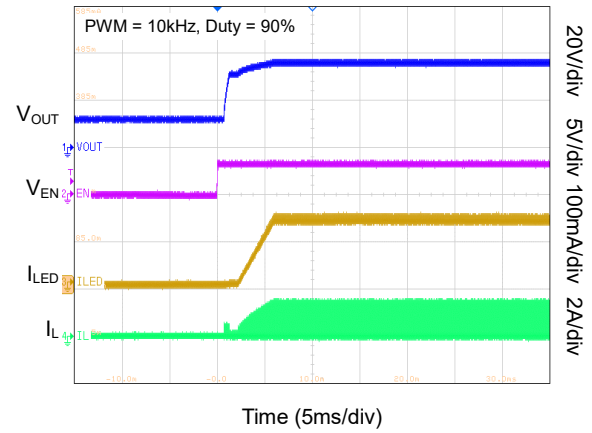
LED Dimming (Mix-26k Mode)



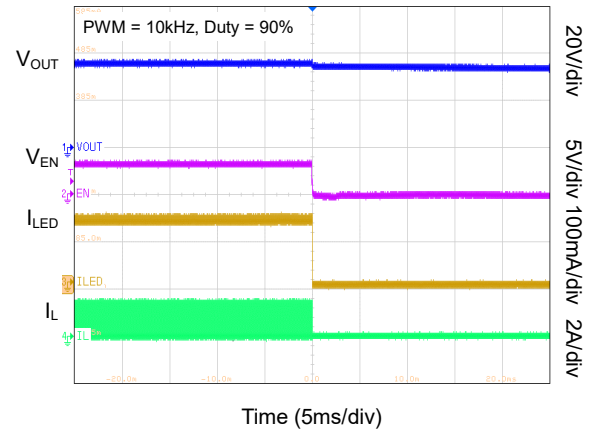
LED Dimming (Mix-26k Mode)



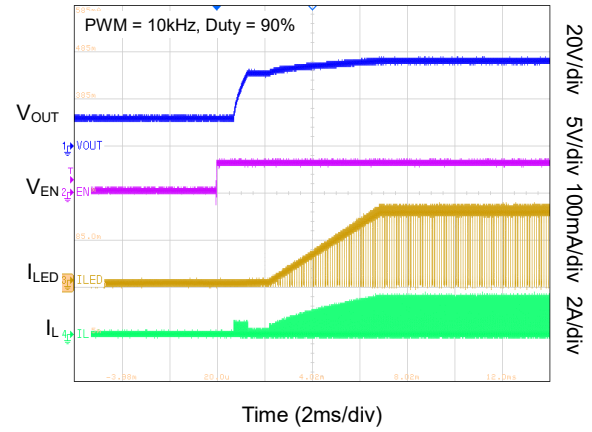
EN On (DC Mode)



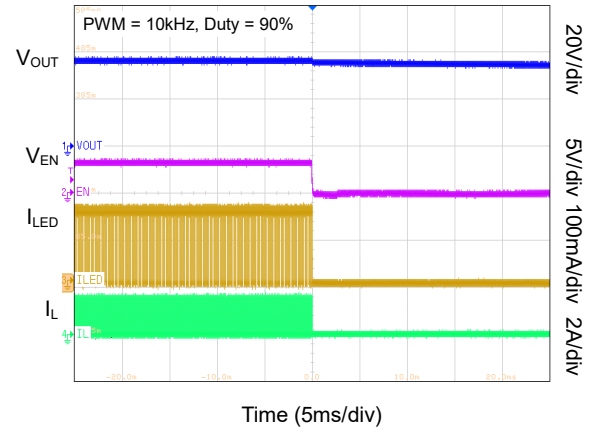
EN Off (DC Mode)



EN On (PWM Mode)



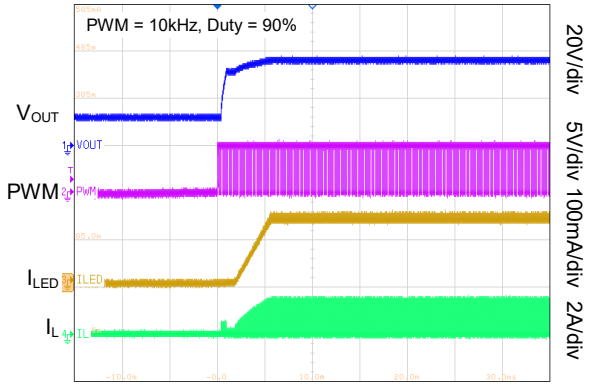
EN Off (PWM Mode)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

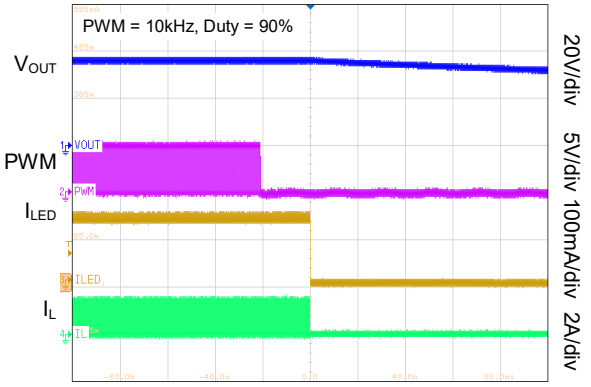
V_{IN} = 12V, 12S6P LEDs, I_{LEDx} = 25mA/channel, I_{LED} = 6 × I_{LEDx}, L_1 = 10μH, C_{IN} = 4.7μF/50V, C_{OUT} = 4.7μF/50V, unless otherwise noted.

PWM On (DC Mode)



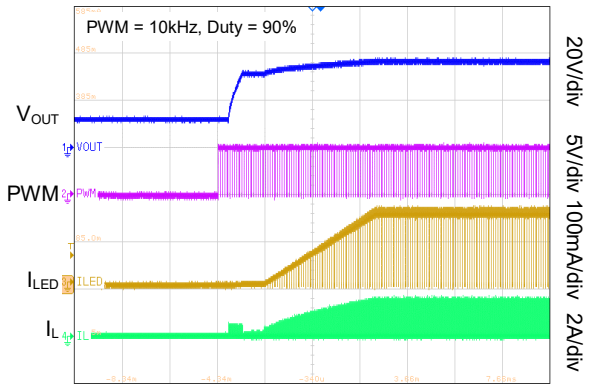
Time (5ms/div)

PWM Off (DC Mode)



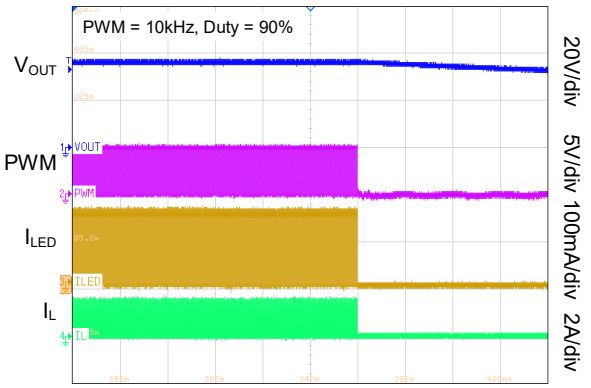
Time (20ms/div)

PWM On (PWM Mode)



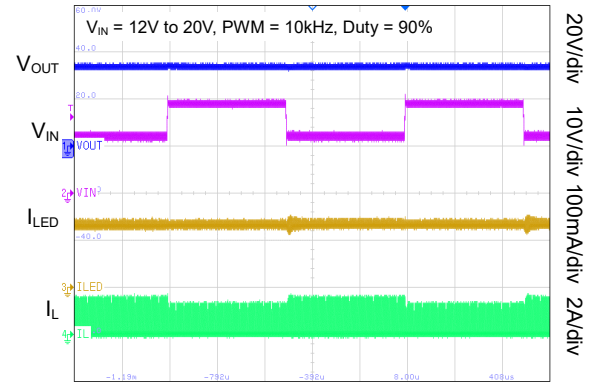
Time (2ms/div)

PWM Off (PWM Mode)



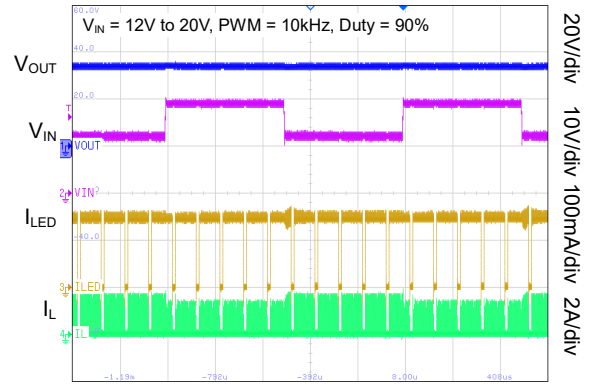
Time (20ms/div)

Line Transient Response (DC Mode)



Time (200μs/div)

Line Transient Response (PWM Mode)

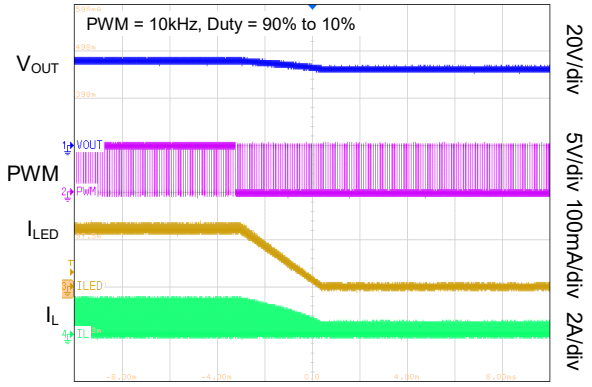


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

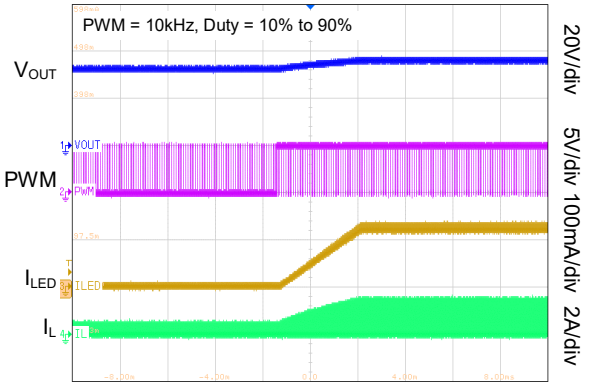
V_{IN} = 12V, 12S6P LEDs, I_{LEDx} = 25mA/channel, I_{LED} = 6 × I_{LEDx}, L_1 = 10μH, C_{IN} = 4.7μF/50V, C_{OUT} = 4.7μF/50V, unless otherwise noted.

Brightness Adjustment (DC Mode)



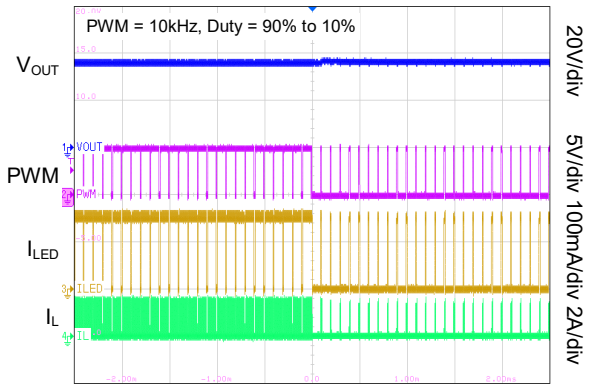
Time (2ms/div)

Brightness Adjustment (DC Mode)



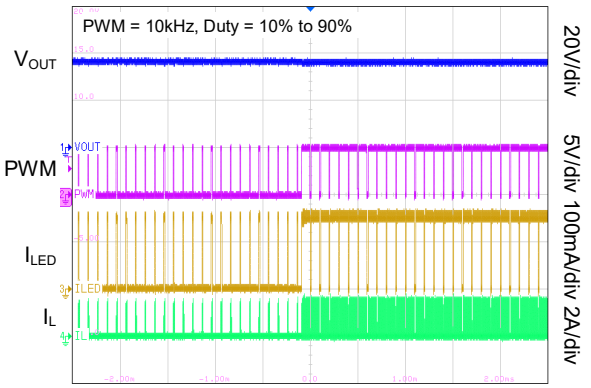
Time (2ms/div)

Brightness Adjustment (PWM Mode)



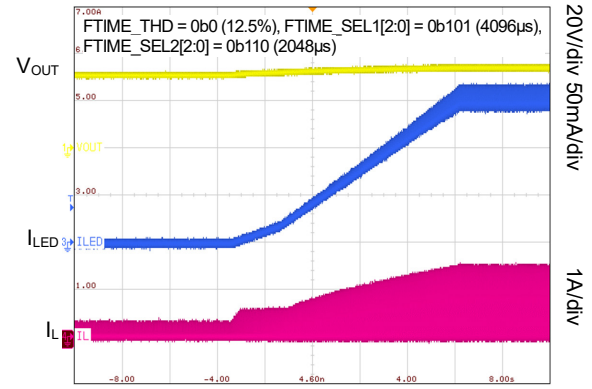
Time (500μs/div)

Brightness Adjustment (PWM Mode)



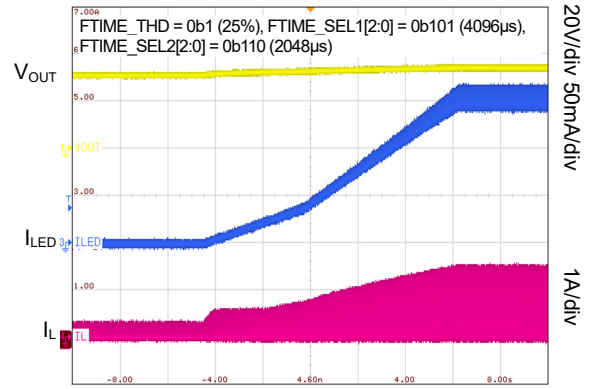
Time (500μs/div)

Fade-in Timing



Time (2s/div)

Fade-in Timing

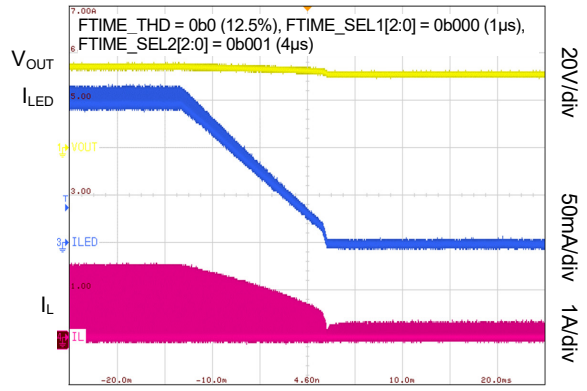


Time (2s/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

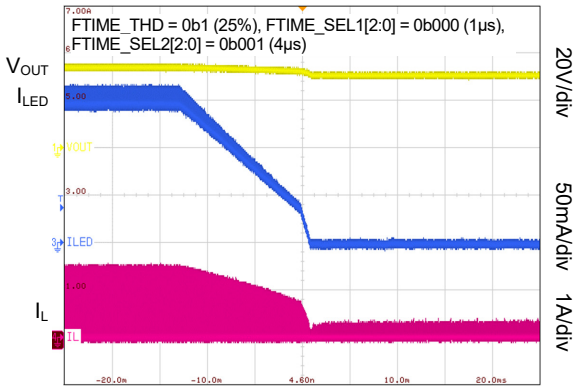
V_{IN} = 12V, 12S6P LEDs, I_{LEDx} = 25mA/channel, I_{LED} = 6 × I_{LEDx}, L_1 = 10μH, C_{IN} = 4.7μF/50V, C_{OUT} = 4.7μF/50V, unless otherwise noted.

Fade-out Timing



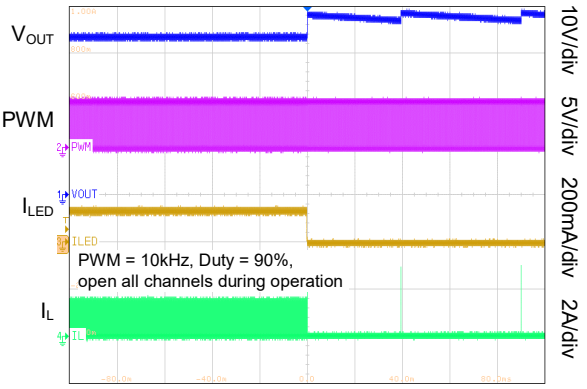
Time (5ms/div)

Fade-out Timing



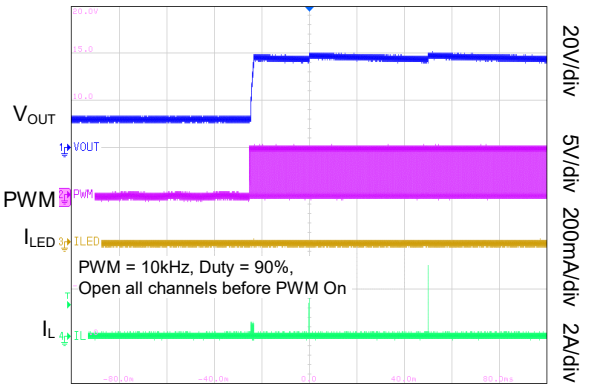
Time (5ms/div)

Output Open Protection (DC Mode)



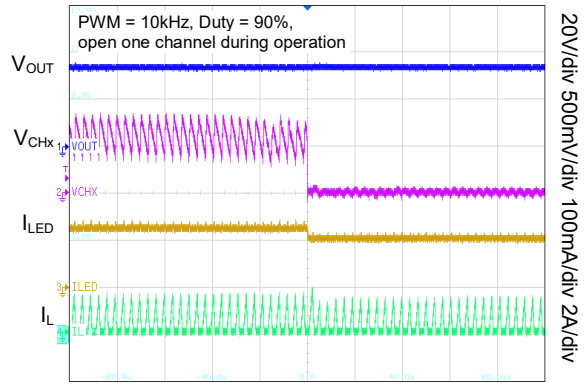
Time (20ms/div)

Output Open Protection (DC Mode)



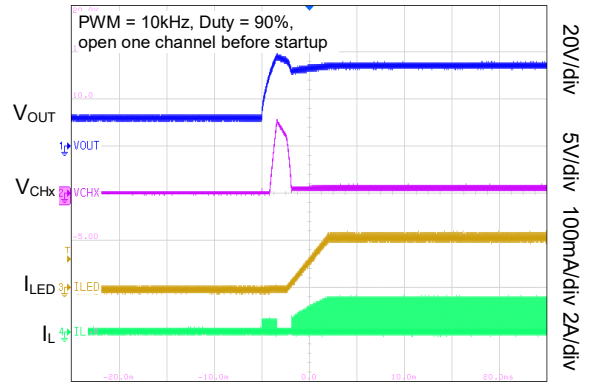
Time (20ms/div)

LED Open Protection (DC Mode)



Time (20μs/div)

LED Open Protection (DC Mode)

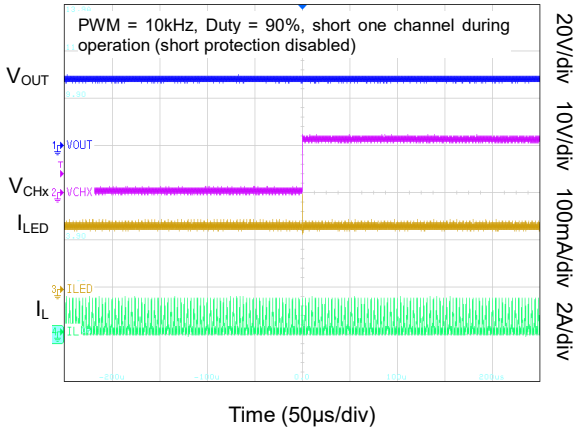


Time (5ms/div)

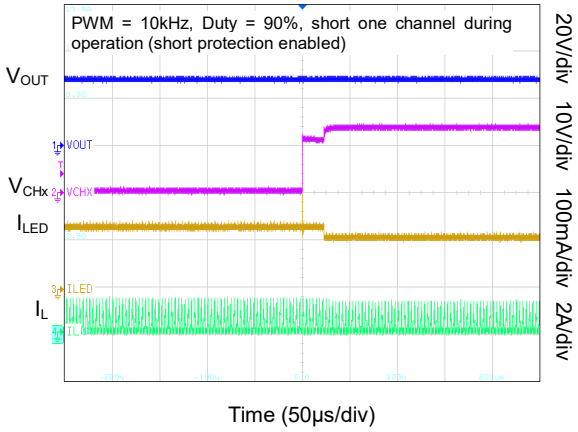
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, 12S6P LEDs, I_{LEDx} = 25mA/channel, I_{LED} = 6 × I_{LEDx}, L_1 = 10μH, C_{IN} = 4.7μF/50V, C_{OUT} = 4.7μF/50V, unless otherwise noted.

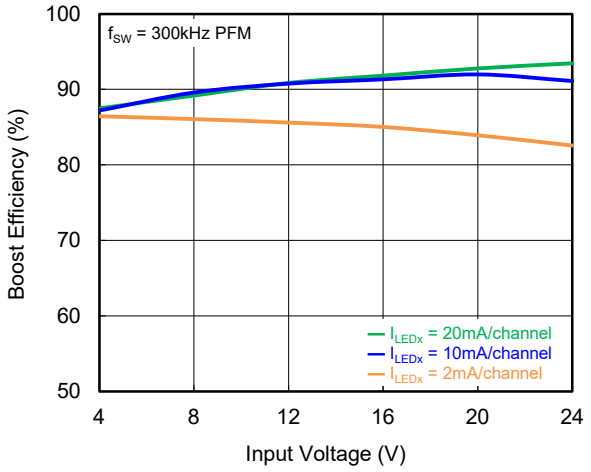
LED Short Protection (DC Mode)



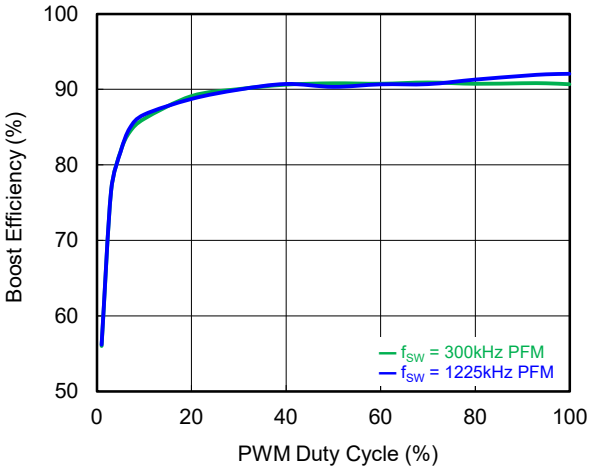
LED Short Protection (DC Mode)



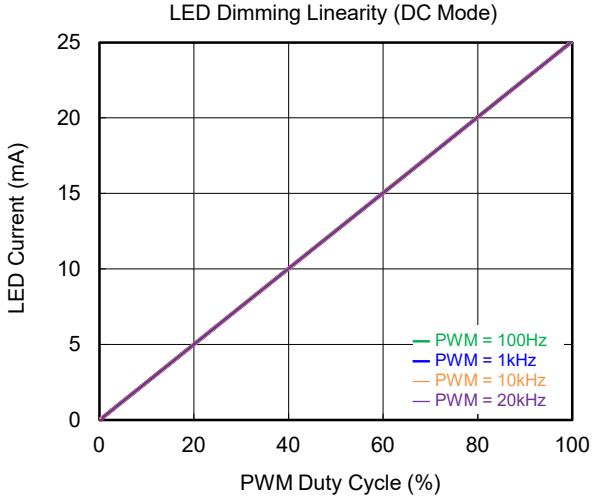
Boost Efficiency vs. Input Voltage



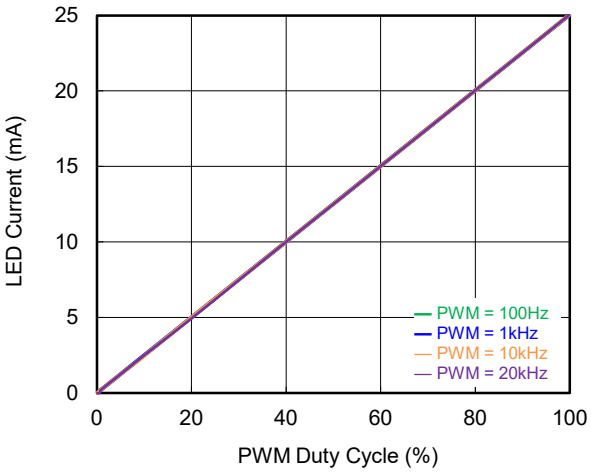
Boost Efficiency vs. PWM Duty Cycle (DC Mode)



LED Dimming Linearity (DC Mode)



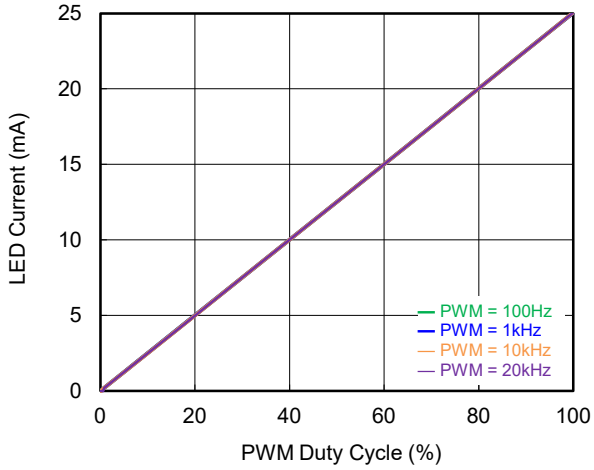
LED Dimming Linearity (PWM Mode)



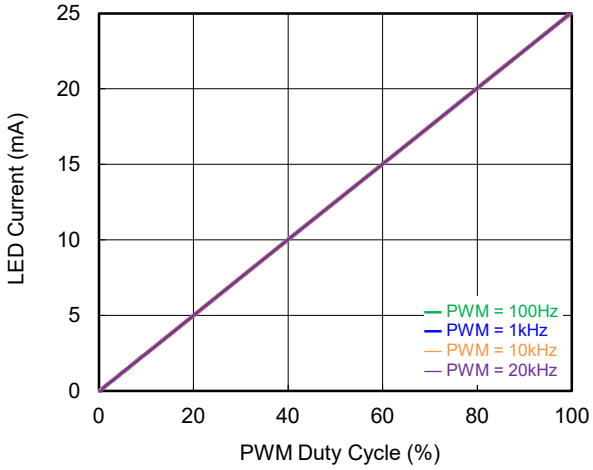
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, 12S6P LEDs, I_{LEDx} = 25mA/channel, I_{LED} = 6 × I_{LEDx}, L_1 = 10μH, C_{IN} = 4.7μF/50V, C_{OUT} = 4.7μF/50V, unless otherwise noted.

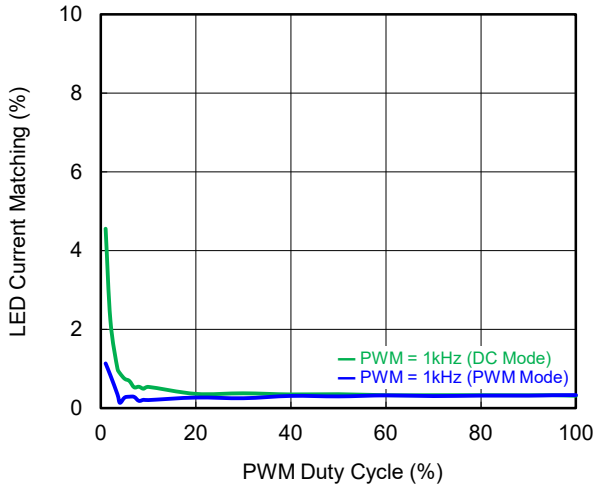
LED Dimming Linearity (Mix Mode)



LED Dimming Linearity (Mix-26k Mode)



LED Current Matching vs. PWM Duty Cycle



FUNCTIONAL BLOCK DIAGRAM

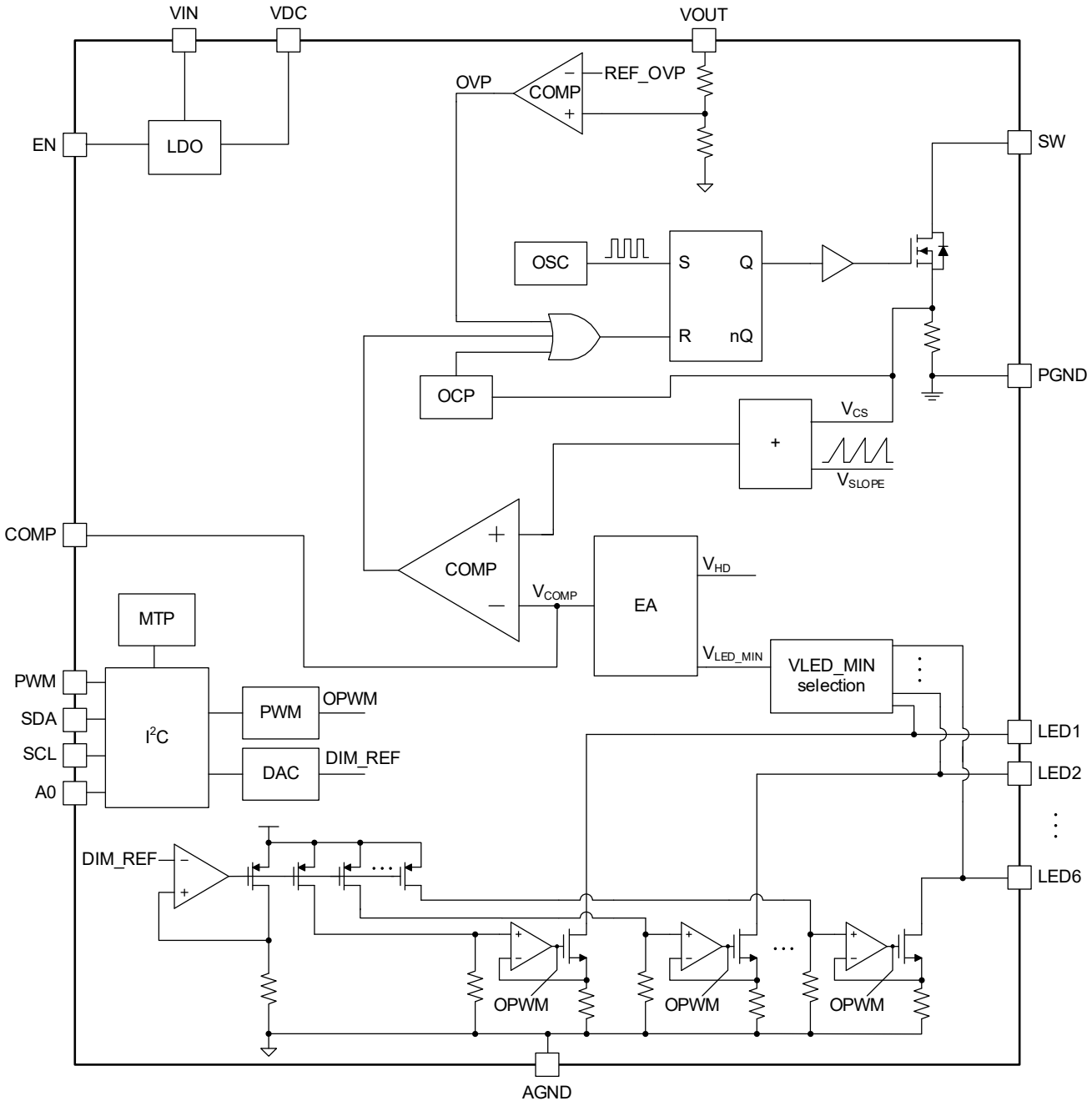


Figure 3. Functional Block Diagram

TIMING DIAGRAM

I²C Interface

SGM37601 I²C slave address = 7'b0110110 (A0 = low) and 7'b0110111 (A0 = high). I²C interface supports fast mode (bit rate up to 400kb/s). The write or read bit stream is shown in Figure 4 to Figure 11.

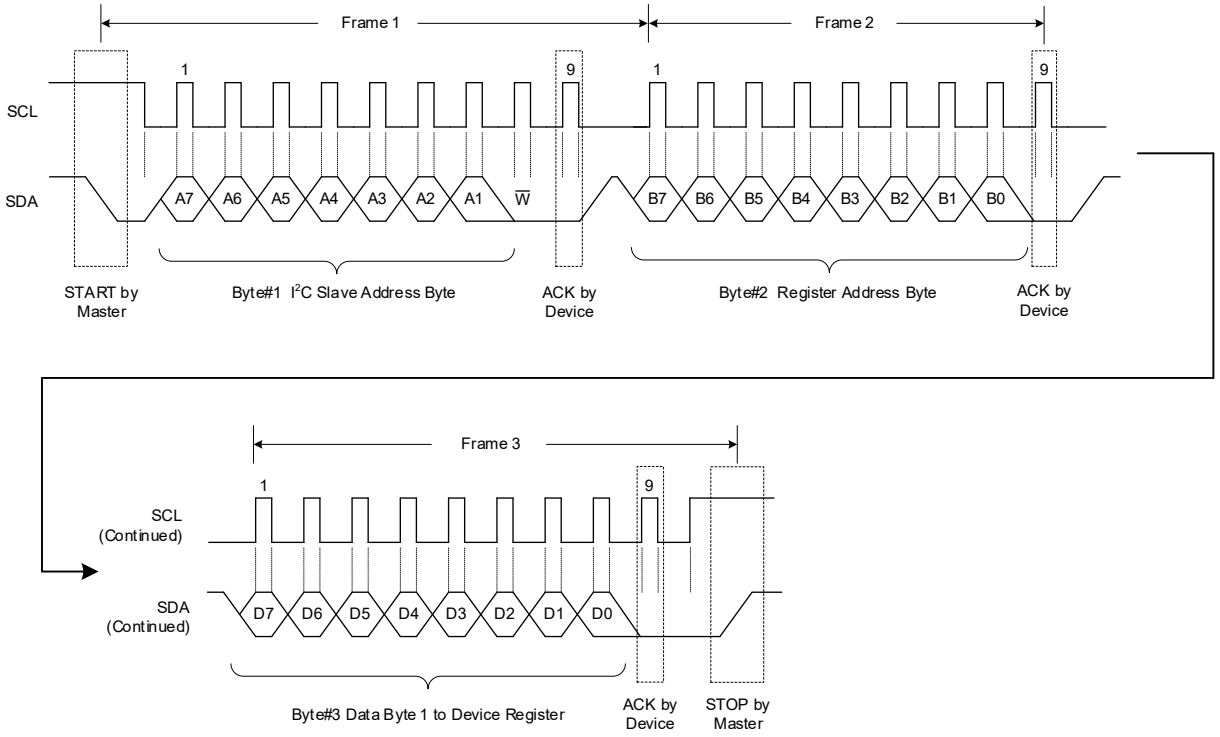


Figure 4. A Single Write Transaction (To SGM37601)

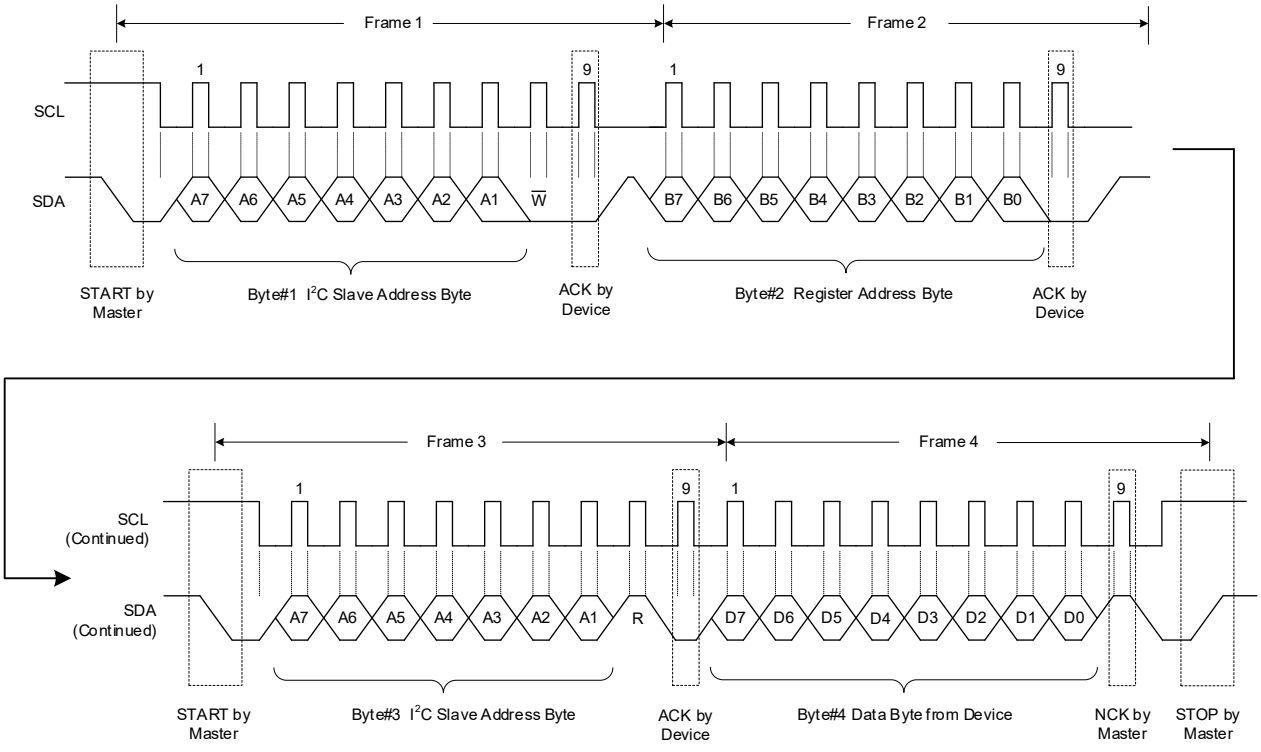


Figure 5. A Single Read Transaction (From SGM37601)

TIMING DIAGRAM (continued)

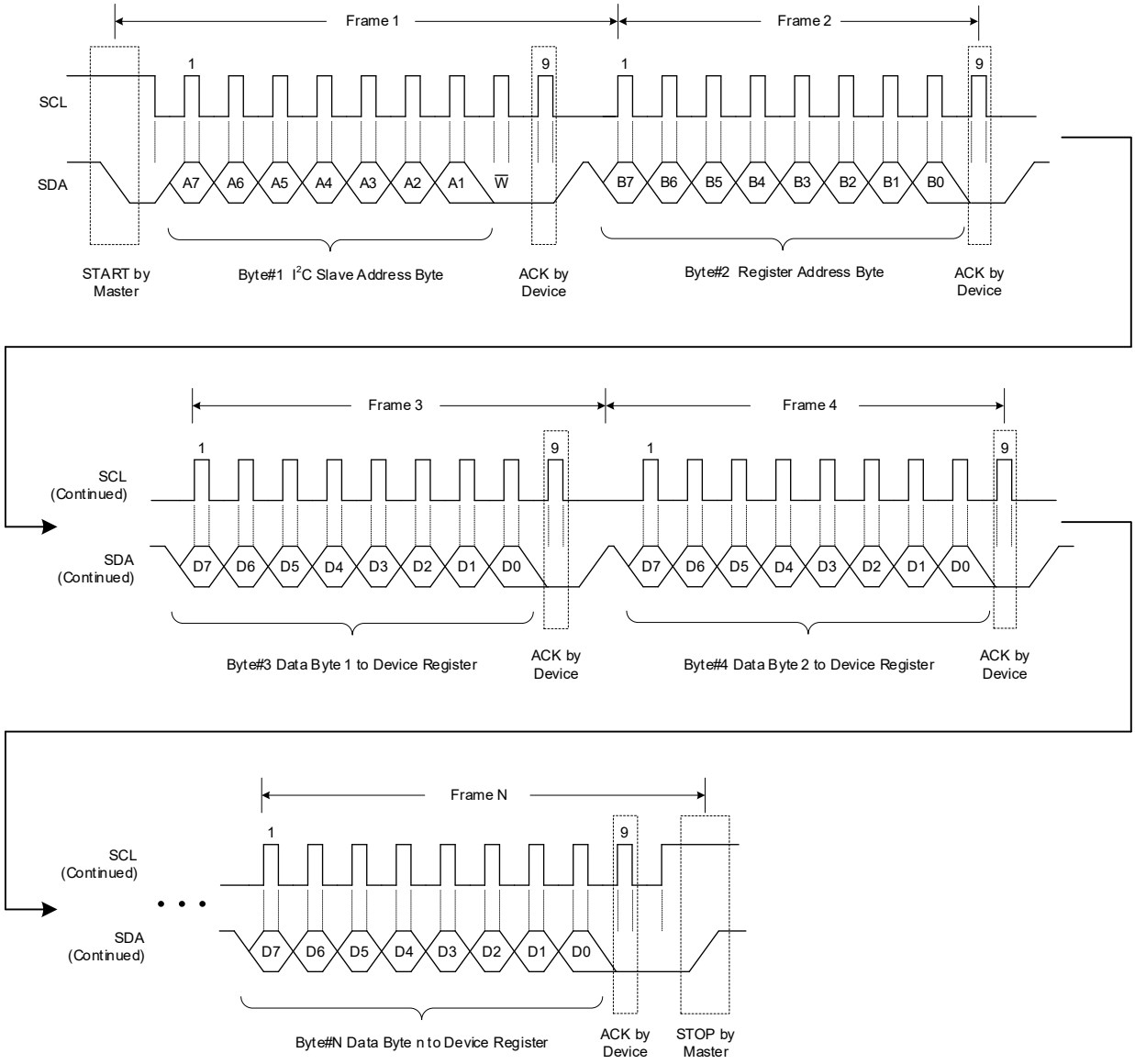


Figure 6. A Multi-Write Transaction (To SGM37601)

TIMING DIAGRAM (continued)

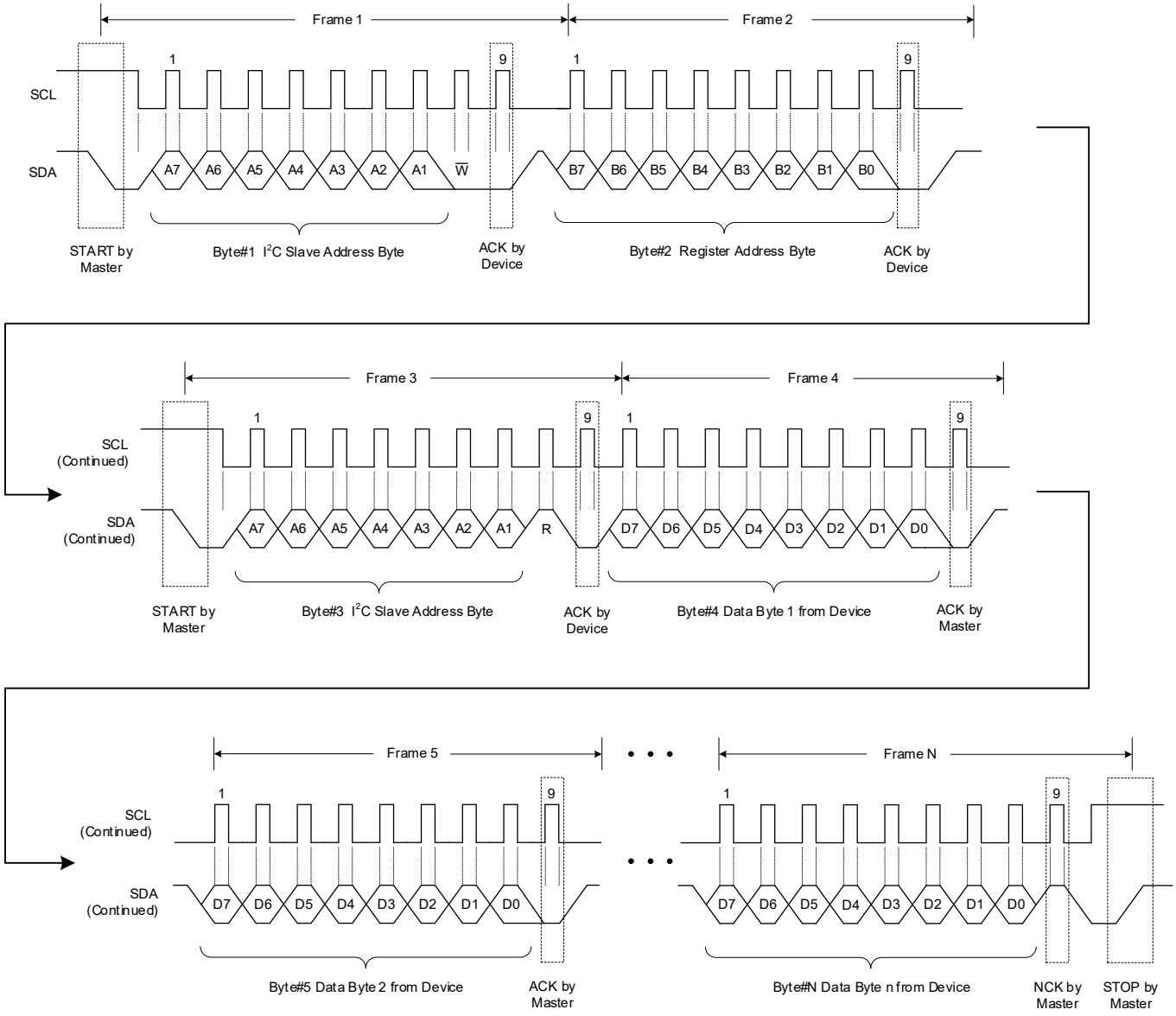


Figure 7. A Multi-Read Transaction (From SGM37601)

TIMING DIAGRAM (continued)

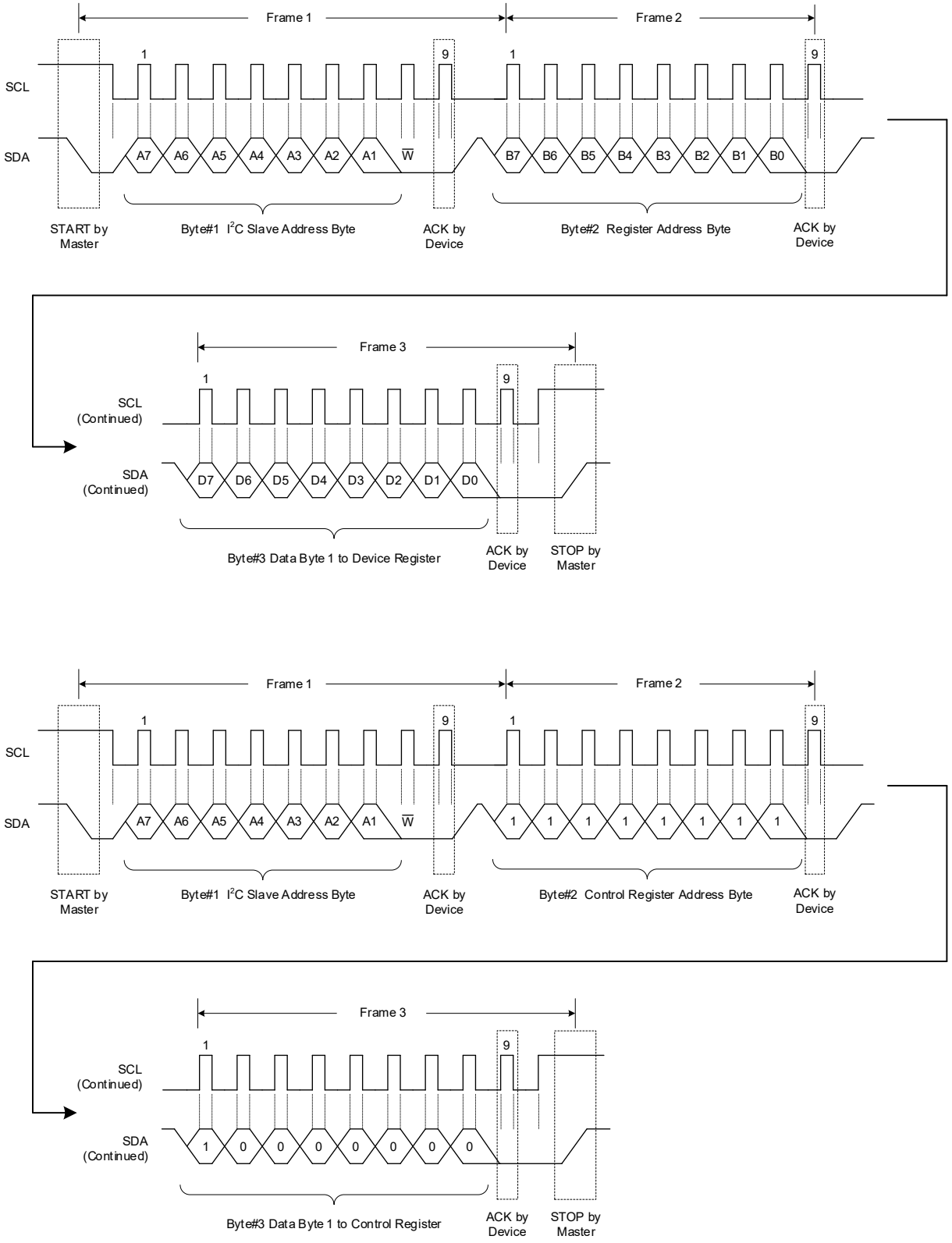


Figure 8. A Single Write Transaction (To EEPROM)

TIMING DIAGRAM (continued)

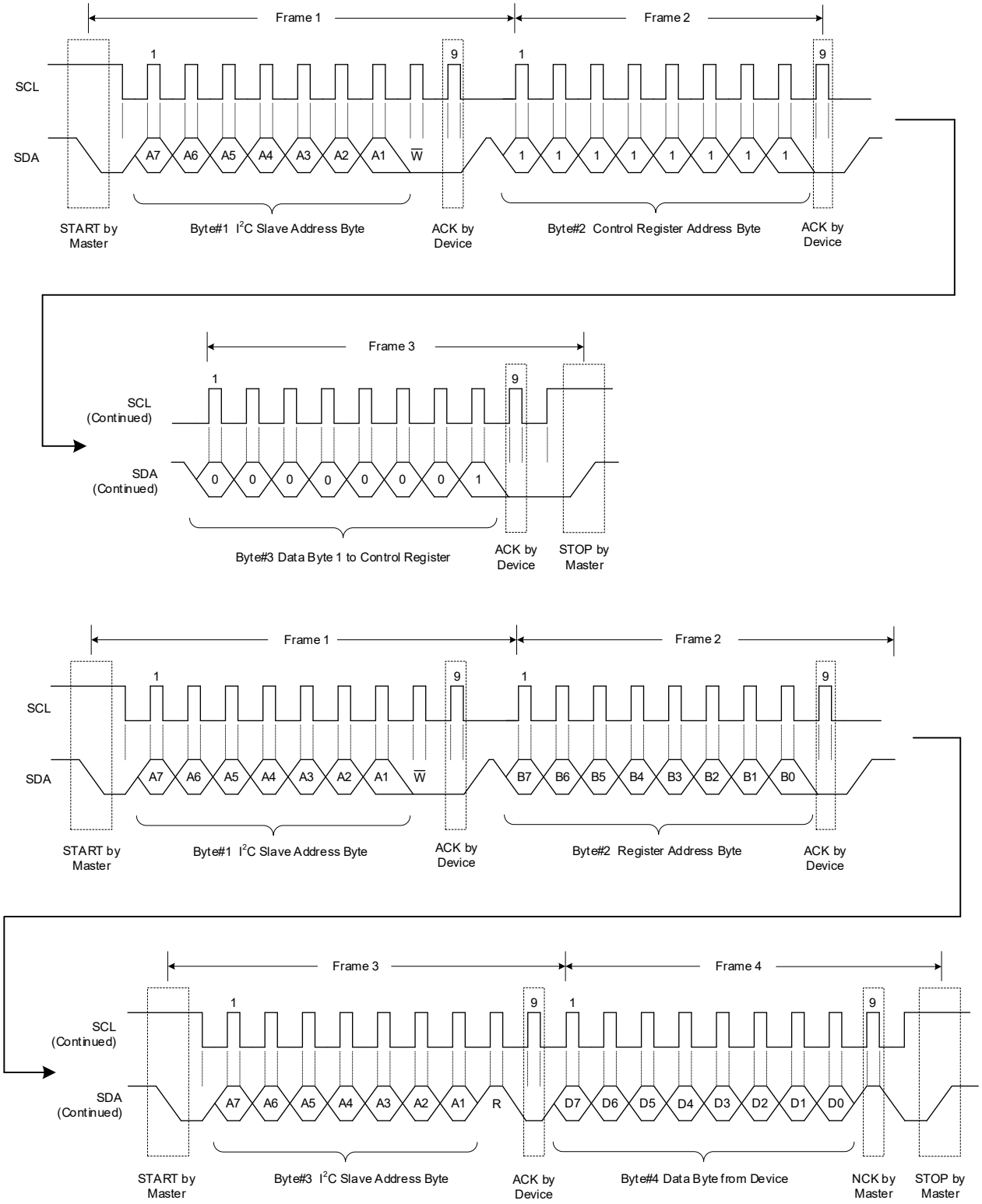


Figure 9. A Single Read Transaction (From EEPROM)

TIMING DIAGRAM (continued)

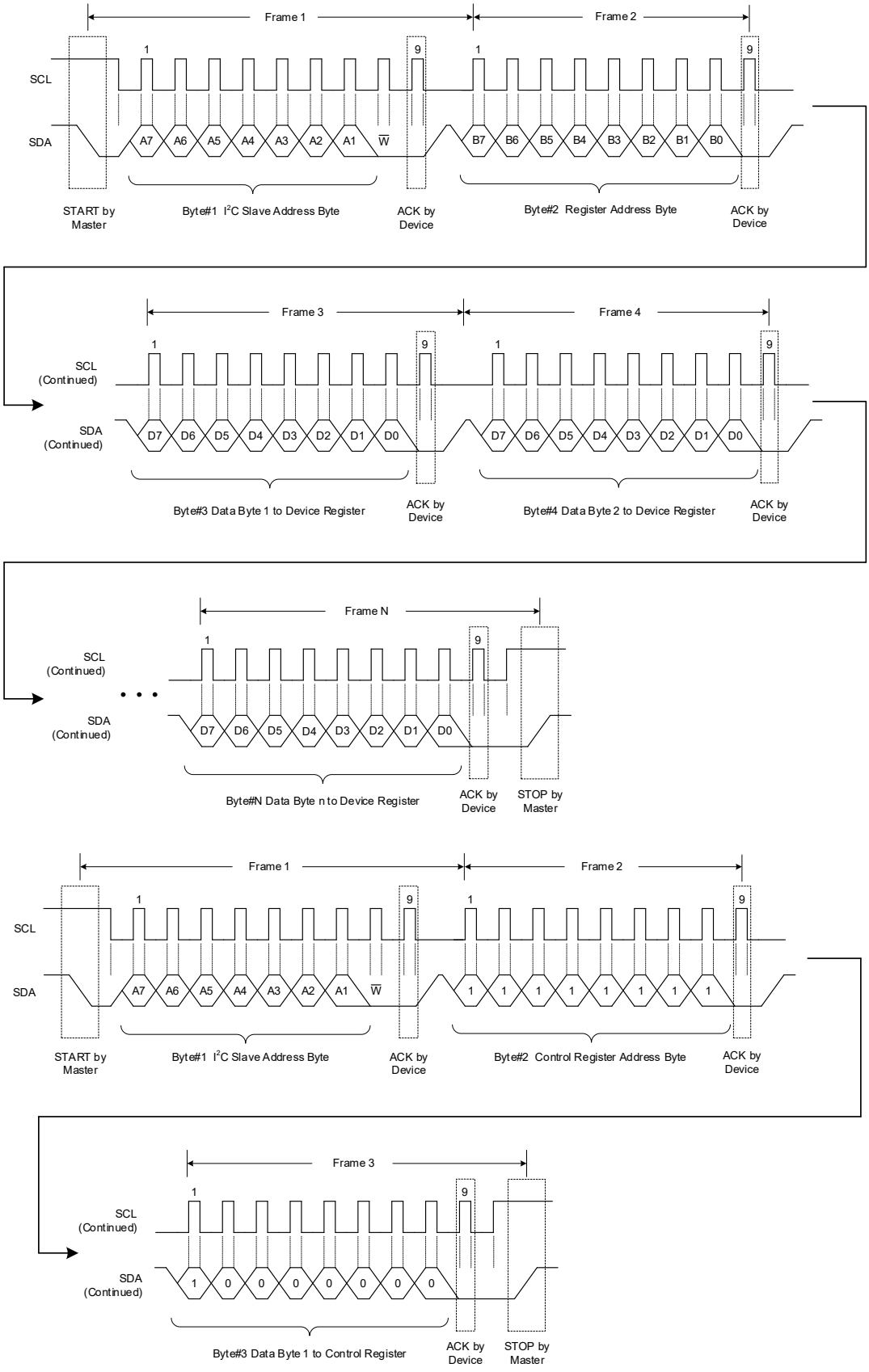


Figure 10. A Multi-Write Transaction (To EEPROM)

TIMING DIAGRAM (continued)

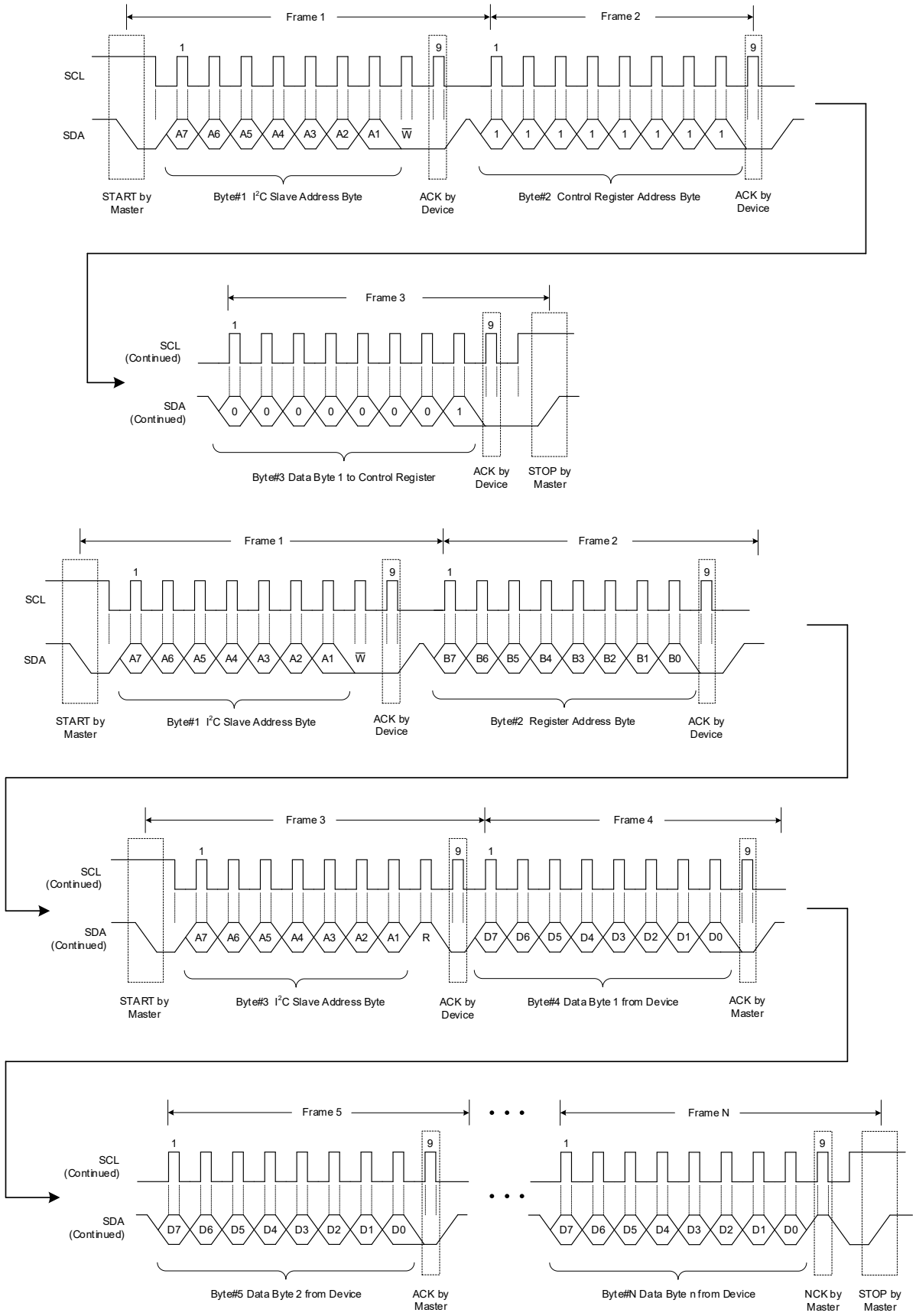
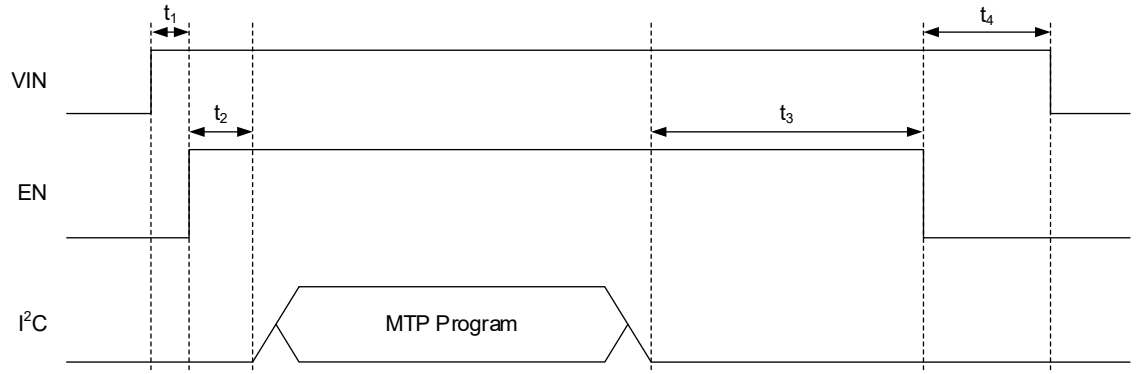


Figure 11. A Multi-Read Transaction (From EEPROM)

TIMING DIAGRAM (continued)

MTP Program Sequence



Write:

t_1 = 30ms, t_2 = 50ms, t_3 = 500ms, t_4 = 100ms

Read:

t_1 = 30ms, t_2 = 50ms, t_3 = 10ms, t_4 = 100ms

f_{SCL} = 400kHz

DETAILED DESCRIPTION

Overview

The SGM37601 is a 6-channel LED driver featuring programmable current output from 6mA to 25mA per channel. It operates as a peak current mode boost converter with an integrated 40V, 155mΩ power switch and supports an input voltage range of 2.8V to 24V.

Device flexibly configure parameters including Dimming mode, LED current, switching frequency, inductor current limit, and compensation method are configurable via the I²C interface. The device incorporates comprehensive protection features such as VIN UVLO, output OVP, LED Open/Short/OVP, and OTP.

It supports four dimming modes: DC Mode, PWM Mode, Mix mode, and Mix mode with 26kHz modulation, with PWM dimming frequencies ranging from 100Hz to 20kHz to accommodate various application needs. The SGM37601 offers high efficiency, excellent current accuracy, and superior channel-to-channel current matching.

Soft-Start Function

When V_{IN} exceeds the UVLO threshold and the EN pin voltage rises above its logic-high level, the internal VDC rail is regulated to approximately 3.3V, provided that VIN remains above this level. The SGM37601 also incorporates a soft-start function that activates once the VIN, EN, and PWM signals are ready, independent of their power-on sequence. After a brief delay, the LED current ramps up linearly to the target value set by the ILED[7:0] bits. The soft-start duration varies with the operating mode (PWM or Mix-mode) and PWM duty cycle, ensuring smooth brightness transition and improved user experience while supporting arbitrary power-on sequences.

Brightness Control through the I²C Interface

The output current of each channel is programmed via the 8-bit ILED[7:0] bits field in REG0x01 register. It provides precise control through 191 digital steps with a resolution of 0.1mA per step and 00h programs 0mA.

Brightness Control through the PWM Pin

The SGM37601 offers four configurable dimming modes for LED brightness control: PWM, DC, Mix, and Mix-26kHz. The desired mode is selected using the DMS[1:0] bits in REG0x00 register. It supports Direct PWM, PWM-to-Analog, PWM-to-Mixed, and PWM-to-Mixed-26kHz dimming operations with a PWM frequency of up to 2kHz and 12-bit resolution.

PWM Dimming Mode (DMS[1:0] = 00)

In this mode, the current sources are synchronized with the PWM signal, switching on and off accordingly. The LED current frequency matches the PWM input frequency.

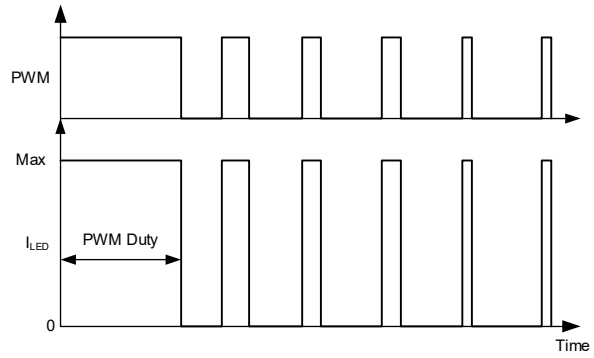


Figure 12. PWM Dimming

DC Dimming Mode (DMS[1:0] = 01)

The DC dimming mode introduces a two-cycle delay: the first cycle detects the PWM duty ratio, and the second cycle calculates the LED current reference. And at the beginning of the third cycle, the channel current starts to fade in or out. The average LED current is then set based on the measured duty ratio.

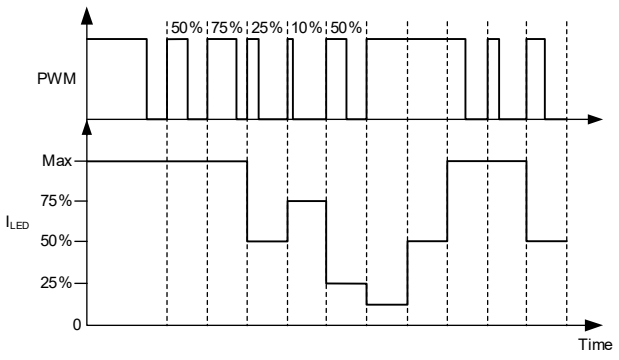


Figure 13. DC Dimming

Mix Dimming Mode (DMS[1:0] = 10)

This mode combines analog and PWM dimming. When the PWM duty cycle is between 25% and 100%, the output uses DC dimming with current amplitude scaled proportionally. When the PWM duty cycle is below 25%, it switches to a PWM dimming method where the current is fixed at 25% of the full-scale value and the effective dimming duty becomes four times the input PWM duty cycle.

DETAILED DESCRIPTION (continued)

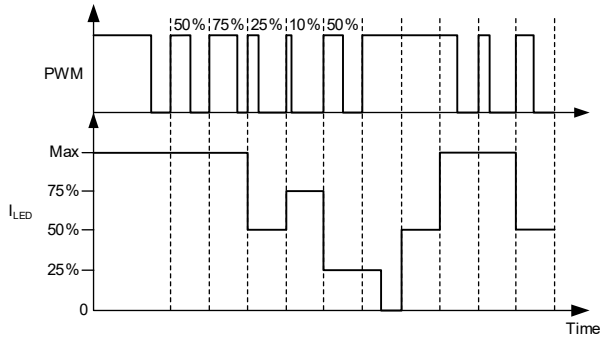


Figure 14. Mix Mode Dimming

Mix-26k Dimming Mode (DMS[1:0] = 11)

Similar to Mix mode, this option operates at a fixed 26kHz high frequency. It ensures inaudible operation while maintaining the same dimming principle: DC-based amplitude modulation above 25% duty cycle and PWM dimming below.

NOTE: During DC/Mix/Mix-26k mode dimming, when PWM Duty = 100% and 0% I_{LED} behavior is shown in Figure 15.

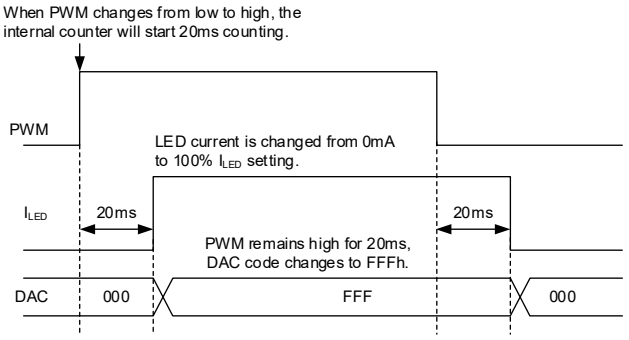


Figure 15. Duty 100% and 0% I_{LED} Behavior

LED Adaptive Control

The SGM37601 continuously monitors all LEDx pin voltages and selects the minimum value for feedback through the error amplifier (EA). This ensures that the lowest LED pin voltage is maintained at approximately 500mV (default value), allowing the boost converter to regulate the output to match the highest forward voltage among all LED strings. The headroom voltage can be configured via I²C using LED_HEADROOM[1:0] bits. The maximum configurable headroom voltage is 560mV.

Boost Switching Frequency Setting

The switching frequency of the Boost converter in the SGM37601 is configurable via the I² C interface. Using the BOOST_FSW[3:0] bits, the frequency can be programmed across a range of 100kHz to 1.6MHz, with specific step resolution defined in the corresponding register settings.

SW Slew Rate Control

The SGM37601 provides programmable SW slew rate control via the SW_RATE[1:0] Bits, enabling optimization of switching edge rates to reduce high-frequency noise and facilitate compliance with EMI requirements.

PFM Function

The SGM37601 supports a PFM (Pulse Frequency Modulation) mode, enabled via the EN_PFM bit in REG0x03, which enhances light-load efficiency by reducing switching losses and minimizing power consumption under low-load conditions. The minimum PFM switching frequency is configurable through the PFM_LOWEST_FSW[5:0] bits, allowing the user to set a frequency threshold above the audible range to avoid noise and ensure reliable performance in audio-sensitive applications.

Entry into PFM mode is determined by the minimum on-time set via the TON_L_PFM[2:0] bits, while exit is controlled by the TON_H_PFM[2:0] bits. These settings allow flexible optimization of light-load efficiency under various application conditions such as switching frequency, output LED voltage, and LED current.

Additionally, when operating in PFM mode, the PFM_SLOW_EN bit can be enabled to control the rate of frequency change, thereby improving stability during frequency modulation.

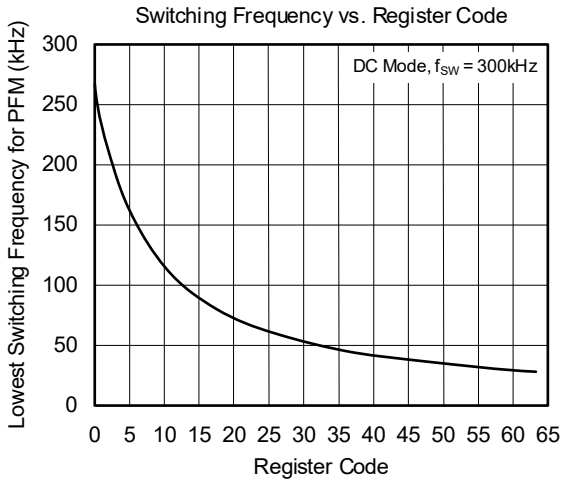


Figure 16. Switching Frequency vs. PFM_LOWEST_FSW[5:0] Code

DETAILED DESCRIPTION (continued)

Fade IN/OUT Time Control

The fade parameters are configured via I²C register REG0x08. The FTIME_THD bit sets the duty cycle threshold (relative to the full-scale I_{LED} current) for adaptive fade control: when this bit is set to 0, step time adjustment applies below 12.5% duty cycle; while this bit is set to 1, it applies below 25%. Below the threshold (12.5%×I_{LED} or 25%×I_{LED}), step time is controlled by FTIME_SEL1[2:0], and above the threshold, it is controlled by FTIME_SEL2[2:0]. The maximum configurable fade time is 16384μs, enabling smooth brightness transitions.

Boost Loop Compensation

The SGM37601 provides both internal and external compensation modes to optimize loop performance, configurable via the SET_BOOST bit. Internal compensation is enabled by default and allows real-time adjustment of loop characteristics through I²C programming of the RCOMP_SEL[1:0] bits, facilitating efficient in-system debugging without external components.

For applications requiring higher precision, external compensation utilizes an RC network connected to the COMP pin which is the output of the internal error amplifier, together with the GM_OPTION[1:0] bits for transconductance fine-tuning. The external resistor and capacitor values determine the integrator's gain bandwidth and zero frequency, enabling optimized transient response and stability.

Additionally, slope compensation can be adjusted in real time through the SLOP_COMP_SEL[1:0] bits, supporting diverse application conditions without BOM changes. This flexibility allows designers to rapidly adapt to various operating scenarios and shorten development cycles.

MTP (Non-Volatile Memory) Function

The SGM37601 supports multiple-time programmable (MTP) memory for parameter storage and retrieval. MTP programming and reading are managed through the I²C interface via REG0xFF register. A 5V supply voltage is required to perform writes to the MTP memory.

At power-on, the default values stored in the MTP are loaded into the corresponding I²C control registers. During operation, all device settings can be adjusted directly through the I²C registers without modifying the underlying MTP data. To update the non-volatile MTP defaults, first write the desired configuration to the I²C registers, and then program them into MTP by writing the value 0x80 to address REG0xFF.

Protections in Fault Operation

Under-Voltage Lockout (UVLO)

The SGM37601 features a configurable VIN UVLO threshold programmable via the VIN_UVLO[1:0] bits, with a default value of 2.7V. The device becomes operational when the input voltage exceeds the configured UVLO threshold (typically 2.7V for startup). If both the PWM and EN signals are present, a soft-start sequence is initiated. The device shuts down when the input voltage falls below the configured UVLO threshold 2.49V. The maximum programmable UVLO threshold is 3.8V.

LED Open Detection

The SGM37601 identifies an LED channel as open when its pin voltage falls below the 130mV entry threshold. The faulty channel is automatically disabled and excluded from the minimum voltage selection to ensure proper regulation of the remaining active channels. This state is non-latching, and normal operation resumes once the pin voltage rises above the exit threshold upon reconnection. Unused LEDx pins can be left floating or connected to AGND. If left unconnected, ensure sufficient noise immunity to prevent false triggering that may interfere with active LED channels. If all LEDx channels are open, the output voltage is clamped at the programmed over-voltage protection (OVP) level to maintain system safety.

Channel LED OVP Level

The SGM37601 continuously monitors the minimum voltage among all LEDx channels. When this voltage exceeds the configured LED OVP threshold, the internal switch is disabled. It is re-enabled once the minimum LEDx voltage falls back below the OVP threshold. As a result, the minimum LEDx voltage is effectively clamped at the programmed OVP level, preventing excessive voltage and avoiding LED thermal damage. The OVP threshold is programmable via the LED_OVP[1:0] bits.

DETAILED DESCRIPTION (continued)

Channel LED Short Protection

The SGM37601 incorporates a LED Short Protection (SLP) function. During operation, if the voltage on any LEDx pin exceeds approximately 5.5V, that channel is immediately turned off and latched into a protected state. The SLP feature can be enabled or disabled via the LED_SHORT control bit. Setting LED_SHORT = 1 enables the protection, and setting LED_SHORT = 0 disables it. A latched channel resulting from a short event can be reset by toggling the EN pin or through an UVLO cycle.

Current Limit Protection

The SGM37601 provides over-current protection (OCP) by limiting the peak inductor current. It senses the inductor current during the on time. The duty cycle is determined by comparing the sensed current signal, along with internal slope compensation, with the error amplifier output. The peak current limit threshold is configurable via the ILIM_SEL[1:0] bits to accommodate different application requirements. If the inductor current exceeds the set limit, the device immediately stops switching for the remainder of the current cycle. Normal operation resumes at the beginning of the next switching cycle. In cases where the over-current condition persists, the SGM37601 will operate repeatedly in this current-limited state.

Over-Voltage Protection

The SGM37601 incorporates an over-voltage protection (OVP) function, which can be configured via I²C interface. The protection mechanism employs a comparator to monitor the voltage at the OVP pin. When this voltage exceeds the programmed OVP threshold, the device enters a protective state after a delay of several microseconds: switching is halted to cease energy transfer from the input to the output. Once the OVP pin voltage decreases by the specified hysteresis value, the boost converter resumes normal switching operation. The OVP threshold voltage is programmable through the OVP[4:0] configuration bits.

Over-Temperature Protection

The over-temperature protection (OTP) is activated when the device's junction temperature exceeds the threshold configured via the OTP_OPTION[1:0] bits. Upon triggering, the SGM37601 immediately stops switching. Once the junction temperature decreases by the typical hysteresis value of 20°C, the Boost converter restarts automatically, and the LED driver resumes normal operation.

REGISTER MAP

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

Slave Device Address: b0110110/b0110111 + R/W

Register Address	Default Value	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x00	01h	Reserved						DMS[1:0]	
0x01	8Dh	ILED[7:0]							
0x02	E9h	SET_BOOST	OVP[4:0]					VIN_UVLO[1:0]	
0x03	24h	Reserved		EN_PFM	Reserved	BOOST_FSW[3:0]			
0x04	F3h	PFM_LOWEST_FSW[5:0]						SW_RATE[1:0]	
0x06	22h	Reserved						LED_HEADROOM[1:0]	
0x07	00h	Reserved			LED_SHORT	Reserved		LED_OVP[1:0]	
0x08	00h	Reserved	FTIME_THD	FTIME_SEL2[2:0]			FTIME_SEL1[2:0]		
0x09	21h	Reserved		RCOMP_SEL[1:0]		Reserved		SLOP_COMP_SEL[1:0]	
0x0A	12h	Reserved	TON_L_PFM[2:0]			Reserved		ILIM_SEL[1:0]	
0x0B	41h	GM_OPTION[1:0]		PFM_SLOW_EN	OTP_OPTION[1:0]		TON_H_PFM[2:0]		
0xFF	00h	MTP_P	Reserved						MTP_R

Bit Type:
R/W: Read/Write

REG0x00: Dimming Mode Selection Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	000000	R/W	Reserved
D[1:0]	DMS[1:0]	01	R/W	Dimming Mode Selection 00 = PWM Mode 01 = DC Mode (default) 10 = Mix Mode 11 = Mix-26kHz Mode

REG0x01: LED Current Setting Register [Reset = 0x8D]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	ILED[7:0]	10001101	R/W	Maximum LED Current Level. Each LED current can be set by I²C command. Range: 6mA (00000001) to 25mA (10111111), 0mA (00000000) (See Table 1) Default: 20mA (10001101)

REGISTER MAP (continued)

Table 1. LED Current Setting

ILED[7:0] (hex)	I_{LED} (mA)	ILED[7:0] (hex)	I_{LED} (mA)	ILED[7:0] (hex)	I_{LED} (mA)	ILED[7:0] (hex)	I_{LED} (mA)	ILED[7:0] (hex)	I_{LED} (mA)	ILED[7:0] (hex)	I_{LED} (mA)
0x00	0	0x21	9.2	0x42	12.5	0x63	15.8	0x84	19.1	0xA5	22.4
0x01	6.0	0x22	9.3	0x43	12.6	0x64	15.9	0x85	19.2	0xA6	22.5
0x02	6.1	0x23	9.4	0x44	12.7	0x65	16.0	0x86	19.3	0xA7	22.6
0x03	6.2	0x24	9.5	0x45	12.8	0x66	16.1	0x87	19.4	0xA8	22.7
0x04	6.3	0x25	9.6	0x46	12.9	0x67	16.2	0x88	19.5	0xA9	22.8
0x05	6.4	0x26	9.7	0x47	13.0	0x68	16.3	0x89	19.6	0xAA	22.9
0x06	6.5	0x27	9.8	0x48	13.1	0x69	16.4	0x8A	19.7	0xAB	23.0
0x07	6.6	0x28	9.9	0x49	13.2	0x6A	16.5	0x8B	19.8	0xAC	23.1
0x08	6.7	0x29	10.0	0x4A	13.3	0x6B	16.6	0x8C	19.9	0xAD	23.2
0x09	6.8	0x2A	10.1	0x4B	13.4	0x6C	16.7	0x8D	20.0	0xAE	23.3
0x0A	6.9	0x2B	10.2	0x4C	13.5	0x6D	16.8	0x8E	20.1	0xAF	23.4
0x0B	7.0	0x2C	10.3	0x4D	13.6	0x6E	16.9	0x8F	20.2	0xB0	23.5
0x0C	7.1	0x2D	10.4	0x4E	13.7	0x6F	17.0	0x90	20.3	0xB1	23.6
0x0D	7.2	0x2E	10.5	0x4F	13.8	0x70	17.1	0x91	20.4	0xB2	23.7
0x0E	7.3	0x2F	10.6	0x50	13.9	0x71	17.2	0x92	20.5	0xB3	23.8
0x0F	7.4	0x30	10.7	0x51	14.0	0x72	17.3	0x93	20.6	0xB4	23.9
0x10	7.5	0x31	10.8	0x52	14.1	0x73	17.4	0x94	20.7	0xB5	24.0
0x11	7.6	0x32	10.9	0x53	14.2	0x74	17.5	0x95	20.8	0xB6	24.1
0x12	7.7	0x33	11.0	0x54	14.3	0x75	17.6	0x96	20.9	0xB7	24.2
0x13	7.8	0x34	11.1	0x55	14.4	0x76	17.7	0x97	21.0	0xB8	24.3
0x14	7.9	0x35	11.2	0x56	14.5	0x77	17.8	0x98	21.1	0xB9	24.4
0x15	8.0	0x36	11.3	0x57	14.6	0x78	17.9	0x99	21.2	0xBA	24.5
0x16	8.1	0x37	11.4	0x58	14.7	0x79	18.0	0x9A	21.3	0xBB	24.6
0x17	8.2	0x38	11.5	0x59	14.8	0x7A	18.1	0x9B	21.4	0xBC	24.7
0x18	8.3	0x39	11.6	0x5A	14.9	0x7B	18.2	0x9C	21.5	0xBD	24.8
0x19	8.4	0x3A	11.7	0x5B	15.0	0x7C	18.3	0x9D	21.6	0xBE	24.9
0x1A	8.5	0x3B	11.8	0x5C	15.1	0x7D	18.4	0x9E	21.7	0xBF	25.0
0x1B	8.6	0x3C	11.9	0x5D	15.2	0x7E	18.5	0x9F	21.8		
0x1C	8.7	0x3D	12.0	0x5E	15.3	0x7F	18.6	0xA0	21.9		
0x1D	8.8	0x3E	12.1	0x5F	15.4	0x80	18.7	0xA1	22.0		
0x1E	8.9	0x3F	12.2	0x60	15.5	0x81	18.8	0xA2	22.1		
0x1F	9.0	0x40	12.3	0x61	15.6	0x82	18.9	0xA3	22.2		
0x20	9.1	0x41	12.4	0x62	15.7	0x83	19.0	0xA4	22.3		

REGISTER MAP (continued)

REG0x02: VIN UVLO, OTP and Boost Compensation Register [Reset = 0xE9]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	SET_BOOST	1	R/W	Boost Compensation 0 = External 1 = Internal (default)
D[6:2]	OVP[4:0]	11010	R/W	Over-Voltage Protection Selection V_{OVP} = OVP[4:0] × 1V + 10V Range: 10V (00000) to 41V (11111) (see Table 2) Default: 36V (11010)
D[1:0]	VIN_UVLO[1:0]	01	R/W	VIN UVLO Selection 00 = 2.4V 01 = 2.7V (default) 10 = 3.2V 11 = 3.8V

Table 2. Boost Output Over-Voltage Setting

OVP[4:0] (hex)	Boost Output Over-Voltage (V)	OVP[4:0] (hex)	Boost Output Over-Voltage (V)
0x00	10	0x10	26
0x01	11	0x11	27
0x02	12	0x12	28
0x03	13	0x13	29
0x04	14	0x14	30
0x05	15	0x15	31
0x06	16	0x16	32
0x07	17	0x17	33
0x08	18	0x18	34
0x09	19	0x19	35
0x0A	20	0x1A	36
0x0B	21	0x1B	37
0x0C	22	0x1C	38
0x0D	23	0x1D	39
0x0E	24	0x1E	40
0x0F	25	0x1F	41

REGISTER MAP (continued)

REG0x03: Boost Switching Frequency Setting Register [Reset = 0x24]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/W	Reserved
D[5]	EN_PFM	1	R/W	PFM Function Enable 0 = OFF 1 = ON (default)
D[4]	Reserved	0	R/W	Reserved
D[3:0]	BOOST_FSW[3:0]	0100	R/W	Boost Switching Frequency (f_{SW}) 0000 = 100kHz 0001 = 150kHz 0010 = 200kHz 0011 = 250kHz 0100 = 300kHz (default) 0101 = 400kHz 0110 = 500kHz 0111 = 600kHz 1000 = 700kHz 1001 = 800kHz 1010 = 900kHz 1011 = 1000kHz 1100 = 1225kHz 1101 = 1335kHz 1110 = 1450kHz 1111 = 1600kHz

REG0x04: SW Slew Rate and Switching Frequency of PFM Control Register [Reset = 0xF3]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	PFM_LOWEST_FSW[5:0]	111100	R/W	Lowest Switching Frequency for PFM Lowest switching frequency setting: = 16000/{16000/f_{SW} + (8 × DAC) + 7} where DAC is the lowest switching frequency for PFM setting. NOTE: The PFM function can be enabled by EN_PFM bit. When EN_PFM = 0, the Boost switching frequency is just determined by the switching frequency setting. When EN_PFM = 1 and the Boost on time < the minimum on time, the Boost switching frequency is decreased.
D[1:0]	SW_RATE[1:0]	11	R/W	SW Edge Rate Control 00 = 200% 01 = 50% 10 = 100% 11 = 200% (default)

REG0x06: LED Driver Headroom Setting Register [Reset = 0x22]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	001000	R/W	Reserved
D[1:0]	LED_HEADROOM[1:0]	10	R/W	LED Driver Headroom 00 = 400mV 01 = 460mV 10 = 500mV (default) 11 = 560mV

REGISTER MAP (continued)

REG0x07: LED Protection Setting Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000	R/W	Reserved
D[4]	LED_SHORT	0	R/W	LED Short Protection 0 = OFF (default) 1 = ON
D[3:2]	Reserved	00	R/W	Reserved
D[1:0]	LED_OVP[1:0]	00	R/W	LED OVP Level 00 = 2.1V (default) 01 = 2.52V 10 = 2.8V 11 = 3.5V

REG0x08: Fade IN/OUT Time Control Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6]	FTIME_THD	0	R/W	Fading Time Duty Change Threshold 0 = 12.5% (default) 1 = 25%
D[5:3]	FTIME_SEL2[2:0]	000	R/W	Fading Time Selection (Duty > Fading Time Duty Change) 000 = 1μs (default) 001 = 4μs 010 = 16μs 011 = 64μs 100 = 512μs 101 = 1024μs 110 = 2048μs 111 = 4096μs
D[2:0]	FTIME_SEL1[2:0]	000	R/W	Fading Time Selection (Duty < Fading Time Duty Change) 000 = 1μs (default) 001 = 4μs 010 = 16μs 011 = 64μs 100 = 1024μs 101 = 4096μs 110 = 8192μs 111 = 16384μs

REG0x09: COMP Control Register [Reset = 0x21]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/W	Reserved
D[5:4]	RCOMP_SEL[1:0]	10	R/W	R_{COMP} Select Control 00 = 100kΩ 01 = 200kΩ 10 = 400kΩ (default) 11 = 800kΩ
D[3:2]	Reserved	00	R/W	Reserved
D[1:0]	SLOP_COMP_SEL[1:0]	01	R/W	Slope Compensation Select at f_{SW} = 1000kHz 00 = slope = 1V/μs 01 = slope = 1.5V/μs (default) 10 = slope = 0.5V/μs 11 = slope = 1V/μs

REGISTER MAP (continued)

REG0x0A: Control Register [Reset = 0x12]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:4]	TON_L_PFM[2:0]	001	R/W	PFM ON Time ($t_{ON_L_PFM}$) Select 000 = 250ns 001 = 300ns (default) 010 = 350ns 011 = 400ns 100 = 450ns 101 = 500ns 110 = 550ns 111 = 600ns
D[3:2]	Reserved	00	R/W	Reserved
D[1:0]	ILIM_SEL[1:0]	10	R/W	Peak Limit (I_{LIM}) Select 00 = 1.8A 01 = 2.1A 10 = 2.5A (default) 11 = 3.0A

REG0x0B: Control Register [Reset = 0x41]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	GM_OPTION[1:0]	01	R/W	GM Option 00 = 3.2μA/V 01 = 6.4μA/V (default) 10 = 12.8μA/V 11 = 51.2μA/V
D[5]	PFM_SLOW_EN	0	R/W	PFM SLOW Function Enable Control 0 = PFM SLOW function disable (default) 1 = PFM SLOW function enable
D[4:3]	OTP_OPTION[1:0]	00	R/W	Over-Temperature Protection (OTP) Select 00 = 140℃ (default) 01 = 145℃ 10 = 150℃ 11 = 155℃
D[2:0]	TON_H_PFM[2:0]	001	R/W	PFM ON Time ($t_{ON_H_PFM}$) Select 000 = 300ns 001 = 350ns (default) 010 = 400ns 011 = 450ns 100 = 500ns 101 = 550ns 110 = 600ns 111 = 650ns

REG0xFF: SW Slew Rate Control Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	MTP_P	0	R/W	MTP Programming 0 = normal operation (default) 1 = start MTP programming sequence
D[6:1]	Reserved	000000	R/W	Reserved
D[0]	MTP_R	0	R/W	MTP Read 0 = I²C read data from DAC (default) 1 = I²C read data from MTP

APPLICATION INFORMATION

Input Capacitor Selection

The input of the entire controller can be divided into two parts. One part is the input of the Boost converter. Boost converter input capacitor has continuous current throughout the entire switching cycle. A 4.7μF ceramic capacitor is recommended to place as close as possible between the VIN pin and PGND pin. The other input is the input of the chip. High-frequency noise suppression can be achieved by configuring an RC filter to prevent false triggering of the under-voltage lockout (UVLO). It is recommended to use a resistor of 10Ω and a capacitor of 1μF.

Output Capacitor Selection

The output capacitor in a power supply or LED driver must meet ripple voltage requirement.

This ripple section is composed of two components. One component results from the voltage variations caused by the charging and discharging of the capacitor, while the other is the product of the inductor current ripple and the equivalent series resistance (ESR) of the output capacitor.

Calculating the value of ΔV_{OUT} based on the below formula:

$$\Delta V_{OUT} = \frac{D \times I_{OUT}}{C_{OUT} \times f_{SW}} \quad (1)$$

Ultimately, taking the equivalent series resistance (ESR) into account, the total output ripple voltage can be calculated by the below formula:

$$\Delta V_{OUT} = R_{ESR} \times \left(\frac{I_{OUT} \times V_{OUT}}{V_{IN}} + \frac{\Delta I_L}{2}\right) + \frac{D \times I_{OUT}}{C_{OUT} \times f_{SW}} \quad (2)$$

Ensure the capacitor ESR (Equivalent Series Resistance) low enough to prevent excessive power dissipation and thermal stress.

Inductor Selection

The selection of the inductor for SGM37601 should be based on the configuration of the input voltage, output voltage, LED channel current, and switching frequency. Under normal circumstances, it is recommended to use an inductor with an inductance value of 10μH or 4.7μH. The inductance value can ultimately be calculated by the below formula:

$$L_1 = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT} \times f_{SW}} \quad (3)$$

where

I_{OUT} = the sum of the currents from every LED channel.

V_{IN} = the minimum input voltage.

f_{SW} = the Boost switching frequency.

V_{OUT} = the maximum output voltage.

In addition to the inductance value, the DCR (DC resistance) of the inductor, as well as its saturation current and rated current, needs to be considered. It is advisable that the saturation current of the inductor be greater than the maximum possible peak value of the inductor current in the application scenario. Generally, it should meet the peak current-limiting value of SGM37601.

Diode Selection

The selection of diodes for an asynchronous Boost converter is crucial to the efficiency and overall performance of the Boost circuit. It is recommended to use Schottky diode with lower junction capacitance, shorter recovery time and lower V_F as rectifier diodes. The average current of the selected Schottky diode should be greater than the sum of the maximum currents of all channels, with a certain margin ensured. Meanwhile, the withstand voltage capacity of the Schottky diode should be greater than the set value of OVP, with a certain margin ensured.

Loop Compensation

The SGM37601 utilizes internal compensation by default, which can be optimized for various applications through the RCOMP_SEL[1:0] bits. When external compensation is employed, the network must be carefully designed to ensure loop stability achieving high DC gain and sufficient phase margin at the target crossover frequency. Select R_{COMP} to optimize the high-frequency integrator gain for transient performance, and C_{COMP} to position the integrator zero for loop stability. The GM_OPTION[1:0] bits further allow internal GM adjustment to co-configure the overall loop response.

For a typical application (6P11S LED, 1.225MHz switching frequency, 25mA/channel, C_{OUT} = 4.7μF, L_1 = 10μH), recommended compensation values are provided in the table below.

Case	V_{IN} Range (V)	R_{COMP} (kΩ)	C_{COMP} (nF)
Case 1: PWM Mode	7 to 21	20	1
Case 2: DC Mode	5 to 21	5.1	22

APPLICATION INFORMATION (continued)

Converter bandwidth and stability must be balanced during compensation design.

In DC mode, where LED current is steady, Case 2 compensation is recommended for enhanced stability.

In PWM mode with pulsed loading, higher bandwidth (Case 1) improves ripple performance but requires careful consideration of input voltage range. If transient response is not critical, Case 2 can be used in both operating modes.

Layout Considerations

A well-designed PCB layout is critical for power switching converter circuits. To maximize the SGM37601's performance, strictly follow these layout guidelines:

Place power components L_1, D_1, C_{VIN}, and C_{OUT} close together to minimize the AC current loop. Place the PCB traces between these components as short and wide as possible due to the large current flow during operation.

Place L_1 and D_1 close to the SW pins. Place the traces short and wide.

Place C_{VIN} (input capacitor) close to the VIN pin.

Place C_{OUT} (output capacitor) close to the VOUT pin.

Place the compensation components close to COMP pin if external compensation is employed.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

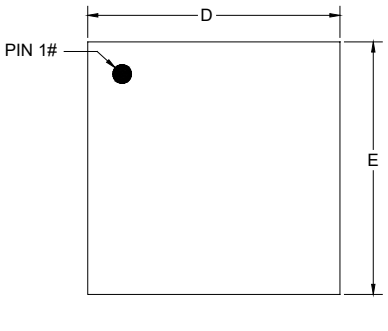
JUNE 2026 – REV.A.1 to REV.A.2	Page
Added Absolute Maximum Ratings section	2
Changed Electrical Characteristics section	5
Changed Figure 2	6

OCTOBER 2025 – REV.A to REV.A.1	Page
Modified Detailed Description section	23

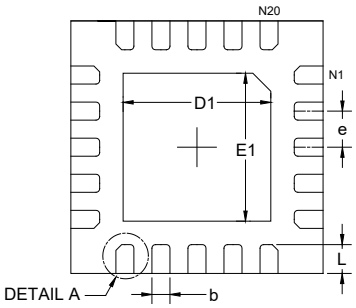
Changes from Original to REV.A (SEPTEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

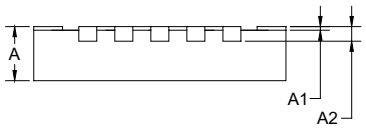
TQFN-3.5×3.5-20L



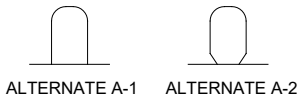
TOP VIEW



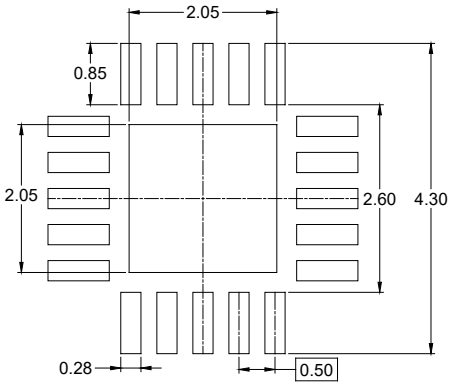
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



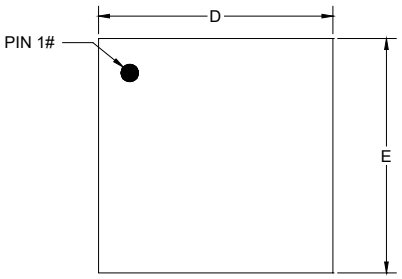
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	-	-	0.050
A2	0.203 REF		
D	3.450	3.500	3.550
D1	2.000	2.050	2.100
E	3.450	3.500	3.550
E1	2.000	2.050	2.100
b	0.200	0.250	0.300
e	0.500 BSC		
L	0.350	0.400	0.450

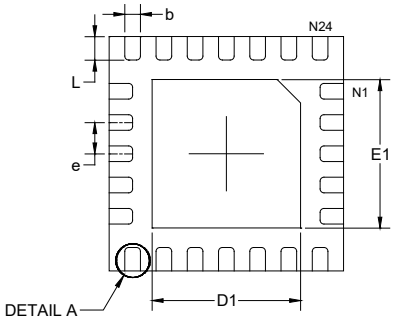
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

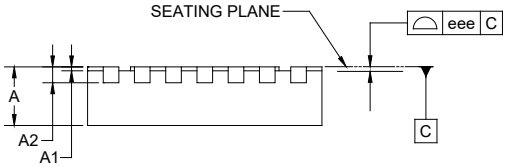
TQFN-3×3-24L



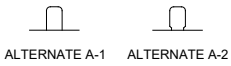
TOP VIEW



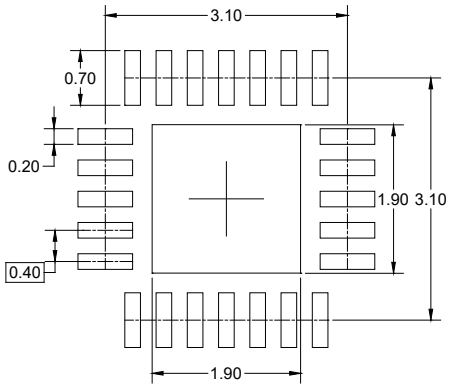
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



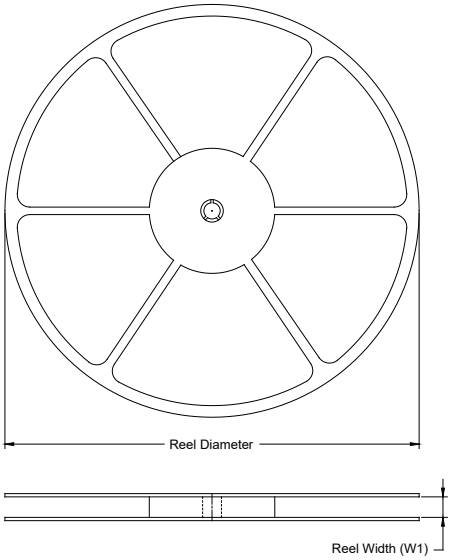
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.150	-	0.250
D	2.900	-	3.100
D1	1.800	-	2.000
E	2.900	-	3.100
E1	1.800	-	2.000
e		0.400 BSC	
L	0.200	-	0.400
eee		0.080	

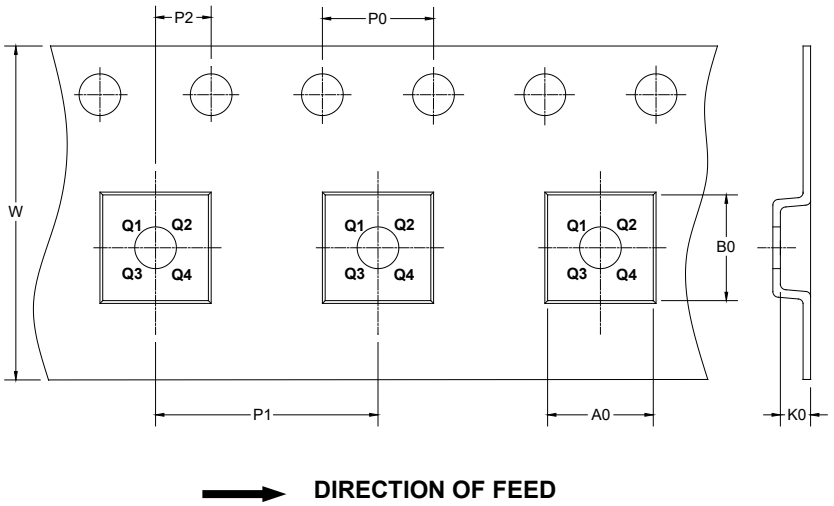
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



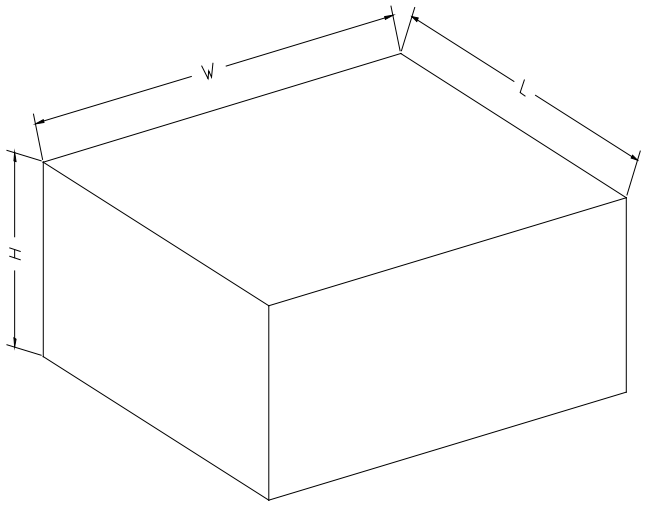
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3.5×3.5-20L	13"	12.4	3.80	3.80	0.95	4.0	8.0	2.0	12.0	Q2
TQFN-3×3-24L	13"	12.4	3.30	3.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002