SGM2546
2.7V to 23V, 7A, 10mΩ eFuse with Accurate Current Monitor and Transient Over-Current Blanking

GENERAL DESCRIPTION

The SGM2546 is a compact electronic fuse (eFuse) with a full suite of protection functions. With very few external components, the SGM2546 can provide multiple protection modes. To encounter overloads, output short-circuit, input voltage surges and high inrush current, the device is suitable as a robust defense.

The V_{OUT} rise time can be programmed by setting an additional capacitor to the SS pin, which can minimize inrush current. Programmable over-voltage protection is used to turn off the device or clamp the output to a fixed voltage (pin-selectable) if the IN rises over a threshold value. Under output overload condition, the over-current protection works which limits the current or cut-off the circuit. The output current limit threshold and the transient over-current blanking timer can be adjusted by the user. The ILIM pin is also used for load current monitoring.

The SGM2546 is available in a Green TQFN-2×2-10L package.

APPLICATIONS

Severs and Block Supplies
Motherboard Power Management
PCIE SSD

FEATURES

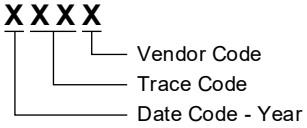
- **Input Voltage: 2.7V to 23V, Surge up to 28V**
- **Low On-Resistance: 10mΩ (TYP)**
- **Fast Over-Voltage Protection**
  - **SGM2546Ax/Cx: Adjustable Over-Voltage Lockout (OVLO) with 1.2μs (TYP) Response Time**
  - **SGM2546Bx: Pin-Selectable Threshold (3.91V, 5.81V, 13.95V) Over-Voltage Clamp (OVC) and 3μs Response Time (TYP)**
- **Over-Current Protection (OCP) with Load Current Monitor Output (ILIM)**
  - **Current Limit or Circuit-Breaker Option**
  - **Programmable Current Limit: 0.87A to 7.65A ±10% Accuracy for I_{LIM} > 1.74A**
  - **Programmable Transient Blanking Timer (ITIMER) Allowing Up to 2 × I_{LIM} Peak Currents**
  - **Load Current Monitor Accuracy: ±8% (MAX)**
- **Fast Short-Circuit Protection**
  - **Fast-Trip Response Time: 550ns (TYP)**
  - **Programmable (2 × I_{LIM}) and Fixed Thresholds**
- **Active High Enable Input with Adjustable Under-Voltage Lockout Threshold (EN/UVLO)**
- **Programmable Output Ramp Time (SS)**
- **Over-Temperature Protection**
- **Digital Outputs**
  - **Fault Indication (nFLT)**
  - **Power Good Indication (PG) with Adjustable Threshold (PGTH)**
- **Available in a Green TQFN-2×2-10L Package**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2546AR	TQFN-2×2-10L	-40℃ to +125℃	SGM2546ARXTSP10G/TR	14E XXXX	Tape and Reel, 3000
SGM2546AL	TQFN-2×2-10L	-40℃ to +125℃	SGM2546ALXTSP10G/TR	19W XXXX	Tape and Reel, 3000
SGM2546BR	TQFN-2×2-10L	-40℃ to +125℃	SGM2546BRXTSP10G/TR	19X XXXX	Tape and Reel, 3000
SGM2546BL	TQFN-2×2-10L	-40℃ to +125℃	SGM2546BLXTSP10G/TR	19Y XXXX	Tape and Reel, 3000
SGM2546CR	TQFN-2×2-10L	-40℃ to +125℃	SGM2546CRXTSP10G/TR	19Z XXXX	Tape and Reel, 3000
SGM2546CL	TQFN-2×2-10L	-40℃ to +125℃	SGM2546CLXTSP10G/TR	1A0 XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

SELECTABLE MODEL

Model	Over-Voltage Response	Over-Current Response	PG and PGTH	nFLT	Response to Fault
SGM2546AR	Adjustable OVLO	Active Current Limit	N	Y	Auto-Retry
SGM2546AL					Latch-Off
SGM2546BR	Pin Selectable OVC (3.92V/5.81V/13.95V)		Y	N	Auto-Retry
SGM2546BL					Latch-Off
SGM2546CR	Adjustable OVLO	Circuit-Breaker			Auto-Retry
SGM2546CL					Latch-Off

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range, V_{IN} ..... -0.3V to 28V
Output Voltage Range, V_{OUT} .....-0.3V to V_{IN} + 0.3V
Output Voltage Pulse (< 1μs), V_{OUT_PLS} .....-0.8V
Enable Voltage Range, $V_{EN/UVLO}$ ..... -0.3V to 6.5V
OVCSEL/OVLO Voltage Range, V_{OV} ..... -0.3V to 6.5V
SS Voltage Range, V_{SS} ..... Internally Limited
ITIMER Voltage Range, V_{ITIMER} ..... Internally Limited
PGTH Voltage Range, V_{PGTH} ..... -0.3V to 6.5V
PG Voltage Range, V_{PG} ..... -0.3V to 6.5V
nFLT Voltage Range, V_{nFLT} ..... -0.3V to 6.5V
ILIM Voltage Range, V_{ILIM} ..... Internally Limited
Continuous Switch Current, I_{MAX} ..... Internally Limited
Package Thermal Resistance
TQFN-2×2-10L, θ_{JA} ..... 69.9℃/W
TQFN-2×2-10L, θ_{JB} ..... 5.2℃/W
TQFN-2×2-10L, θ_{JC} ..... 50.9℃/W
Junction Temperature .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃
ESD Susceptibility (1) (2)
HBM.....±2000V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} .....2.7V to 23V (1)
Output Voltage Range, V_{OUT} ..... V_{IN} (MAX)
EN/UVLO Voltage Range, $V_{EN/UVLO}$.....5V (2) (MAX)
OVLO Voltage Range (SGM2546Ax/Cx) .....0.5V to 1.5V
SS Capacitor, C_{SS}.....3.3nF (MAX)
SS Capacitor Voltage Rating, V_{SS}..... V_{IN} + 5V (MIN)
PGTH Voltage Range, V_{PGTH} .....5V (MAX)
nFLT Voltage Range, V_{nFLT}.....5V (MAX)
PG Voltage Range, V_{PG}..... 5V (MAX)
ITIMER Capacitor Voltage Rating, V_{ITIMER} ..... 4V (MIN)
ILIM Resistance to GND, R_{ILIM} ..... 715Ω to 6650Ω
Continuous Switch Current (T_J ≤ 125℃), I_{MAX} ..... 7A (MAX)
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTES:

1. When using SGM2546Bx variant, ensure that the input voltage is restricted to the chosen output voltage clamp value specified in the electrical characteristics section.

2. When supply voltages are below 5V, connecting the EN/UVLO pin directly to IN is acceptable. For voltages exceeding 5V, it's advised to employ a pull-up resistor with a minimum value of 350kΩ.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

OVERSTRESS CAUTION

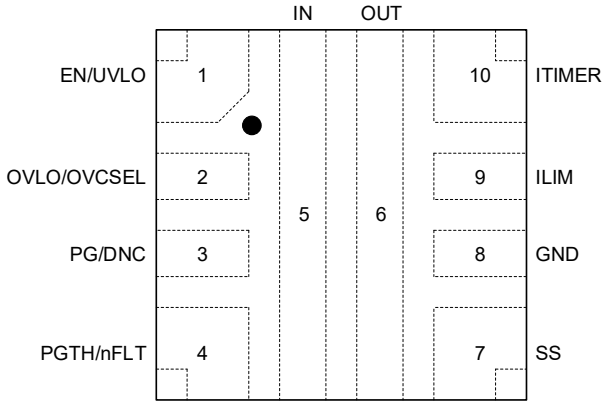
Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-2×2-10L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	EN/UVLO	AI	Enable and Under-Voltage Lockout Input. Asserting EN/UVLO pin high enables the device. As a UVLO pin, the UVLO threshold is programmed by an external resistor divider. This pin cannot be left floating.
2	OVLO	AI	(SGM2546Ax/Cx Only) Over-Voltage Lockout Pin. The over-voltage lockout threshold is programmed by the resistor divider from the power supply to the OVLO terminal to GND. The device is enabled when this pin is tied to low level. This pin cannot be left floating.
	OVCSEL	AI	(SGM2546Bx Only) Output Clamp Voltage Selection Pin.
3	PG	DO	(SGM2546Bx/Cx Only) Power Good Indication. This is an open-drain pin, when the internal FET is fully enhanced and the PGTH voltage is higher than the set value, the pin is set to high level.
	DNC	DO	(SGM2546Ax Only) No Connection. Do not connect this pin to anything.
4	nFLT	DO	(SGM2546Ax Only) Fault Event Indicator. The nFLT is an open-drain output, and when a fault occurs, it will be low.
	PGTH	AI	(SGM2546Bx/Cx Only) Power Good Threshold.
5	IN	P	Input Supply Voltage.
6	OUT	P	Output of the Device.
7	SS	AO	Soft-Start Pin. The capacitor between SS and GND pins will set the slew rate according to the application requirements. When this pin is left floating, the device will start up at the fastest rate.
8	GND	G	Ground.
9	ILIM	AO	Current Limit Programming Pin. Use this dual function pin for limiting and monitoring the output current. Connecting this pin to GND can set the output current limit. This pin can also be used to monitor the load current. Do not float this pin.
10	ITIMER	AO	Place a capacitor between this pin and GND can set the over-current blanking time, at this stage, the output current value can temporarily exceed the internally set current limit value (but not exceed the fast-trip threshold). After this time, the device will take action if it is still in over-current state. Leaving this pin open will provide the fastest response to an over-current event.

NOTE: AI = analog input, AO = analog output, DO = digital output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 12V, OUT pin floating, $V_{EN/UVLO}$ = 2V, V_{OVLO} = 0V for SGM2546Ax/Cx, OVCSEL = 390kΩ to GND for SGM2546Bx, R_{ILIM} = 715Ω, SS and ITIMER pins floating, nFLT pin floating for SGM2546Ax, PGTH and PG pins floating for SGM2546Bx/Cx, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply (IN)							
Supply Quiescent Current	I_{Q_ON}	SGM2546Ax/Cx			172	300	μA
		SGM2546Bx			184	320	
	$I_{Q_ON_OVC}$	SGM2546Bx			223	380	μA
IN Supply Off Current	I_{Q_OFF}	$V_{SD_F} < V_{EN} < V_{UVLO_F}$			56	120	μA
Supply Shutdown Current	I_{SD}	$V_{EN} < V_{SD_F}$			8	35	μA
Under-Voltage Protection Threshold	V_{UVP_R}	Rising		2.46	2.56	2.64	V
	V_{UVP_F}	Falling		2.23	2.33	2.43	V
Output Voltage Clamp (OUT) - SGM2546Bx							
Over-Voltage Clamp Threshold	V_{OVC}	OVCSEL = shorted to GND		3.65	3.91	4.1	V
		OVCSEL = open		5.25	5.81	6.2	
		OVCSEL = 390kΩ to GND		13.2	13.95	14.5	
Output Voltage during Clamping	V_{CLAMP}	I_{OUT} = 10mA	OVCSEL = shorted to GND	3.2	3.83	4.2	V
			OVCSEL = open	5	5.72	6.12	
			OVCSEL = 390kΩ to GND	13	13.83	14.6	
Output Load Current Monitor (ILIM)							
Analog Load Current Monitor Gain	G_{IMON}	I_{MON} : I_{OUT}, I_{OUT} = 1A to 7.7A, $I_{OUT} < I_{LIM}$		99	107.5	116	μA/A
Over-Current Protection (OUT)							
Over-Current Threshold	I_{LIM}	R_{ILIM} = 6.65kΩ		0.75	0.87	0.97	A
		R_{ILIM} = 3.32kΩ		1.55	1.73	1.91	
		R_{ILIM} = 1.65kΩ		3.20	3.48	3.74	
		R_{ILIM} = 750Ω		7.03	7.65	8.20	
Circuit-Breaker Threshold	I_{SPFLT}	SGM2546Ax/Bx, ILIM pin open				0.2	A
		ILIM pin shorted to GND			2	3.1	
Scalable Fast-Trip Threshold	I_{SCGain}	I_{SC} : I_{LIM} ratio		143	203	266	%
V_{OUT} Threshold to Exit Current Limit Foldback	V_{FB}	V_{OUT} threshold to exit current limit foldback		1.55	1.91	2.23	V
On-Resistance (IN - OUT)							
On-Resistance	R_{DSON}	2.7V ≤ V_{IN} ≤ 4V, I_{OUT} = 1A			10	18.3	mΩ
		4V < V_{IN} ≤ 23V, I_{OUT} = 1A			10	18.3	
Enable/Under-Voltage Lockout (EN/UVLO)							
EN/UVLO Rising Threshold	V_{UVLO_R}			1.183	1.2	1.228	V
EN/UVLO Falling Threshold	V_{UVLO_F}			1.076	1.1	1.125	V
EN/UVLO Falling Threshold for Lowest Shutdown Current	V_{SD_F}			0.45	0.73	1	V
EN/UVLO Pin Leakage Current	I_{ENLKG}			-0.15		0.15	μA
Over-Voltage Lockout (OVLO) - SGM2546Ax/Cx							
OVLO Rising Threshold	V_{OV_R}			1.183	1.2	1.228	V
OVLO Falling Threshold	V_{OV_F}			1.076	1.1	1.125	V
OVLO Pin Leakage Current	I_{OVLKG}	0.5V < V_{OV} < 1.5V		-0.1		0.1	μA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, V_{IN} = 12V, OUT pin floating, $V_{EN/UVLO}$ = 2V, V_{OVLO} = 0V for SGM2546Ax/Cx, OVCSEL = 390kΩ to GND for SGM2546Bx, R_{ILIM} = 715Ω, SS and ITIMER pins floating, nFLT pin floating for SGM2546Ax, PGTH and PG pins floating for SGM2546Bx/Cx, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Over-Current Fault Timer (ITIMER)						
ITIMER Internal Discharge Current	I_{ITIMER}	I_{OUT} > I_{LIM}	1.5	2	2.72	μA
ITIMER Internal Pull-Up Resistance	R_{ITIMER}			15.3	35	kΩ
ITIMER Internal Pull-Up Voltage	V_{INT}		2.1	2.58	2.74	V
ITIMER Comparator Threshold	V_{ITIMER_F}	I_{OUT} > I_{LIM}	0.609	1.05	1.37	V
ITIMER Discharge Differential Voltage Threshold	ΔV_{ITIMER}	I_{OUT} > I_{LIM}	1.286	1.53	1.741	V
Power Good Indication (PG) - SGM2546Bx/Cx						
PG Voltage while De-Asserted	V_{PGD}	V_{IN} < V_{UVP_F}, V_{EN} < V_{SD_F}, weak pull-up (I_{PG} = 26μA)		489	1000	mV
		V_{IN} < V_{UVP_F}, V_{EN} < V_{SD_F}, strong pull-up (I_{PG} = 242μA)		640	1000	
		V_{IN} > V_{UVP_R}, I_{PG} = 10mA		168	600	
PG Leakage Current	I_{PGLKG}	PG asserted			3	μA
Power Good Threshold (PGTH)						
PGTH Rising Threshold	V_{PGTH_R}		1.178	1.2	1.23	V
PGTH Falling Threshold	V_{PGTH_F}		1.071	1.1	1.13	V
PGTH Pin Leakage Current	$I_{PGTHLKG}$		-1		1	μA
Fault Indication (nFLT) - SGM2546Ax						
nFLT Leakage Current	$I_{FAULTLKG}$		-1		1	μA
nFLT Internal Pull-Down Resistance	R_{nFLT}			12.4		Ω
Over-Temperature Protection (OTP)						
Thermal Shutdown Rising Threshold	T_{SD}	T_J rising		154		℃
Thermal Shutdown Hysteresis	T_{HYS}	T_J falling		10		℃
SS						
SS Pin Charging Current	I_{SS}		1.4	3.4	5.7	μA

TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Over-Voltage Lockout Response Time	t_{OVLO}	SGM2546Ax/Cx, $V_{OV} > V_{OV_R}$ to V_{OUT}↓		1.2		μs
Over-Voltage Clamp Response Time	t_{OVC}	SGM2546Bx, $V_{IN} > V_{OVC}$ to V_{OUT}↓		3		μs
Current Limit Response Time	t_{LIM}	SGM2545Ax/Bx, $I_{OUT} > I_{LIM}$ + 30% to I_{OUT} settling within 5% of I_{LIM}		600		μs
Short-Circuit Response Time	t_{SC}	$I_{OUT} > 3 \times I_{LIM}$ to output current cut off		550		ns
Fixed Fast-Trip Response Time	t_{FT}	$I_{OUT} > I_{FT}$ to I_{OUT}↓		550		ns
Thermal Shutdown Auto-Retry Interval	t_{TSD_RST}	Device enabled and $T_J < T_{SD} - T_{HYS}$		127		ms
PG Assertion De-Glitch Time	t_{PGA}	$V_{PGTH} > V_{PGTH_R}$ to PG↑		14		μs
PG De-Assertion De-Glitch Time	t_{PGD}	$V_{PGTH} < V_{PGTH_F}$ to PG↓		14		μs

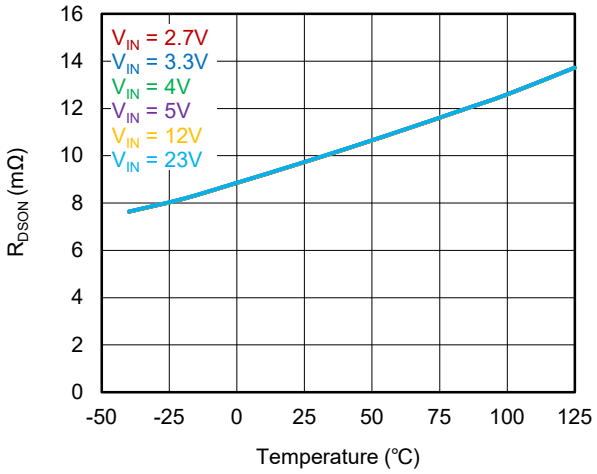
SWITCHING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	C_{SS} = OPEN	C_{SS} = 1800pF	C_{SS} = 3300pF	UNITS
Output Rising Slew Rate	SR_{ON}	V_{IN} = 2.7V	10.85	1.680	1.02	V/ms
		V_{IN} = 12V	23.54	1.694	0.973	
		V_{IN} = 23V	36.88	1.693	0.953	
Turn-On Delay	t_{D_ON}	V_{IN} = 2.7V	0.212	0.506	0.808	ms
		V_{IN} = 12V	0.272	1.161	2.183	
		V_{IN} = 23V	0.27	1.779	2.980	
Rise Time	t_R	V_{IN} = 2.7V	0.194	1.405	2.172	ms
		V_{IN} = 12V	0.268	5.356	9.33	
		V_{IN} = 23V	0.305	10.451	18.78	
Turn-On Time	t_{ON}	V_{IN} = 2.7V	0.406	1.911	2.98	ms
		V_{IN} = 12V	0.540	6.517	11.517	
		V_{IN} = 23V	0.575	12.23	21.761	
Turn-Off Delay	t_{D_OFF}	V_{IN} = 2.7V	19.4	18.8	17.4	μs
		V_{IN} = 12V	8.4	8.4	8.6	
		V_{IN} = 23V	5.0	4.7	5.0	

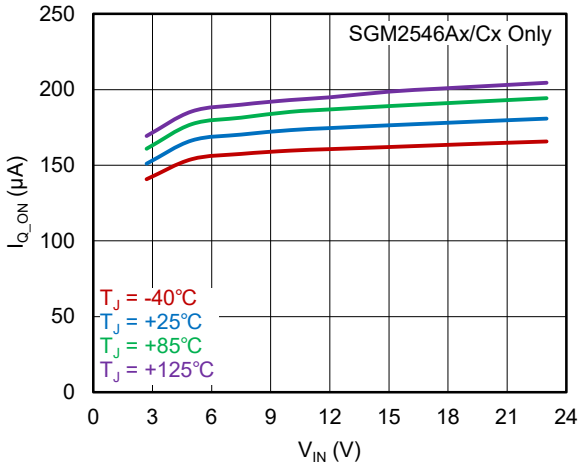
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = -40℃ to +125℃, unless otherwise noted.

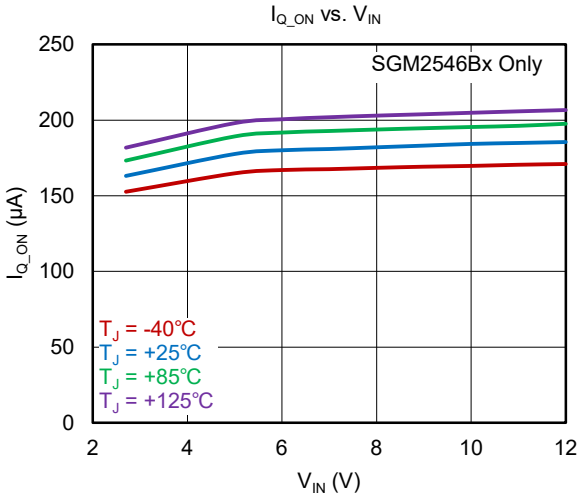
R_{DSON} vs. Temperature



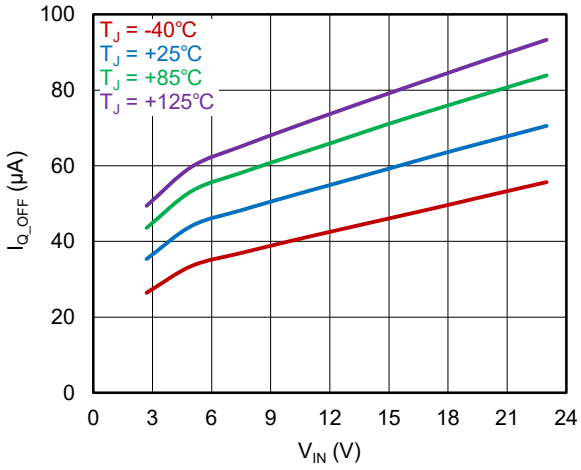
I_{Q_ON} vs. V_{IN}



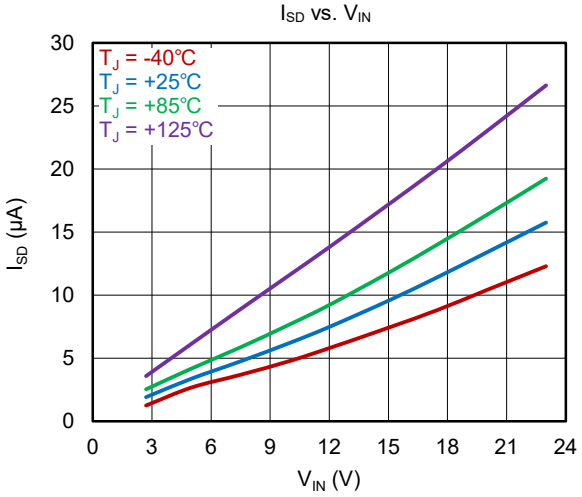
I_{Q_ON} vs. V_{IN}



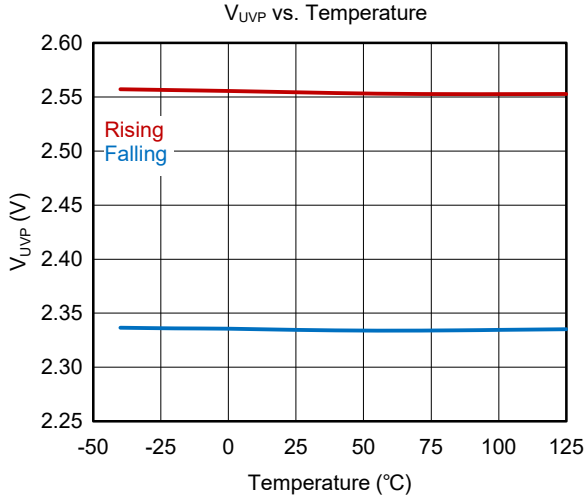
I_{Q_OFF} vs. V_{IN}



I_{SD} vs. V_{IN}



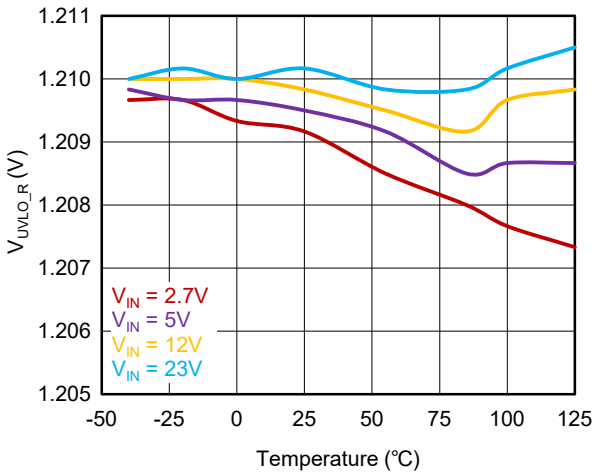
V_{UVP} vs. Temperature



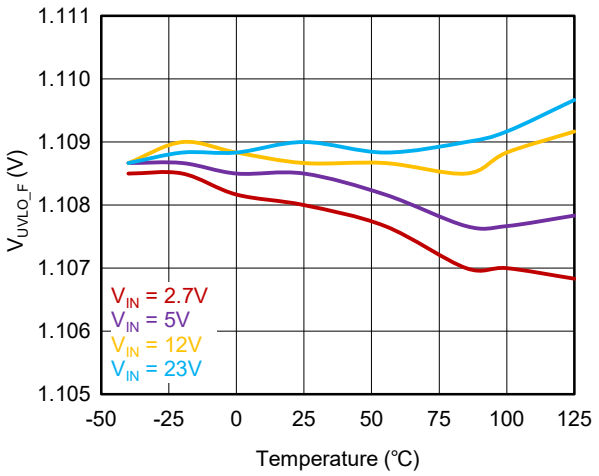
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = -40℃ to +125℃, unless otherwise noted.

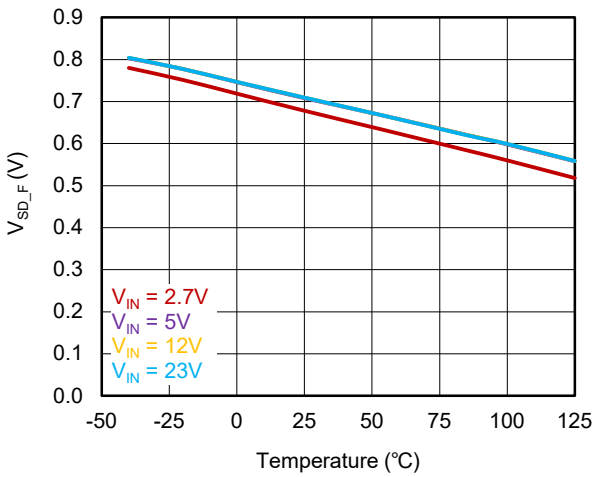
V_{UVLO_R} vs. Temperature



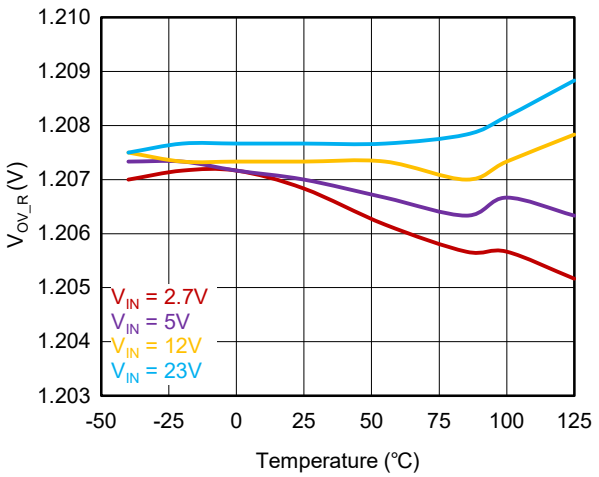
V_{UVLO_F} vs. Temperature



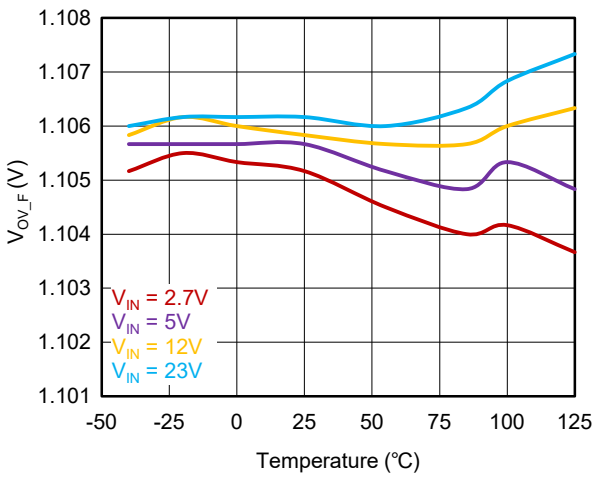
V_{SD_F} vs. Temperature



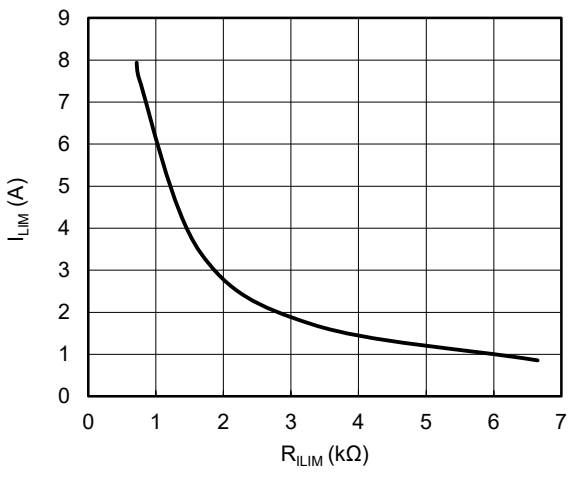
V_{OV_R} vs. Temperature



V_{OV_F} vs. Temperature



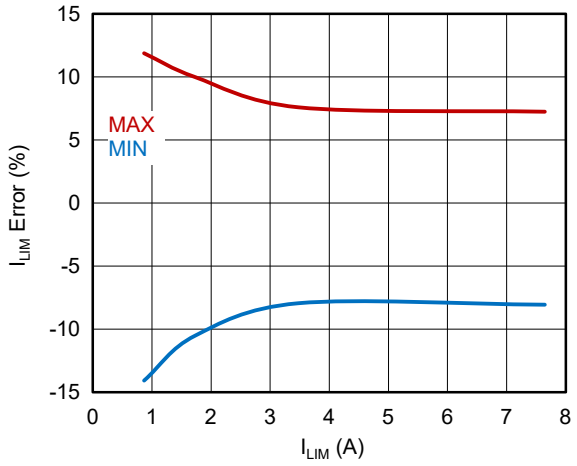
I_{LIM} vs. R_{ILIM}



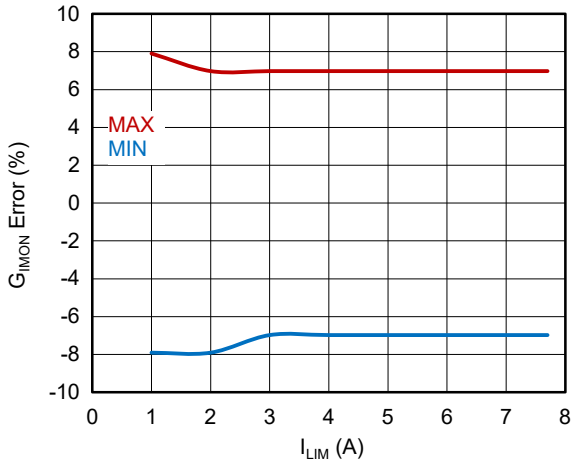
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = -40℃ to +125℃, unless otherwise noted.

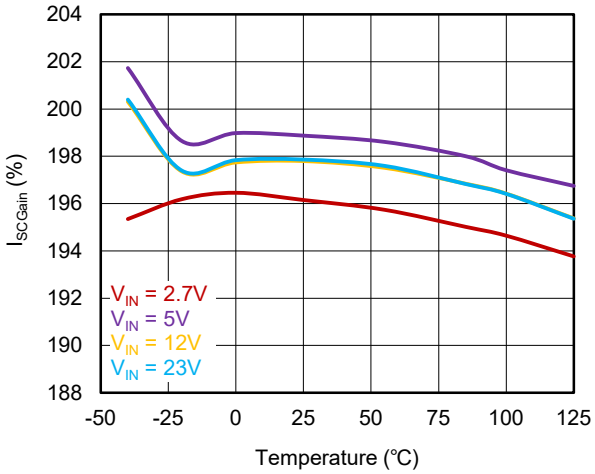
I_{LIM} Error vs. I_{LIM}



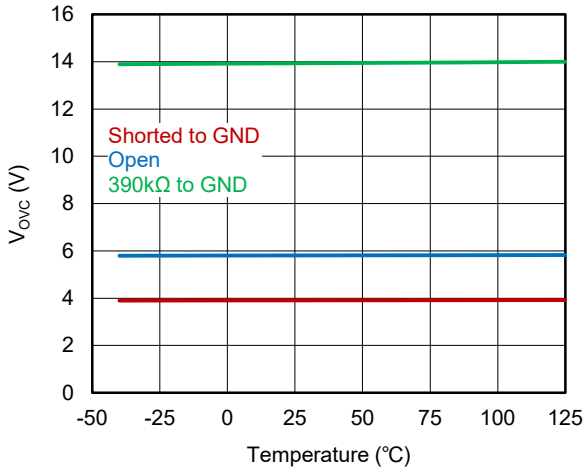
G_{IMON} Error vs. I_{OUT}



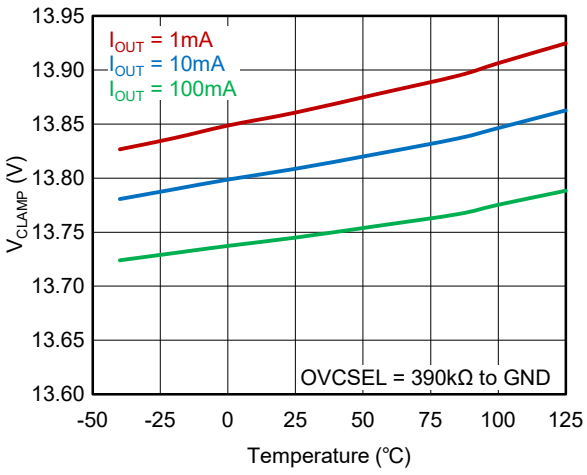
I_{SCGain} vs. Temperature



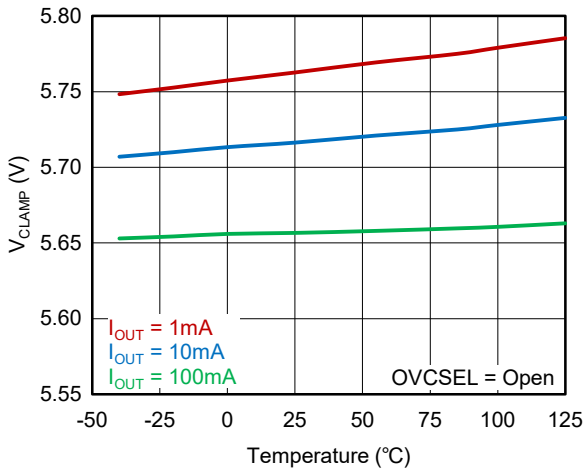
V_{OVC} vs. Temperature



V_{CLAMP} vs. Temperature



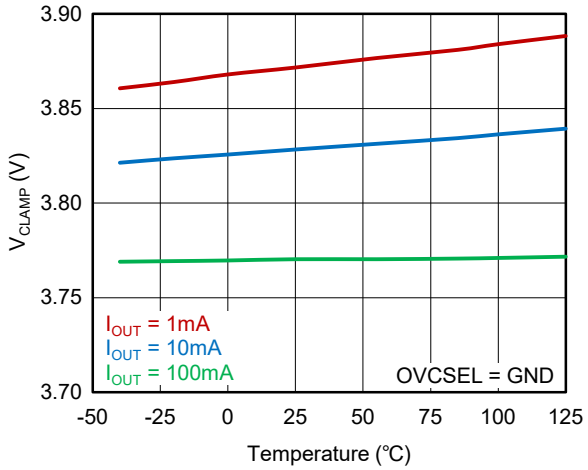
V_{CLAMP} vs. Temperature



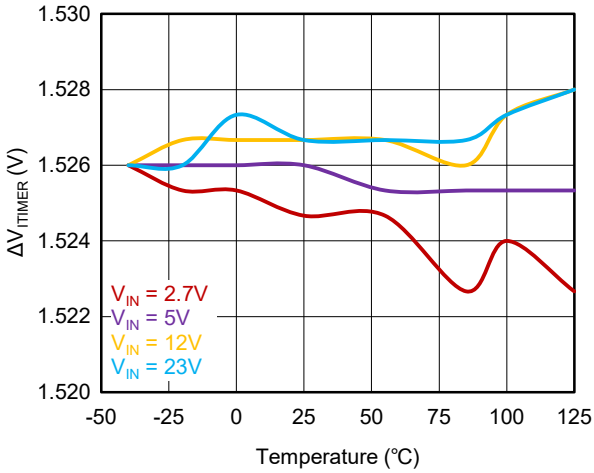
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = -40℃ to +125℃, unless otherwise noted.

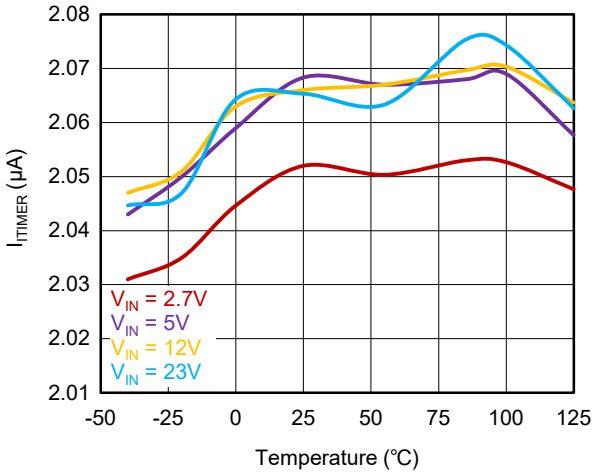
V_{CLAMP} vs. Temperature



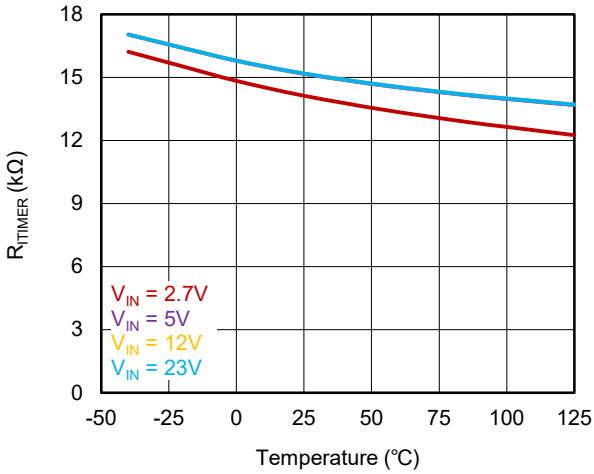
ΔV_{ITIMER} vs. Temperature



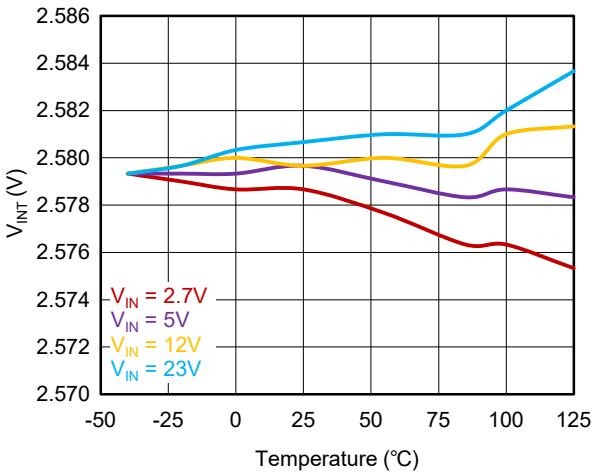
I_{ITIMER} vs. Temperature



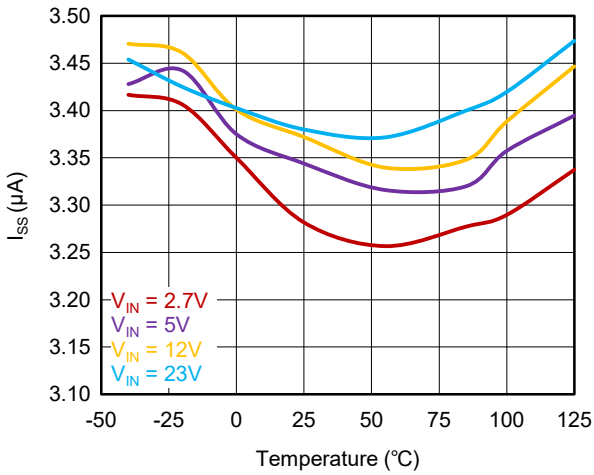
R_{ITIMER} vs. Temperature



V_{INT} vs. Temperature



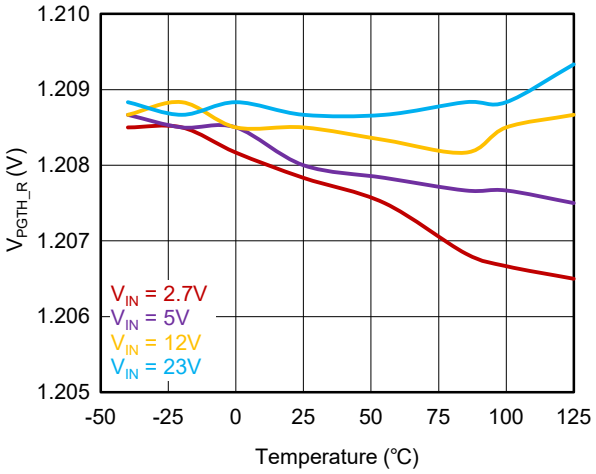
I_{SS} vs. Temperature



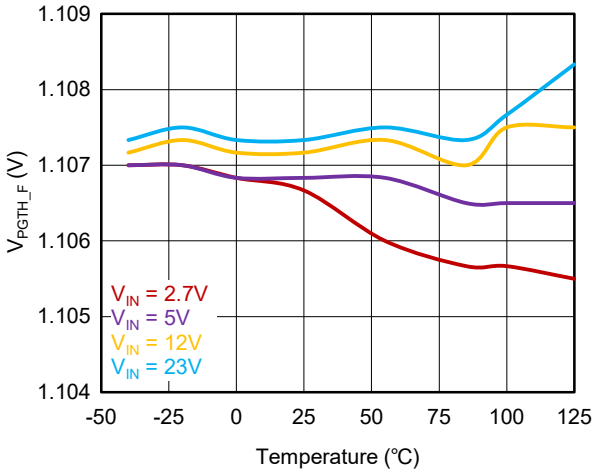
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = -40℃ to +125℃, unless otherwise noted.

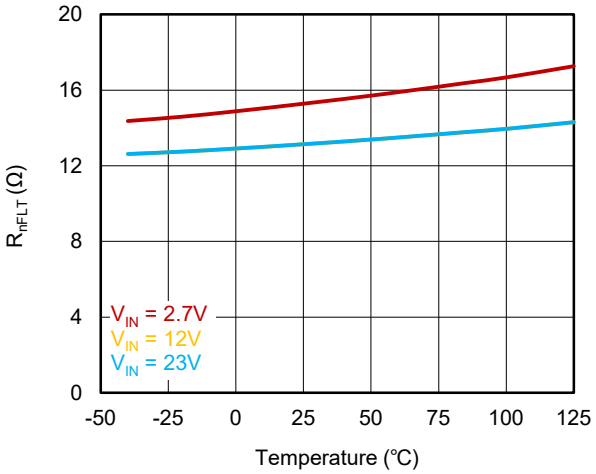
V_{PGTH_R} vs. Temperature



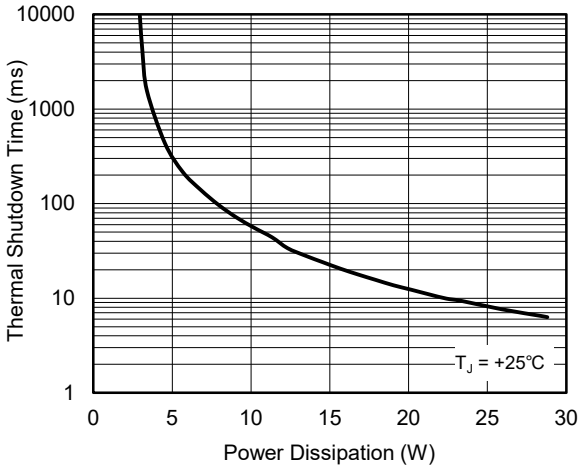
V_{PGTH_F} vs. Temperature



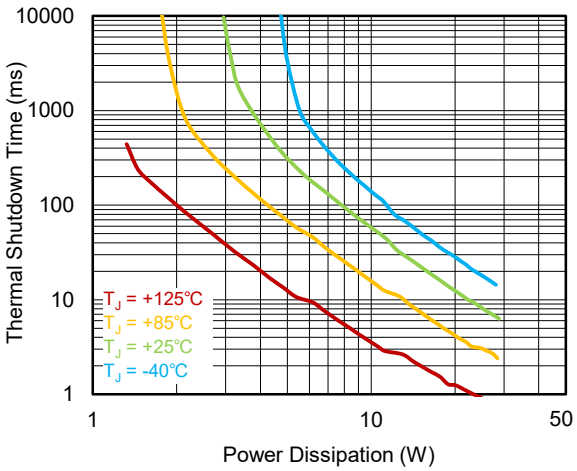
R_{nFLT} vs. Temperature



Thermal Shutdown Time vs. Power Dissipation



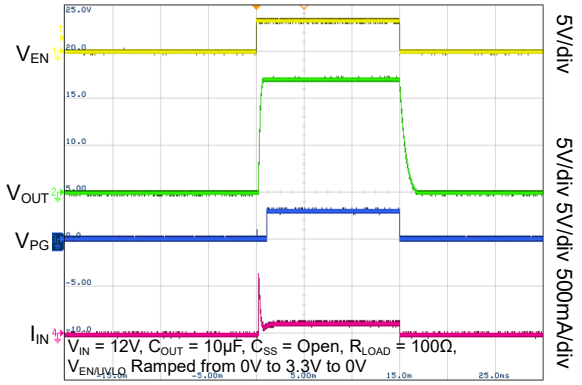
Thermal Shutdown Time vs. Power Dissipation



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

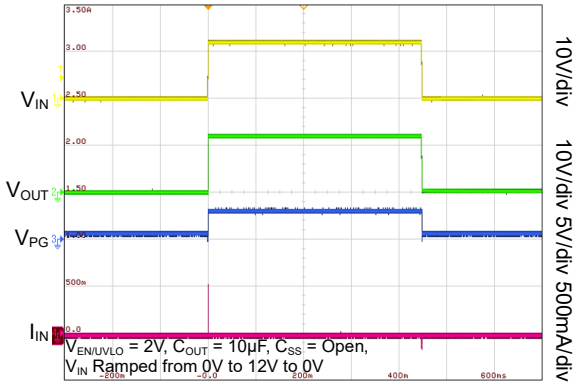
T_J = +25℃, unless otherwise noted.

Power-Up and Power-Down with EN/UVLO Control



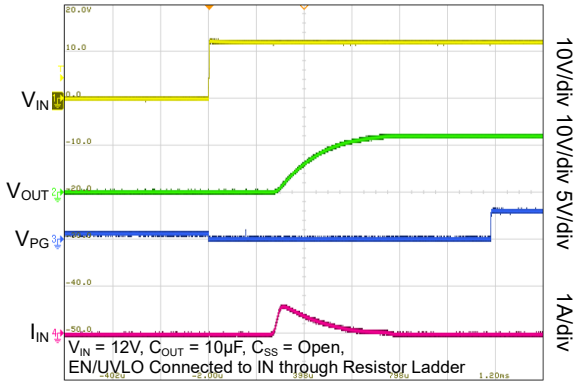
Time (5ms/div)

Power-Up and Power-Down with Input Supply



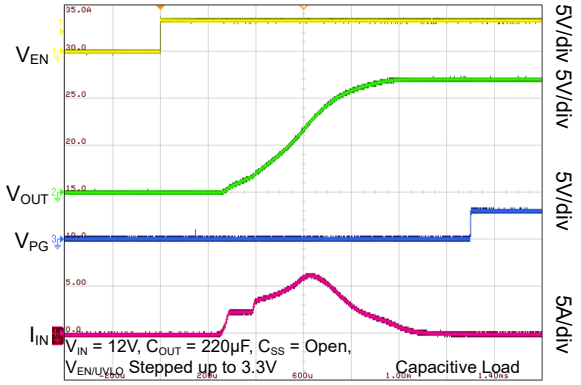
Time (100ms/div)

Input Hot-Plug



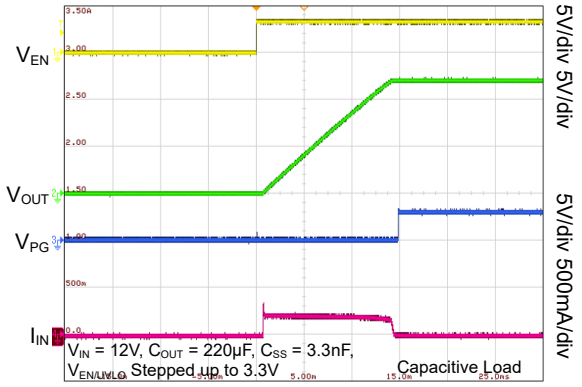
Time (200μs/div)

Inrush Current without Slew Rate Control



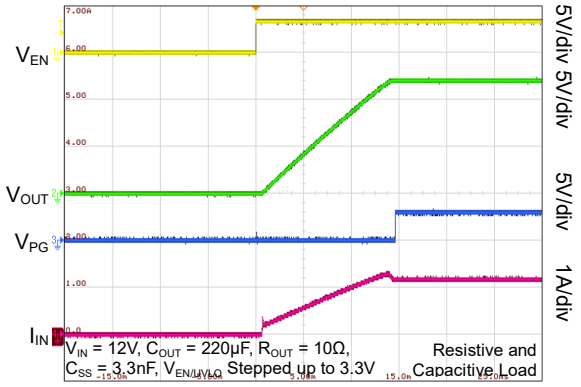
Time (200μs/div)

Inrush Current with Slew Rate Control



Time (5ms/div)

Inrush Current with Slew Rate Control

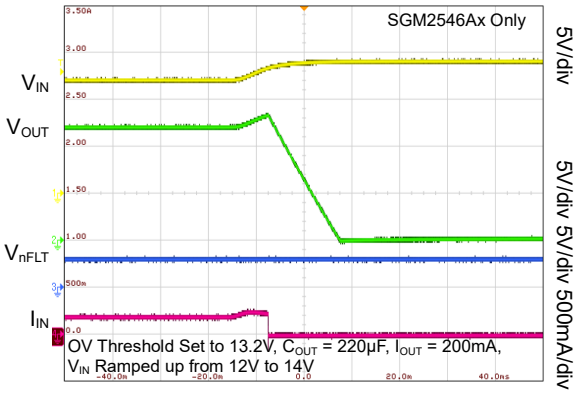


Time (5ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

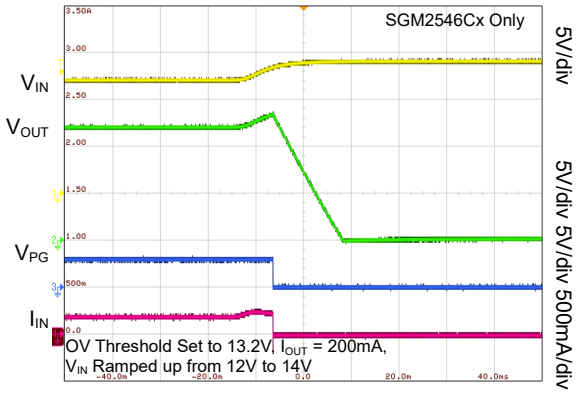
T_J = +25℃, unless otherwise noted.

Over-Voltage Lockout Response



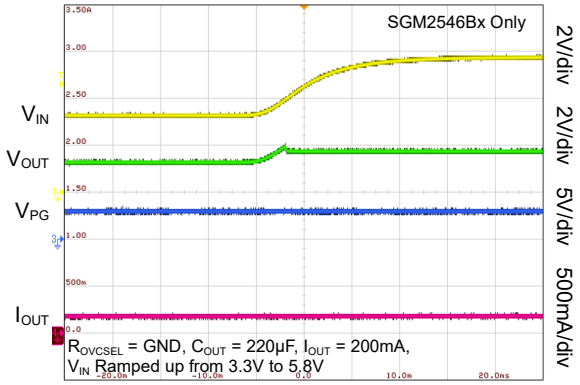
Time (10ms/div)

Over-Voltage Lockout Response



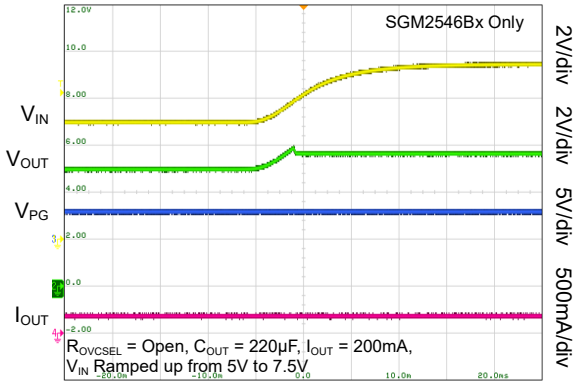
Time (10ms/div)

Over-Voltage Clamp Response



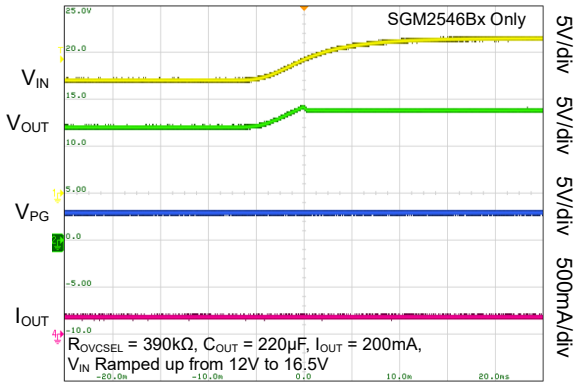
Time (5ms/div)

Over-Voltage Clamp Response



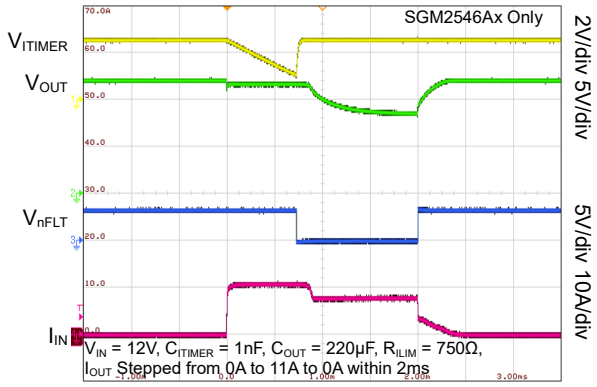
Time (5ms/div)

Over-Voltage Clamp Response



Time (5ms/div)

Active Current Limit Response

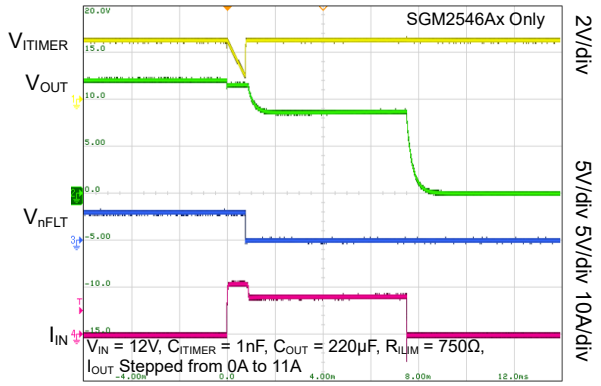


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

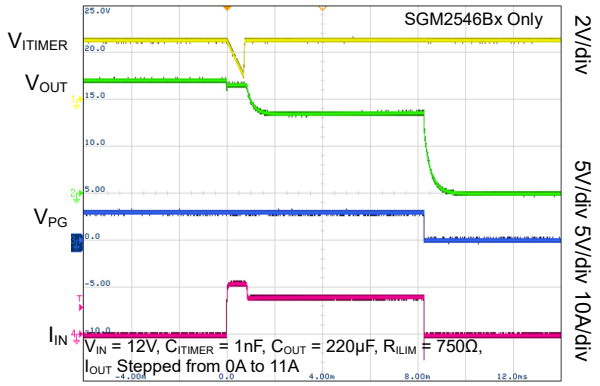
T_J = +25℃, unless otherwise noted.

Active Current Limit Response Followed by TSD



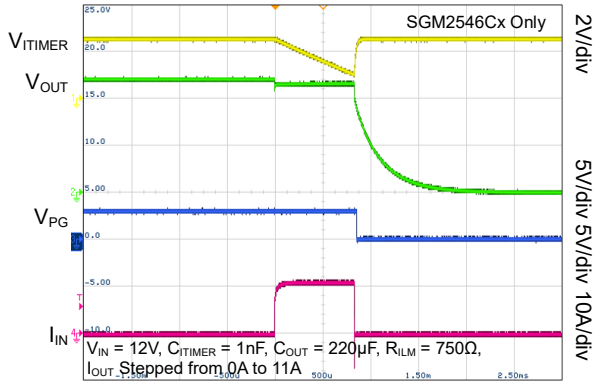
Time (2ms/div)

Active Current Limit Response Followed by TSD



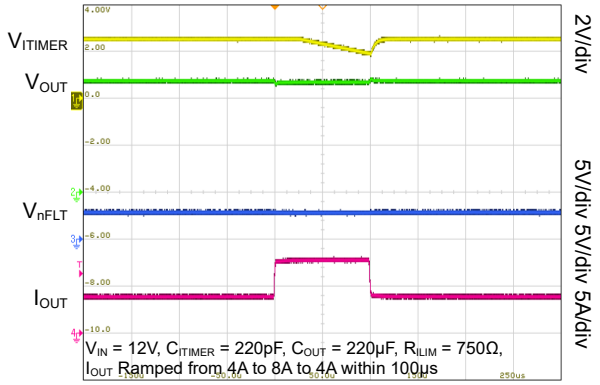
Time (2ms/div)

Circuit Breaker Response



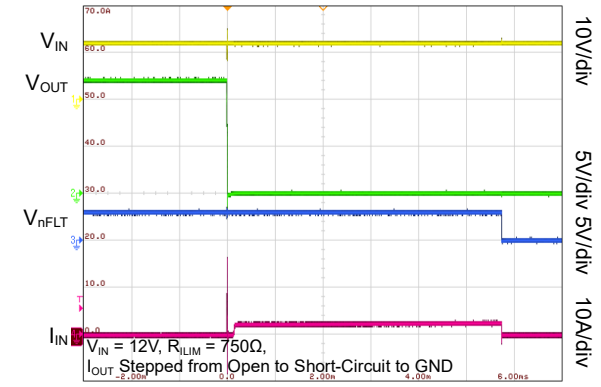
Time (500μs/div)

Transient Over-Current Blanking Timer Response



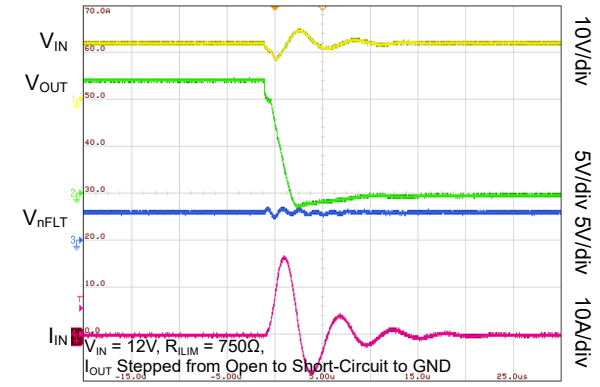
Time (50μs/div)

Output Short-Circuit During Steady State



Time (1ms/div)

Output Short-Circuit During Steady State (Zoomed In)

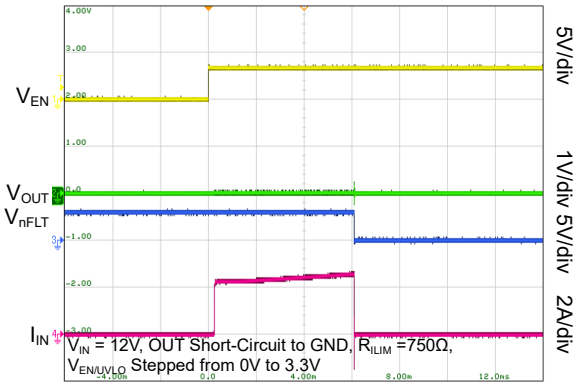


Time (5μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.

Power-Up into Short-Circuit



FUNCTIONAL BLOCK DIAGRAM

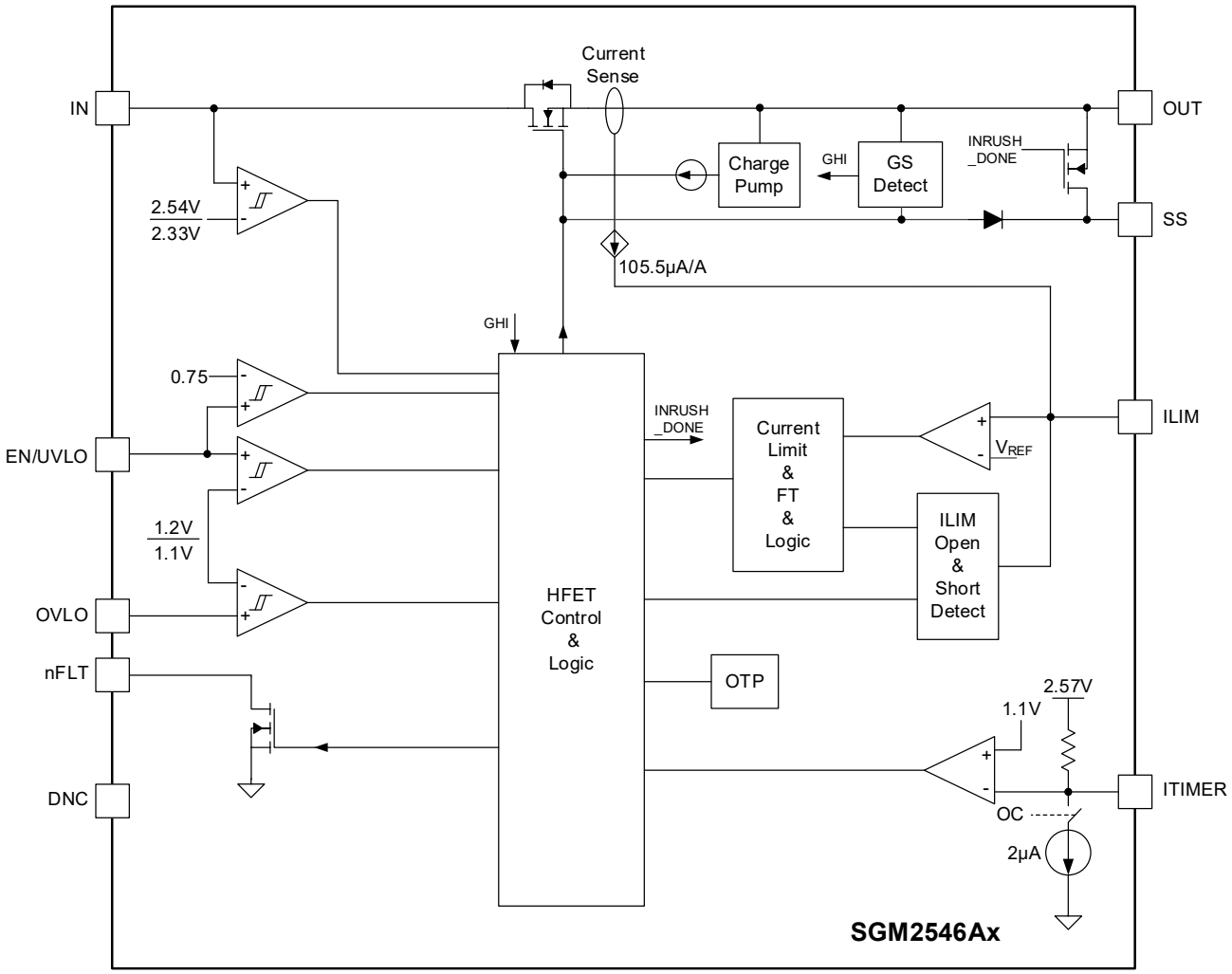


Figure 1. SGM2546Ax Block Diagram

FUNCTIONAL BLOCK DIAGRAM (continued)

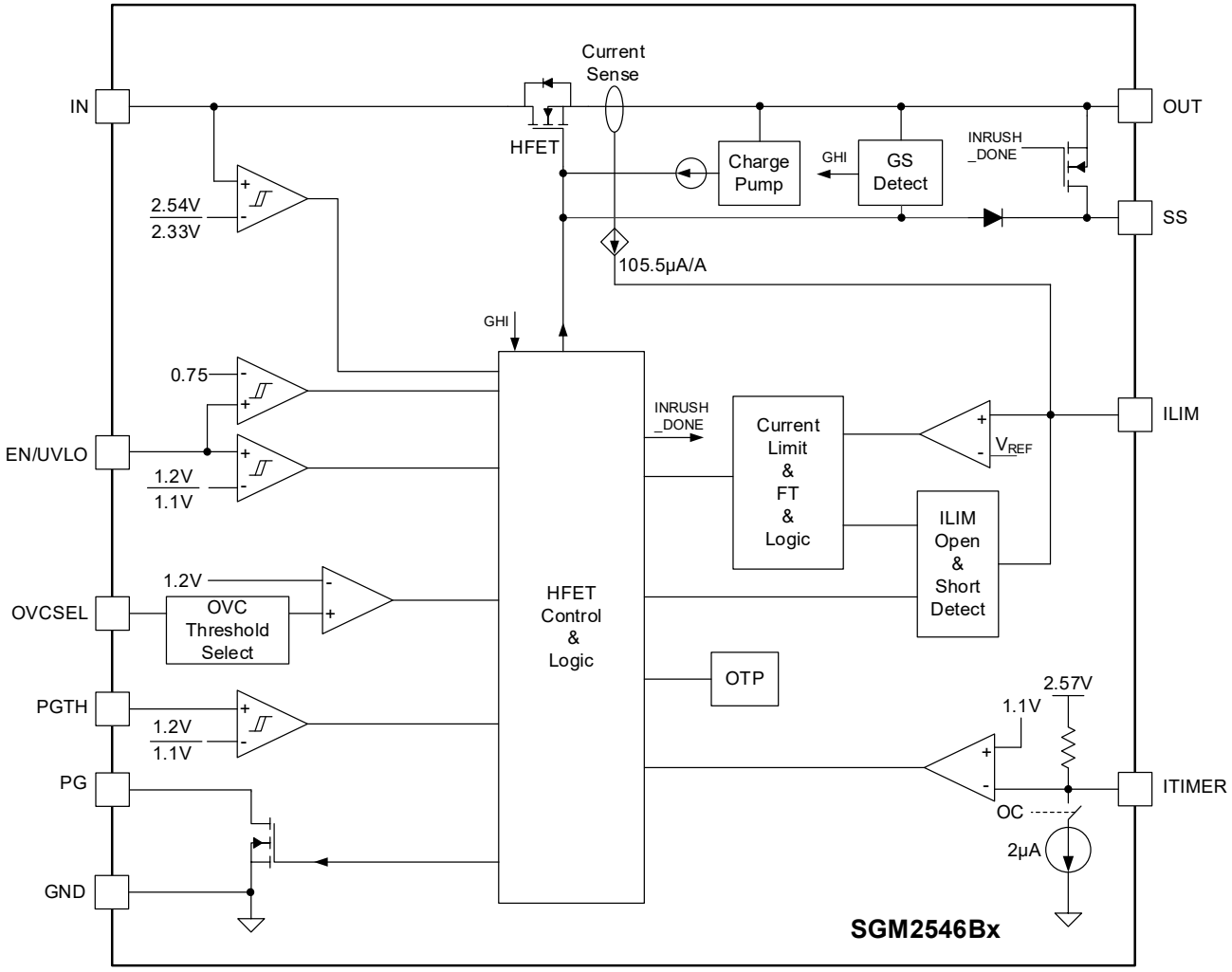


Figure 2. SGM2546Bx Block Diagram

FUNCTIONAL BLOCK DIAGRAM (continued)

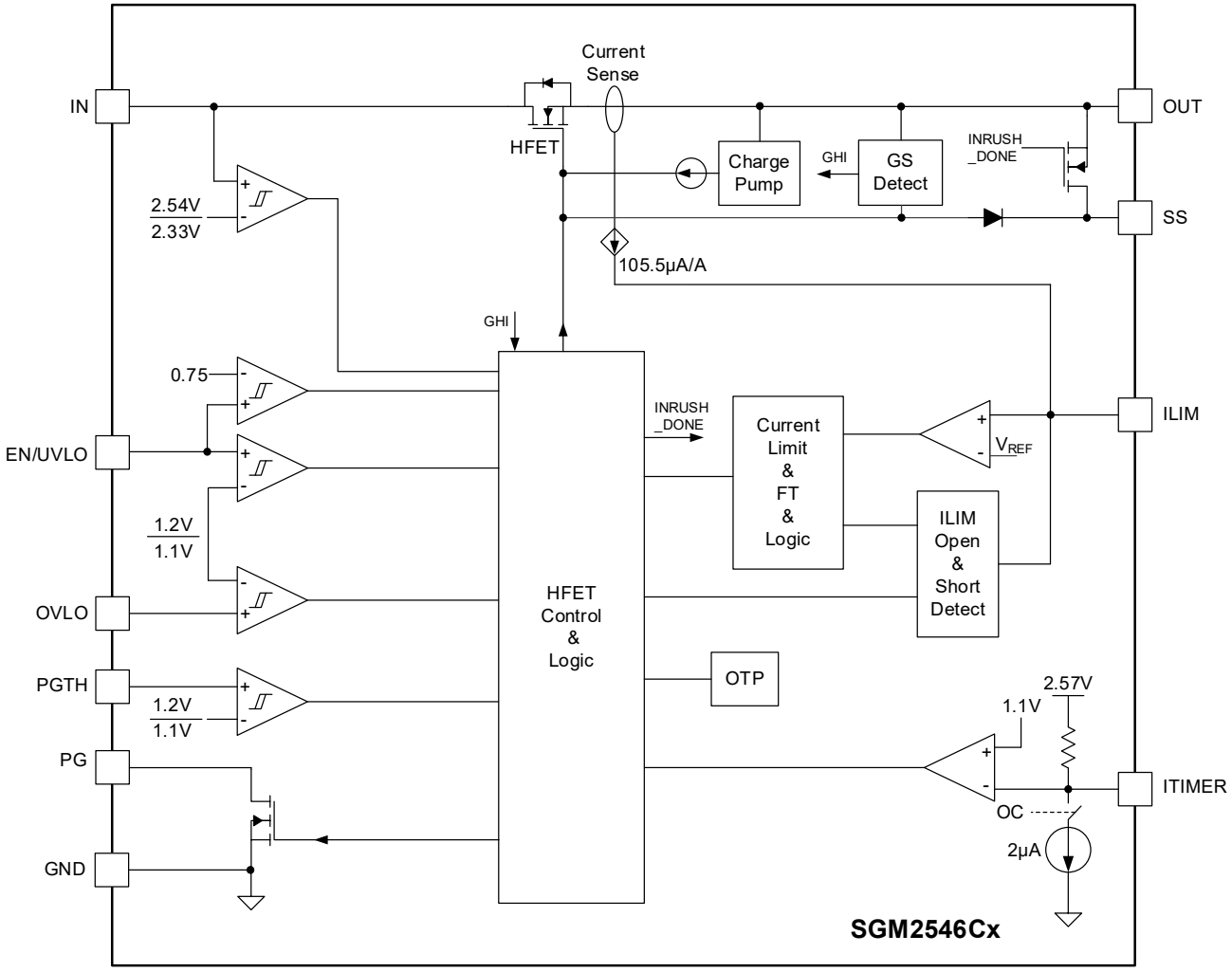


Figure 3. SGM2546Cx Block Diagram

DETAILED DESCRIPTION

SGM2546 is an eFuse with internal integration of FET. It ensures the safety of the power delivery system due to its rich features. When the V_{IN} is greater than V_{UVP_R}, the device starts to sample the voltage of the EN/UVLO pin ($V_{EN/UVLO}$). If $V_{EN/UVLO}$ exceeds V_{UVLO_R}, the internal FET starts conducting and the current can flow from IN to OUT. When the V_{IN} is less than V_{UVP_F} or $V_{EN/UVLO}$ < V_{UVLO_F}, the internal FET is turned off.

After device start-up, the SGM2546 will monitor the V_{IN} and forward current (from IN to OUT). By controlling the internal FET, the load current is limited to the set current limit threshold (I_{LIM}). During over-voltage event, the output voltage will be clamped to the chosen threshold (V_{OVC}) or be cut-off if it exceeds the user-adjustable over-voltage lockout threshold (V_{OV}). The fast-trip response of the device can provide rapid protection against serious over-current during short-circuit of OUT pin, so as to prevent the system from being damaged by harmful voltage and current. In addition, the device also provides a user-adjustable over-current blanking timer to allow short-time over-current in the power path without tripping the device frequently. Therefore, SGM2546 not only provides complete protection functions, but also ensures the maximum system uptime during transient events.

There is an integrated thermal sensor to protect itself when the device temperature exceeds the T_{SD}.

Under-Voltage Lockout (UVLO and UVP)

The SGM2546 implements under-voltage protection at IN pin to prevent IN voltage from being too low for normal operation of system and equipment. A fixed locking threshold voltage (V_{UVP}) is provided inside the device for under-voltage protection. In addition, the comparator on the EN/UVLO terminal can be used to set the user-adjustable under-voltage protection threshold through the external resistor divider. Figure 4 and Equation 1 show how to set the specific value of under-voltage protection threshold using an external resistor divider.

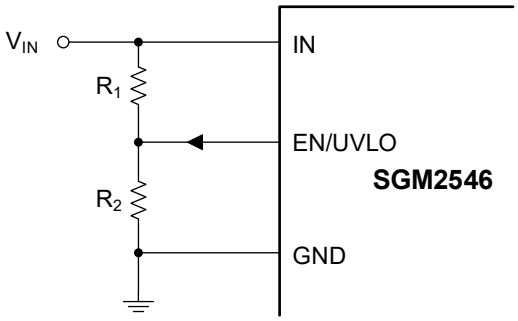


Figure 4. Adjustable Under-Voltage Protection

$$V_{IN_UV} = \frac{V_{UVLO} \times (R_1 + R_2)}{R_2} \quad (1)$$

Over-Voltage Lockout (OVLO)

The SGM2546Ax and SGM2546Cx implement over-voltage lockout at OVLO pin to prevent IN voltage from being too high for normal operation of system and equipment. The comparator on the OVLO pin is used to set the user-adjustable over-voltage protection threshold through the external resistor divider. If the voltage of OVLO pin exceeds the V_{OV_R}, the device will shut down the power path. When the voltage of OVLO pin is lower than the V_{OV_F}, the power path will be reopened with inrush control. There is a hysteresis between the rising threshold and falling threshold of OVLO. The Equation 2 and Figure 5 show how to set the specific value of over-voltage protection threshold using an external resistor divider.

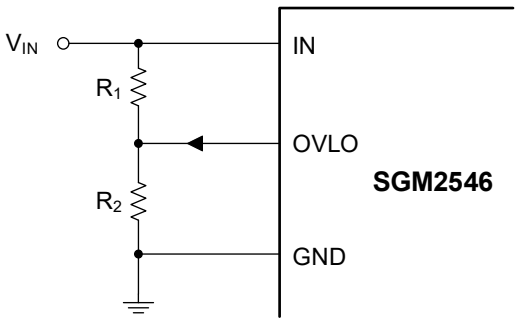


Figure 5. Adjustable Over-Voltage Protection

$$V_{IN_OV} = \frac{V_{OV} \times (R_1 + R_2)}{R_2} \quad (2)$$

DETAILED DESCRIPTION (continued)

While recovering from an OVLO event, the SGM2546Ax variant starts up with inrush control (SS).

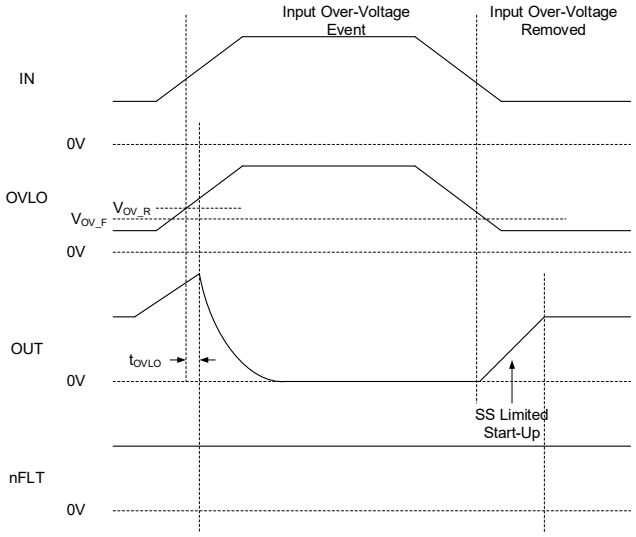


Figure 6. SGM2546Ax Over-Voltage Lockout and Recovery

While recovering from an OVLO event, the SGM2546Cx variants start up with inrush control (SS).

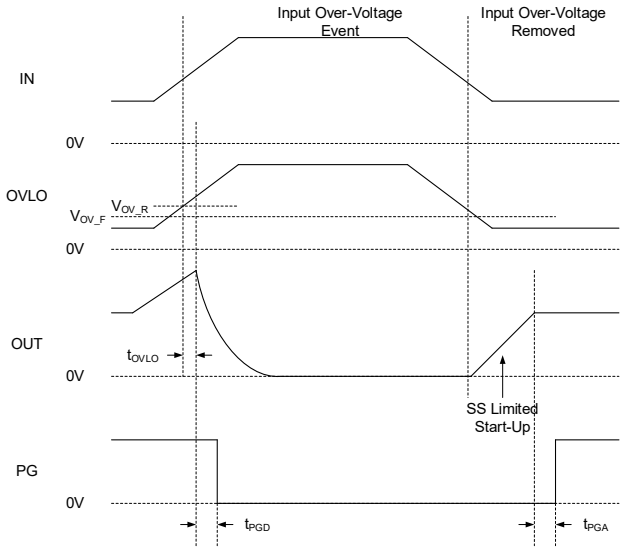


Figure 7. SGM2546Cx Over-Voltage Lockout and Recovery

Over-Voltage Clamp (OVC)

The SGM2546BR performs an output voltage clamp under input over-voltage event. When the input voltage exceeds the over-voltage clamp threshold (V_{OVC}), the device acts quickly within t_{OVC} and clamps the output voltage. The device will be regulated as long as the input over-voltage event is present.

If the device stays in clamp state driving certain load for a long time, considerable power will be dissipated on the device, which could cause over-temperature and thermal shutdown (TSD). After thermal shutdown, the SGM2546BL would stay latched off while the SGM2546BR would re-start after a delay time of T_{TSD} when the junction temperature falls below T_{SD} - T_{HYS}.

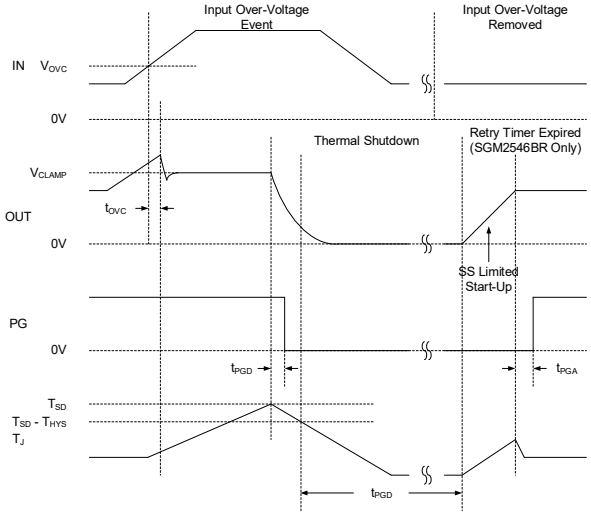


Figure 8. SGM2546Bx Over-Voltage Response (Auto-Retry)

The SGM2546Bx provides three available over-voltage clamp threshold values, which can be configured using the OVCSEL pin.

Table 1. SGM2546Bx Over-Voltage Clamp Threshold Selection

OVCSEL Pin Connection	Over-Voltage Clamp Threshold
Shorted to GND	3.91V
Open	5.81V
Connected to GND through a 390kΩ resistor	13.95V

Inrush Current, Over-Current, and Short-Circuit Protection

SGM2546 adopts four levels of forward over-current protection function:

- Programmable slew rate (SR) for inrush current protection.
- Programmable current limit threshold (I_{LIM}) for over-current in steady state or start-up.
- Programmable threshold (I_{SC}) for severe over-current in steady state or start-up.
- Fixed I_{FT} for fast-trip function when short-circuit of OUT occurs.

DETAILED DESCRIPTION (continued)

Slew Rate (SS) and Inrush Current Control

When hot-plug or system charging large capacitive load occurs, a large inrush current is generated in the equipment power path. The input connector may be damaged or the input power rail voltage may drop, which affects the normal operation and even restarts other equipment in the system.

For a given C_{OUT}, the relationship between the slew rate (SR) and inrush current (I_{INRUSH}) is shown in Equation 3.

$$SR(V/ms) = \frac{I_{INRUSH}(mA)}{C_{OUT}(\mu F)} \quad (3)$$

The slew rate can be controlled by connecting a capacitor at the SS pin to reduce inrush current. For a given slew rate, the corresponding C_{SS} can be calculated by Equation 4. When the SS pin is left floating, the fastest output slew rate can be obtained.

$$C_{SS}(pF) = \frac{3300}{SR(V/ms)} \quad (4)$$

Circuit-Breaker

The SGM2546Cx implement an over-current circuit-breaker response under over-current condition. The device turns off the internal FET after the user-programmable over-current blanking time. When the load current exceeds the over-current threshold I_{LIM} (set by the resistor at ILIM pin) but lower than the fast-trip threshold ($2 \times I_{LIM}$), the capacitor at ITIMER pin C_{ITIMER} starts discharging through the internal 2μA current. If the load current fall below I_{LIM} before the C_{ITIMER} discharges by ΔV_{ITIMER}, the ITIMER pin is reset by re-charging C_{ITIMER} to the internal pull up voltage V_{INT}, and the circuit-breaker will not be activated. If the over-current event persists, once C_{ITIMER} discharges by ΔV_{ITIMER}, the circuit breaker protection acts and turns off the internal FET. Meanwhile, C_{ITIMER} is re-charged to V_{INT} for the next over-current condition. This design ensures full blanking time is provided for every over-current fault.

Use Equation 5 to calculate the R_{ILM} value for an over-current threshold.

$$R_{ILM}(\Omega) = \frac{5747}{I_{LIM}(A)} \quad (5)$$

NOTES:

1. Leave the ILIM pin floating to set the over-current threshold near zero, and the device can hardly be loaded.

2. When the ILIM is short to the GND under normal operations, it will be detected as a fault case. There is a minimum I_{nFLT} which the device allows in this case before the pin short condition is detected.

The blanking time can be adjusted by changing the capacitance connected to the ITIMER pin. Over-current blanking time can be calculated by Equation 6.

$$t_{ITIMER}(ms) = \frac{\Delta V_{ITIMER}(V) \times C_{ITIMER}(nF)}{I_{ITIMER}(\mu A)} \quad (6)$$

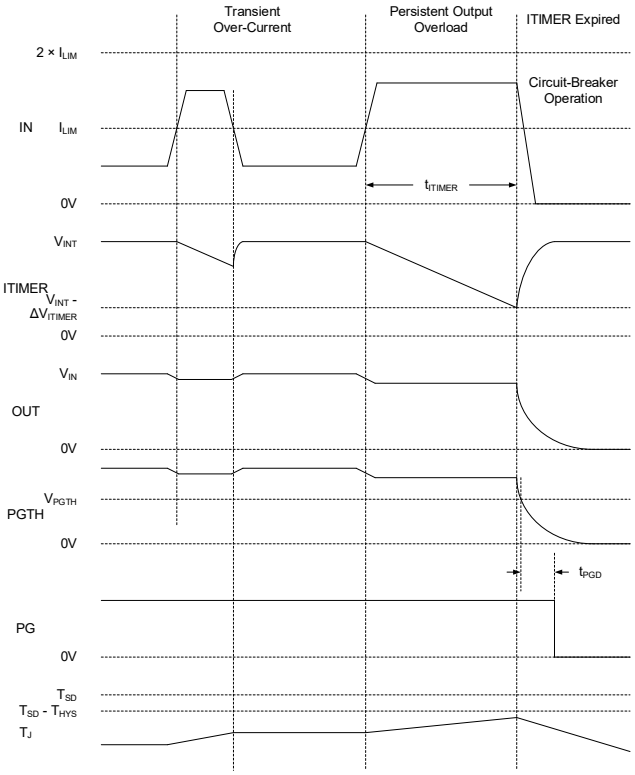


Figure 9. SGM2546Cx Over-Current Response

DETAILED DESCRIPTION (continued)

NOTES:

1. Leaving the ITIMER pin open would make the device to cut off the circuit with the minimum possible delay.

2. Leaving the ITIMER pin floating or short to GND sets the minimum over-current blanking time. But it is not recommended to leave ITIMER pin short to GND, because it increases the current consumption of the device.

3. Increasing C_{ITIMER} can increase the over-current blanking time, but it also increases the time for C_{ITIMER} to charge to V_{INT}. If the next over-current case occurs before the C_{ITIMER} is fully charged to the V_{INT}, the current blanking time of this event will be shorter than intended.

After the device shuts down due to over-current circuit breaker, the SGM2546CL remains latched off while the SGM2546CR would re-start after a fixed delay time.

Active Current Limiting

The SGM2546Ax and SGM2546Bx implement an over-current limiting response under over-current condition. The device actively regulates the current at the current-limit threshold (I_{LIM}) after the user-programmable over-current blanking time. When the load current exceeds the over-current threshold I_{LIM} (set by the resistor at ILIM pin) but lower than the fast-trip threshold ($2 \times I_{LIM}$), the capacitor at ITIMER pin C_{ITIMER} starts discharging through the internal 2μA current. If the load current falls below I_{LIM} before the C_{ITIMER} discharges by ΔV_{ITIMER}, the ITIMER pin is reset by re-charging C_{ITIMER} to the internal pull-up voltage V_{INT}, and the current limit will not be activated. If the over-current event persists, once C_{ITIMER} discharges by ΔV_{ITIMER}, the device actively limits the current at I_{LIM}. Meanwhile, C_{ITIMER} is re-charged to V_{INT} for the next over-current condition. This design ensures full blanking time is provided for every over-current fault. Use Equation 7 to calculate the R_{ILM} value for a desired over-current threshold.

$$R_{ILIM}(\Omega) = \frac{5747}{I_{LIM}(A)} \quad (7)$$

NOTES:

1. Leave the ILIM pin floating to set the over-current threshold near zero, and the device can hardly be loaded.

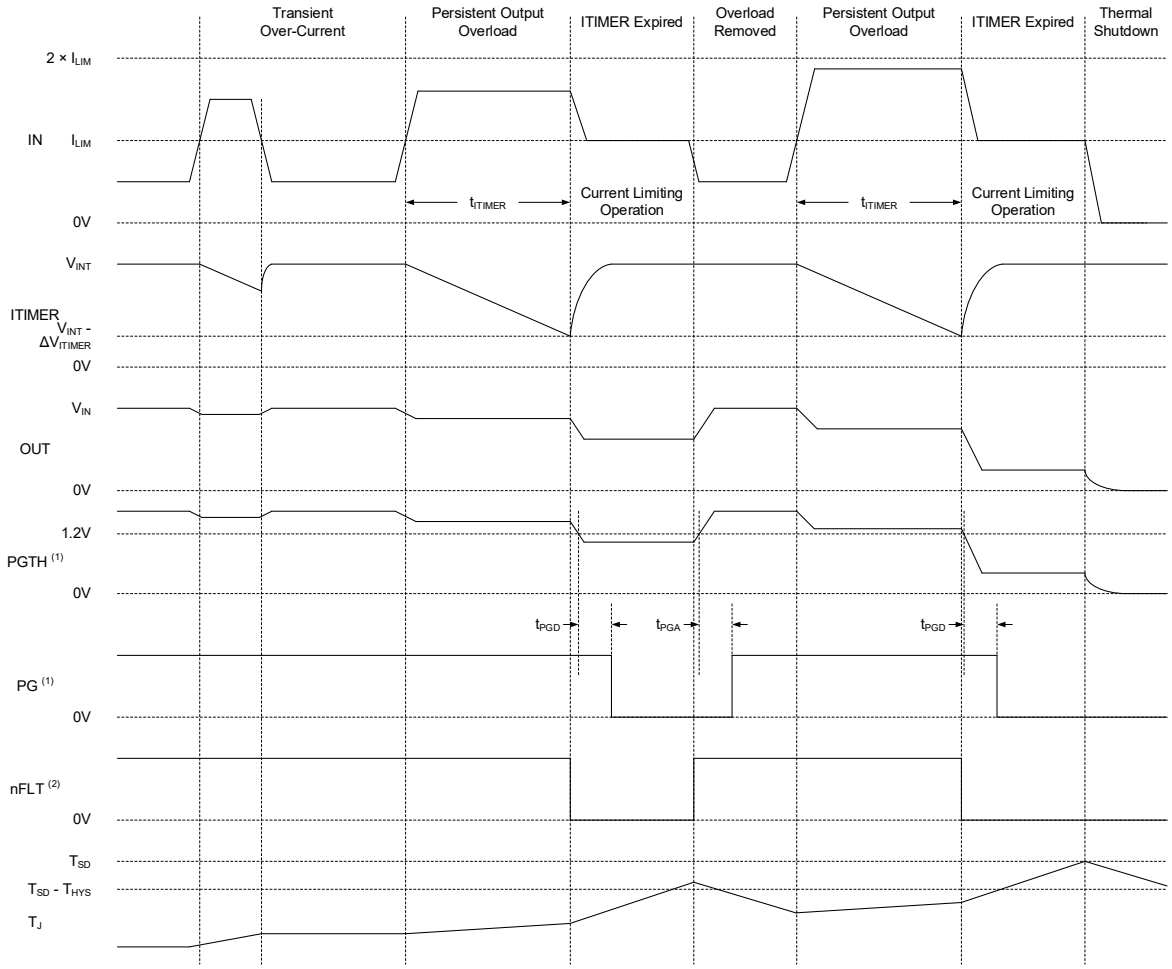
2. The current limit circuit implements the fold-back mechanism. In the fold-back region ($0V < V_{OUT} < V_{FB}$), the current limit threshold is smaller than the current limit threshold (I_{LIM}) under steady state.

3. When the ILIM is short to the GND under normal operations, it will be detected as a fault case. The load current should reach a minimum threshold I_{nFLT} for the device to detect LIM short pin.

The blanking time can be adjusted by changing the capacitance connected to the ITIMER pin. Over-current blanking time can be calculated by Equation 8.

$$t_{ITIMER}(ms) = \frac{\Delta V_{ITIMER}(V) \times C_{ITIMER}(nF)}{I_{ITIMER}(\mu A)} \quad (8)$$

DETAILED DESCRIPTION (continued)



NOTES:

1. Applicable only to SGM2546Bx and SGM2546Cx variants.

2. Applicable only to SGM2546Ax variants.

Figure 10. SGM2546Ax and SGM2546Bx Active Current Limit Response

NOTES:

1. Leaving the ITIMER pin open would make the device to cut off the circuit with the minimum possible delay.

2. Leaving the ITIMER pin floating or short to GND sets the minimum over-current blanking time. But it is not recommended to leave ITIMER pin short to GND, because it increases the current consumption of the device.

3. The active current limit set by R_{ILIM} is still valid for SGM2546Ax and SGM2546Bx during start-up, which ensures that the load current does not exceed I_{LIM} during start-up. However, there is no over-current blanking time in the start-up process.

4. For the SGM2546Bx, during over-voltage clamp condition, if an over-current event occurs, the current limit is activated immediately without the ITIMER delay.

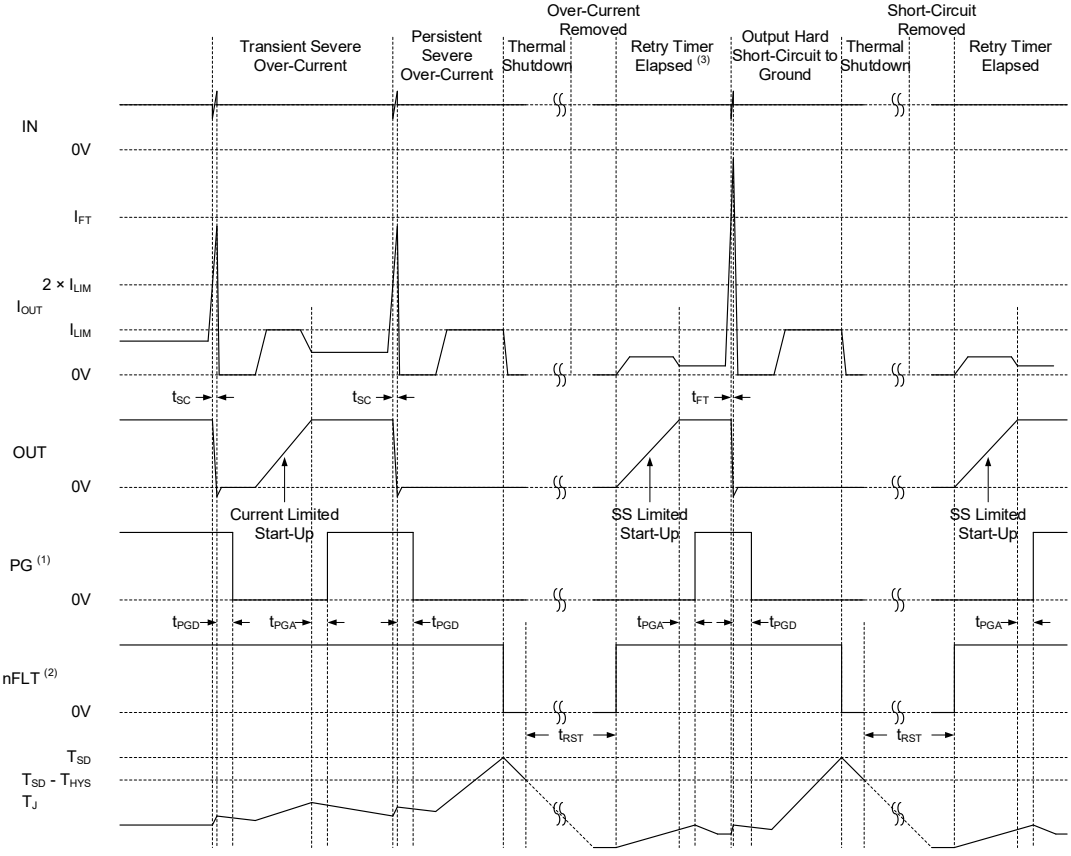
5. Increasing C_{ITIMER} can increase the over-current blanking time, but it also increases the time for C_{ITIMER} to charge to V_{INT}. If the next over-current case occurs before the C_{ITIMER} is fully charged to the V_{INT}, the current blanking time of this event will be shorter than intended.

During the active current limit, there is more power dissipation on the internal FET because the output voltage drops. If the internal temperature of the device exceeds the T_{SD}, the internal FET will be turned off, and the device will either be latched off (SGM2546xL) or restarted automatically after a certain time interval (SGM2546xR).

DETAILED DESCRIPTION (continued)

Short-Circuit Protection

When a serious over-current event similar to a short-circuit event occurs, the SGM2546 triggers a fast-trip response to prevent the system from being damaged by excessive current flowing through the device. A fast-trip comparator with scalable threshold (I_{SC} = 2 × I_{LIM}) is adopted inside the device, which allows users to program the fast-trip threshold in low current system. A fixed fast-trip threshold is also set inside the device for fast protection against hard short-circuit events in steady state. The fixed fast-trip threshold is higher than the maximum fast-trip threshold configured by user within the recommended operating range. The internal FET will be completely turned off within t_{FT} if the current exceeds I_{FT} or I_{SC}. Then the device will turn on the internal FET again after a short of deglitch time in a current limit mode. In this way, the rapid recovery of internal FET can be realized after a transient severe over-current event, and the drop of OUT voltage can be minimized. If the fault persists, the devices continue to operate in the current limit mode, causing the internal temperature of the device to rise until the thermal shutdown.



NOTES:

1. Applicable only to SGM2546Bx and SGM2546Cx variants.

2. Applicable only to SGM2546Ax variants.

3. Applicable only to SGM2546xR variants.

Figure 11. SGM2546 Short-Circuit Response

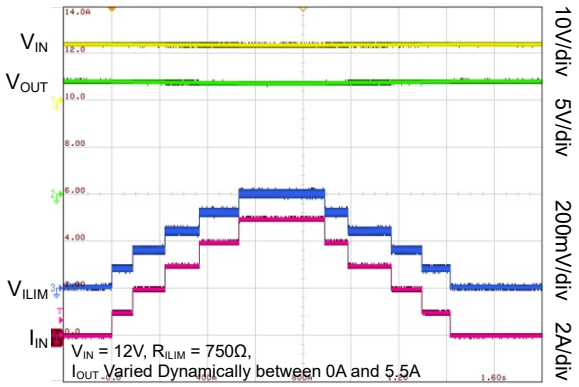
Analog Load Current Monitor

The device provides an analog current sensing output proportional to the load current at the ILIM pin, which enables the device to monitor the load current (from IN to OUT). The user can calculate the load current through the voltage of the ILIM pin connected to the R_{ILIM}. The relationship between V_{ILIM} and I_{OUT} is shown in Equation 9.

$$I_{OUT}(A) = \frac{V_{ILM}(\mu V)}{R_{ILIM}(\Omega) \times G_{IMON}(\mu A / A)} \quad (9)$$

DETAILED DESCRIPTION (continued)

The waveform below shows the analog load current monitor response to a load step at the output.



Time (200ms/div)

Figure 12. Analog Load Current Monitor Response

NOTE:

1. ILIM pin is sensitive to capacitive loads. In order to ensure the normal operation of the device, the parasitic capacitance of the ILIM pin needs to be less than 50pF.

Over-Temperature Protection (OTP)

The SGM2546 continuously monitors the temperature (T_J) of the internal die. Once the internal temperature exceeds the T_{SD}, the device shuts down immediately. The SGM2546 will not turn on until the internal temperature is lower than a safe threshold (T_{SD} - T_{HYS}).

When SGM2546xL triggers the thermal shutdown, it still remains in the shutdown state unless the equipment is re-enabled or power cycled. When SGM2546xR triggers the thermal shutdown, it remains in the shutdown state until the internal temperature of the equipment drops by T_{HYS}. After that, it will retry to turn on automatically after a t_{RST} delay time if the device is still enabled.

Table 2. Thermal Shutdown

Part Number	ENTER Thermal Shutdown	EXIT Thermal Shutdown
SGM2546xL (Latch-Off)	$T_J \geq T_{SD}$	$T_J < T_{SD} - T_{HYS}$ V_{IN} re-power up (below V_{UVP_F} and then above V_{UVP_R}) or EN/UVLO reset (below V_{SD_F} then above V_{SD_R})
SGM2546xR (Auto-Retry)	$T_J \geq T_{SD}$	$T_J < T_{SD} - T_{HYS}$ V_{IN} re-power up (below V_{UVP_F} and then above V_{UVP_R}) or EN/UVLO reset (below V_{SD_F} then above V_{SD_R}) or t_{RST} time out.

Fault Response and Indication (nFLT)

Table 3 shows the protection response of equipment under different fault conditions. The SGM2546Ax provides an active-low external fault flag pin.

Table 3. Fault Summary

EVENT	PROTECTION RESPONSE	FAULT LATCHED INTERNALLY	nFLT PIN STATUS (1)	nFLT ASSERTION DELAY (1)
Over-Temperature	Shutdown	Y	L	
Under-Voltage (UVP or UVLO)	Shutdown	N	H	
Input Over-Voltage	Shutdown (1)(2)	N	H	
	Voltage Clamp (2)	N	N/A	
Transient Over-Current ($I_{LIM} < I_{OUT} < 2 \times I_{LIM}$)	None	N	H	
Persistent Over-Current	Circuit-Breaker (3)	Y	N/A	
Persistent Over-Current	Current Limit (4)	N	L	t_{ITIMER}
Output Short-Circuit to GND	Circuit-Breaker followed by Current Limit	N	H	
ILM Pin Open (During Steady State)	Shutdown	N	L	t_{ITIMER}
ILM Pin Shorted to GND	Shutdown	Y	L	

NOTES:

1. Applicable to SGM2546Ax variants only.
2. Applicable to SGM2546Bx variants only.
3. Applicable to SGM2546Cx variants only.
4. Applicable to SGM2546Ax and SGM2546Bx variants only.

DETAILED DESCRIPTION (continued)

A latched fault can be cleared by power cycling (pulling V_{IN} to 0V) or re-enable (pulling EN/UVLO pin below V_{SD}). This will reset the nFLT pin for the SGM2546Ax and reset the t_{RST} in SGM2546xR (auto-retry version).

During a latched fault, pulling the EN/UVLO just below the UVLO threshold cannot clear the latched fault, which is true for both SGM2546xL (latch-off) and SGM2546xR (auto-retry) versions.

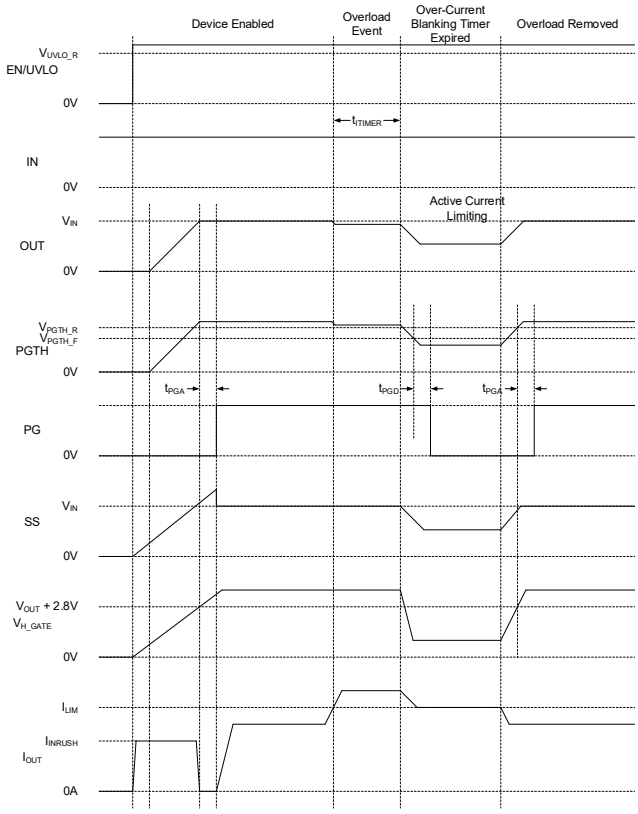
For SGM2546xR (auto-retry), after the retry delay t_{RST}, the device restarts automatically and the nFLT pin is released (SGM2546AR).

Power Good Indication (PG)

The SGM2546Bx and SGM2546Cx provide an active-high open-drain output (PG) as the indication pin of power good. It is asserted as high according to the PGTH pin voltage and the device working state. PG pin needs to be pulled up to an external power supply.

At the initial stage of power-on, PG is pulled down. Then the device enters the start-up sequence, in which the internal FET has been controlled and not fully conductive. When the gate voltage of the internal FET reaches overdrive, it is fully conductive and the start-up sequence is completed, V_{PGTH} is higher than V_{PGTH_R}, and PG is asserted high after a deglitch time (t_{PGA}).

The PG will be de-asserted when the PGTH voltage falls below V_{PGTH_F} or when the system has faults other than over-current during steady state. The deglitch time is t_{PGD}, when PG is de-asserted.



NOTES:

1. Not applicable to SGM2546Cx
2. Not applicable to SGM2546Ax

Figure 13. SGM2546Bx/Cx PG Timing Diagram

Table 4. SGM2546Bx and SGM2546Cx PG Indication Summary

EVENT	DEVICE STATUS	PG PIN STATUS	PG PIN TOGGLE DELAY
Under-Voltage UVP or UVLO)	OFF	L	
Over-Voltage (SGM2546Bx only)	ON (Clamping)	H (If PGTH pin voltage > V_{PGTH_R}) L (If PGTH pin voltage < V_{PGTH_F})	t_{PGA} t_{PGD}
Over-Voltage (SGM2546Cx only)	OFF	L	t_{PGD}
Steady State	ON	H (If PGTH pin voltage > V_{PGTH_R}) L (If PGTH pin voltage < V_{PGTH_F})	t_{PGA} t_{PGD}
Transient Over-Current	ON	H (If PGTH pin voltage > V_{PGTH_R}) L (If PGTH pin voltage < V_{PGTH_F})	t_{PGA} t_{PGD}
Persistent Overload (SGM2546Bx Only)	ON (Current Limiting)	H (If PGTH pin voltage > V_{PGTH_R}) L (If PGTH pin voltage < V_{PGTH_F})	t_{PGA} t_{PGD}
Persistent Overload (SGM2546Cx Only)	OFF (Circuit-Breaker)	L	t_{PGD}
Output Short-Circuit to GND	Fast-Trip Followed by Current Limit	H (If PGTH pin voltage > V_{PGTH_R}) L (If PGTH pin voltage < V_{PGTH_F})	t_{PGA} t_{PGD}
ILM Pin Open	OFF	L	t_{PGD}
ILM Pin Shorted to GND	OFF	L	t_{PGD}
Over-Temperature	OFF	L	t_{PGD}

DETAILED DESCRIPTION (continued)

When the device is not powered, the PG pin should be low. However, there is no effective power supply to drive the PG pin down to GND in this case. If the PG is pulled up by an independent power supply and the device is not powered, there may be a small voltage on the PG caused by sink current, which is a function of the pull-up supply and pull-up resistance connected to the PG. In order to avoid the small voltage on the PG pin being detected as logic high by the external related circuit, the sink current of the pin should be minimized.

Device Functional Modes

The SGM2546Ax and SGM2546Cx has only one functional mode within recommended operation conditions.

The SGM2546Bx offers three different OVC features according to the OVCSEL pin connection.

Table 5. SGM2546Bx Over-Voltage Clamp Threshold Selection

OVCSEL Pin Connection	Over-Voltage Clamp Threshold
Shorted to GND	3.91V
Open	5.81V
Connected to GND through a 390kΩ Resistor	13.95V

APPLICATION INFORMATION

Single Device, Self-Controlled

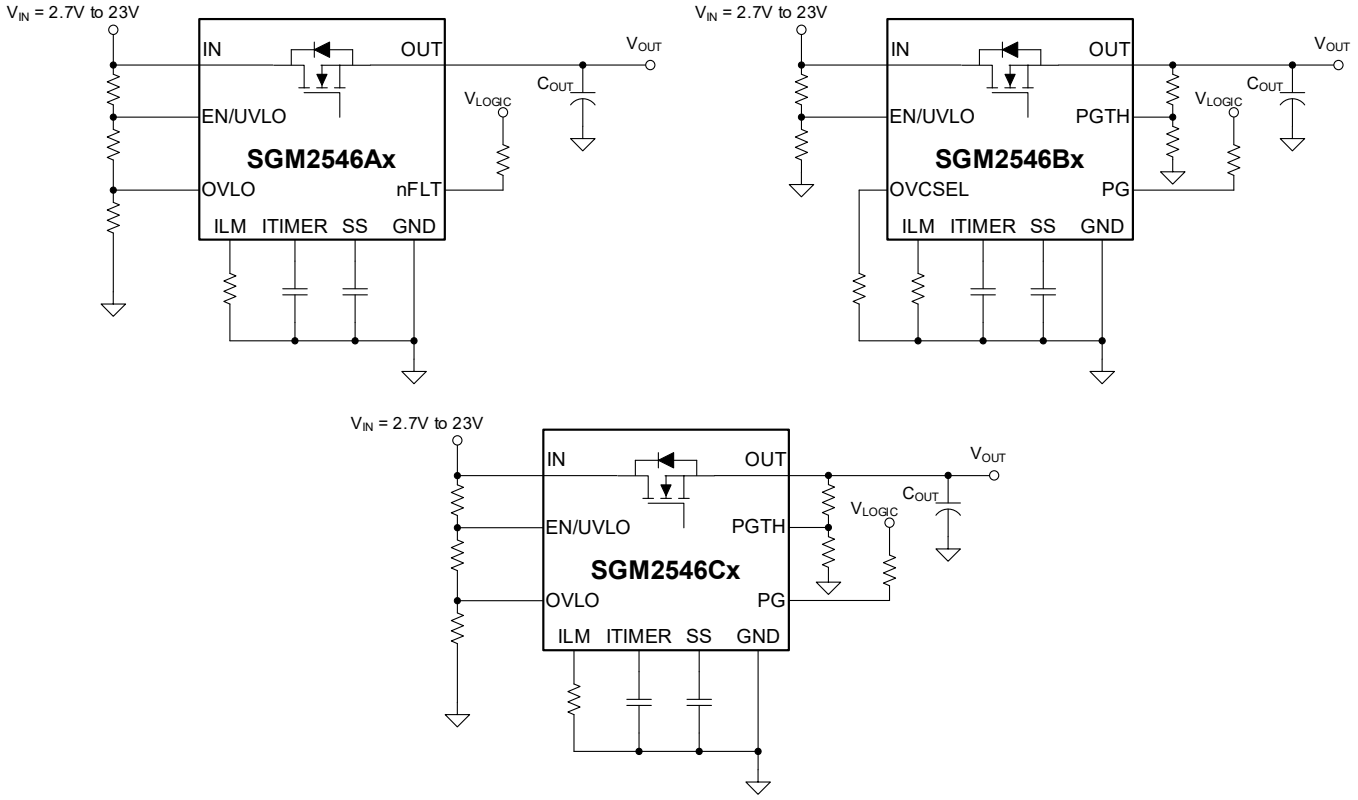


Figure 14. Single Device, Self-Controlled

In a system where the MCU is the host, the EN/UVLO or OVLO pin of the device can be driven by the GPIO of the host to realize the control of the device. The ILIM pin can be used as an ADC input to the MCU for current monitoring.

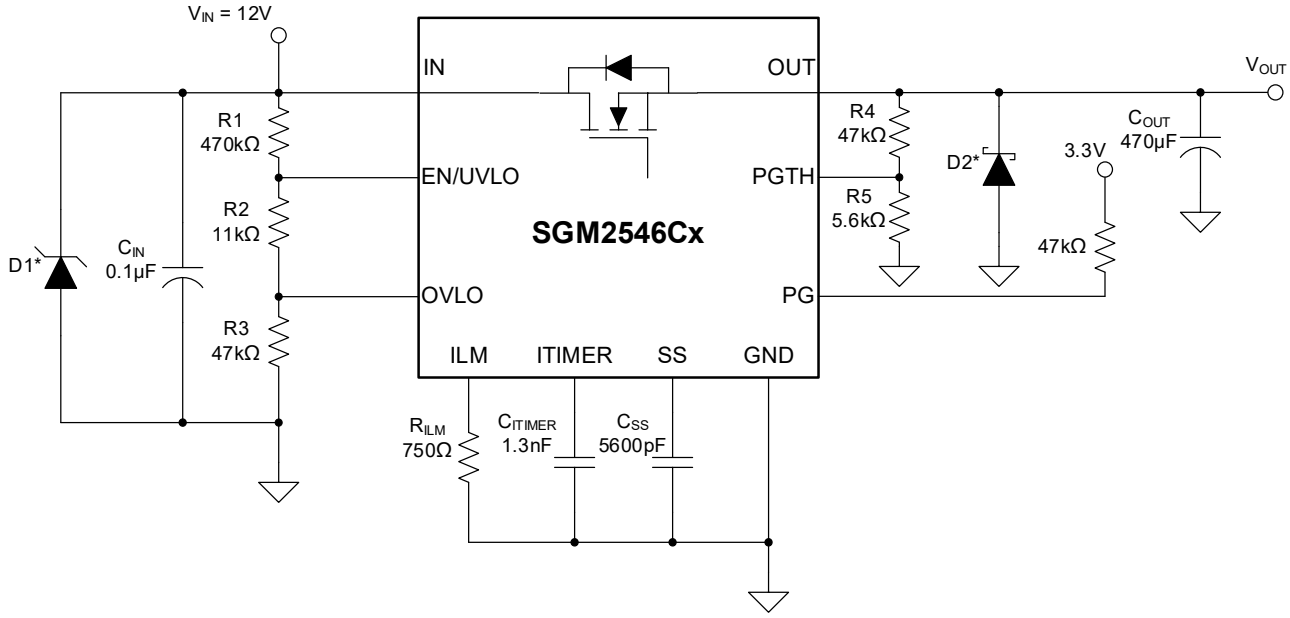
NOTE: ILIM pin is sensitive to parasitic capacitance. In order to ensure the normal operation of the device, the parasitic capacitance of the ILIM pin needs to be less than 50pF.

For the SGM2546Bx and SGM2546Cx, resistor divider of PGTH can be connected to either IN or OUT, depending on which voltage is more suitable as a power good indication.

APPLICATION INFORMATION (continued)

Typical Application

SGM2546 can be typically applied in server add-on card input power protection. The device responds quickly to fault such as over-current or short-circuit through turning off the internal FET rapidly, thus protecting the downstream load and prevent input drooping. The transient blanking time design (ITIMER) allow the device to pass through over-current during user-configurable time duration without triggering protections, which matches system transient load current profile.



* Transient protection requires optional circuit components. See the Transient Protection section for details.

Figure 15. Server Add-on Card Input Power Protection

Design Requirements

Table 6. Design Parameters

PARAMETER	VALUE
Input Supply Voltage (V_{IN})	12V
Under-Voltage Threshold (V_{IN_UV})	10.8V
Over-Voltage Threshold (V_{IN_OV})	13.2V
Output Power-Good Threshold (V_{PG})	11.4V
Maximum Continuous Current	7A
Load Transient Blanking Interval (t_{ITIMER})	1ms
Output Capacitance (C_{OUT})	470μF
Output Rise Time (t_R)	20ms
Over-Current Threshold (I_{LIM})	7.7A
Over-Current Response	Cut-Off
Fault Response	Latch-Off

Detailed Design Procedure

Device Selection

Since the application requires cut-off response to over-current with latch-off response after a fault, the SGM2546CL is selected.

Setting Under-Voltage and Over-Voltage Thresholds

The under-voltage lockout (UVLO) and the over-voltage lockout (OVLO) thresholds can be adjusted through the resistor divider network R_1, R_2 and R_3 connected from between IN, EN/UVLO, OVLO and GND pins. The resistor values are calculated using Equation 10 and Equation 11.

$$V_{IN_UV} = \frac{V_{UVLO_R} \times (R_1 + R_2 + R_3)}{R_2 + R_3} \quad (10)$$

$$V_{IN_OV} = \frac{V_{OV_R} \times (R_1 + R_2 + R_3)}{R_3} \quad (11)$$

APPLICATION INFORMATION (continued)

For minimizing the current drawn by the resistors, use higher values of resistance for R_1, R_2 and R_3.

However, the internal leakage current of the device pins would introduce errors to the calculations. Therefore, the current flow through the resistors current, I_{R123} must be chosen to be 20× greater than the leakage current expected.

From the ELECTRICAL CHARACTERISTICS, V_{OV_R} = 1.2V and V_{UVLO_R} = 1.2V. For design requirements, V_{IN_OV} = 13.2V and V_{IN_UV} = 10.8V. First, Choose the value of R_1 = 470kΩ. Then, Combing Equation 10 with Equation 11 yields R_2 = 10.7kΩ and R_3 = 48kΩ.

Using the closest standard 1% resistor values, we get R_1 = 470kΩ, R_2 = 11kΩ, and R_3 = 47kΩ.

Setting Output Voltage Rise Time (t_R)

During start-up and steady state operation, the device temperature should be well designed below the upper limit to avoid thermal shutdown. Since transient power dissipation are often much greater than the steady state, it is necessary to design the proper start-up time and inrush current for the given output capacitance to prevent the device from thermal shutdown.

From the output rise time requirement, the slew rate (SR) is calculated as

$$SR(V/ms) = \frac{V_{IN}(V)}{t_R(ms)} = \frac{12V}{20ms} = 0.6V/ms \quad (12)$$

Based on Equation 4, the C_{SS} needed to achieve this slew rate is calculated as:

$$C_{SS}(pF) = \frac{3300}{SR(V/ms)} = \frac{3300}{0.6} = 5500pF \quad (13)$$

Choose the nearest standard capacitor value, C_{SS} is 5.6nF.

The inrush current is calculated as:

$$I_{INRUSH}(mA) = SR(V/ms) \times C_{OUT}(\mu F) = 0.6 \times 470 = 282mA \quad (14)$$

Therefore, the average power dissipation of the device during start-up process is calculated as:

$$PD_{INRUSH}(W) = \frac{I_{INRUSH}(A) \times V_{IN}(V)}{2} = \frac{0.282 \times 12}{2} = 1.69W \quad (15)$$

For $P_{DINRUSH}$ = 1.69W, the thermal shutdown time should be greater than the soft-start time t_{SS}. The thermal shutdown time is more than 10s for T_A = +85℃, P_D = 1.69W. Therefore, it is safe to use 20ms soft-start time with only output capacitance and without load.

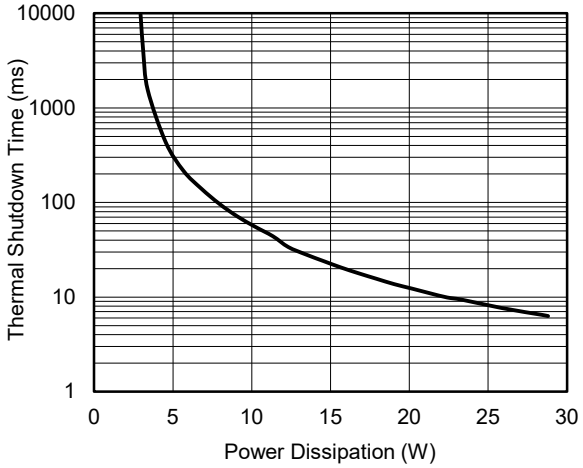


Figure 16. Thermal Shutdown Time

NOTE: For some applications, the downstream load could have low turn-on thresholds which begin drawing current during the soft-start of eFuse. This increases the power dissipation of the device during start-up and may lead to thermal shutdown. To avoid this, it is recommended to use the Power Good (PG) as the enable signal to control the downstream circuits. This design ensures the downstream load is powered until the eFuse has finished the start-up process.

Setting Power-Good Assertion Threshold

The power good assertion threshold is set by a resistor divider connected to the PGTH pin. This threshold can be calculated from Equation 16:

$$V_{PG} = \frac{V_{PGTH_R} \times (R_4 + R_5)}{R_5} \quad (16)$$

APPLICATION INFORMATION (continued)

Since R_4 & R_5 draws additional current from output, their values need to be taken into account for the acceptable leakage current of the system. The leakage current flowing through R_4 & R_5 from the supply is I_{R45} = $V_{OUT}/(R_4 + R_5)$. Considering that an external active device connected to a resistor divider causes additional leakage current, this increases the calculation error of the supply over-voltage threshold. Therefore, the leakage current flowing through R_4 & R_5 (I_{R45}) should be greater than 20 times the leakage current expected by the PGTH pin.

As can be seen from the ELECTRICAL CHARACTERISTICS, the maximum leakage current of the PGTH pin is 1μA, and V_{PGTH_R} = 1.2V. According to the application scenario requirements, V_{PG} = 11.4V. Given R_4 = 47kΩ, R_5 = 5.52kΩ can be obtained according to the above equation.

Choose the nearest standard 1% resistor values, R_4 = 47kΩ & R_5 = 5.6kΩ are selected.

Setting Over-Current Threshold (I_{LIM})

The over-current cut-off threshold is set by the R_{ILM} resistor, which is calculated as:

$$R_{ILM}(\Omega) = \frac{5747}{I_{LIM}(A)} = \frac{5747}{7.7A} = 746.4\Omega \quad (17)$$

Choose nearest 1% standard resistor value as 750Ω.

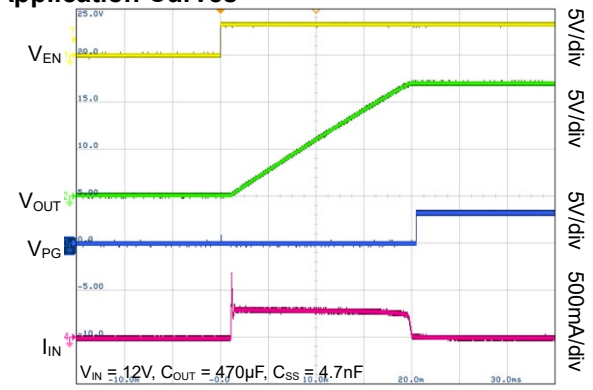
Setting Over-Current Blanking Interval (t_{ITIMER})

The transient over-current blanking time is set by the C_{ITIMER} capacitor using Equation 18.

$$C_{ITIMER}(nF) = \frac{t_{ITIMER}(ms) \times I_{ITIMER}(\mu A)}{\Delta V_{ITIMER}(V)} = \frac{1 \times 2}{1.52} = 1.32nF \quad (18)$$

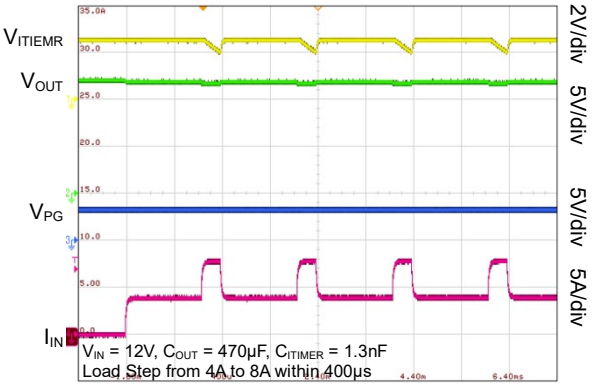
Choose nearest standard capacitor value as 1.3nF.

Application Curves



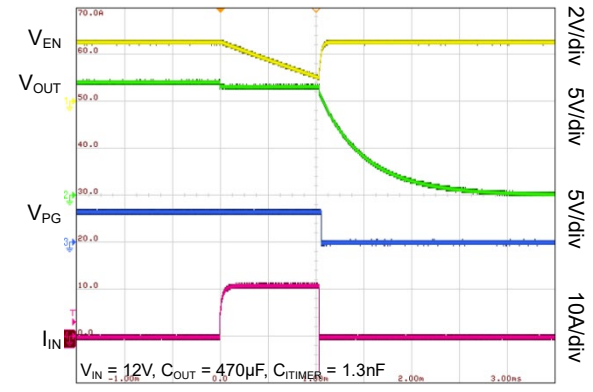
Time (5ms/div)

Figure 17. Power Up



Time (1ms/div)

Figure 18. Transient Overload



Time (500μs/div)

Figure 19. Circuit-Breaker Response

APPLICATION INFORMATION (continued)

Parallel Operation

For applications that deliver higher current to load side, two SGM2546Cx can be connected in parallel, as shown in Figure 20. In this configuration, the first device powers up firstly to provide inrush current control. The second device remains in OFF state through pulling the EN/UVLO pin low using the PG pin of the first device. After the output rise up completely, the PG pin of the first device asserts and enable the second device. After the second device turns on completely, its PG pin asserts to indicate that the system with parallel eFuses is ready for operation.

During steady state, the two device share current passively depending on the on-state resistance of device and PCB trace resistance. Therefore, possible unequal current could appear due to parameters mismatch.

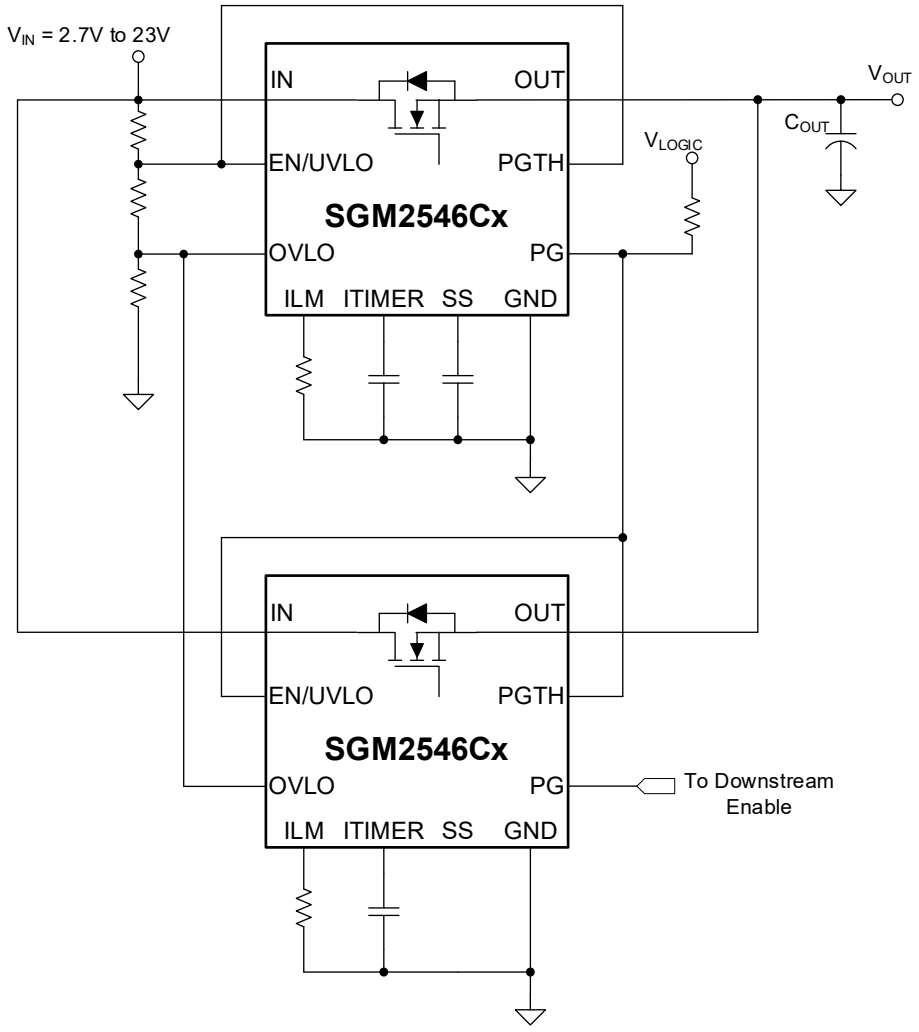
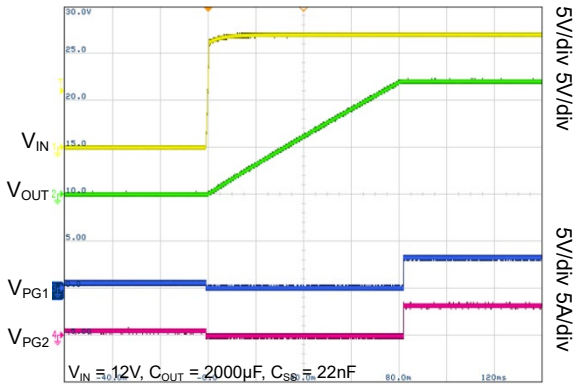


Figure 20. Two eFuses Operation in Parallel for Higher Current Delivery Capability

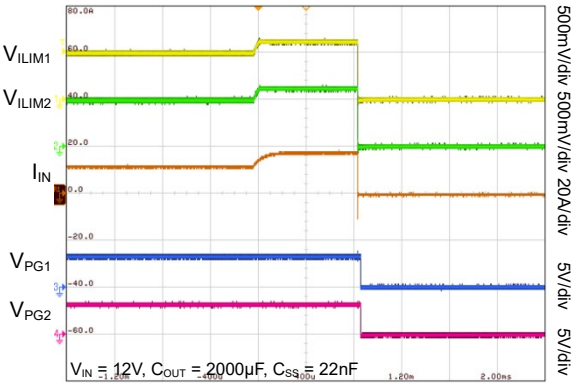
APPLICATION INFORMATION (continued)

The waveforms below illustrate the behavior of the parallel configuration during start-up as well as during steady state.



Time (20ms/div)

Figure 21. Parallel Devices Sequencing During Startup



Time (400μs/div)

Figure 22. Parallel Devices Load Current During Steady State and Overload

Power Supply Recommendations

The SGM2546 devices are designed for a supply voltage range of 2.7V ≤ V_{IN} ≤ 23V. If the distance between the power supply and the device is more than a few inches away, it is recommended to place a bypass ceramic capacitor greater than 0.1μF at the IN terminal. The rated current of the power supply must be greater than the over-current threshold set by the device, otherwise the supply voltage will drop in the event of an over-current or short-circuit.

Transient Protection

If the short-circuit or over-current limit case occurs, the device may cut off the current, and due to the parasitic inductance in series at the input and output of the device, a positive voltage spike will occur at the input with a negative voltage spike occur at the output. The amplitude of the voltage spike is determined by the parasitic inductance. These transients can cause the voltage on the device pins to exceed their maximum absolute rating if the following measures are not taken:

- The length of the wires at the input and output of the device is as small as possible.
- A TVS diode is paralleled at the input port of the device to absorb a positive voltage spike, and a Schottky diode is connected in parallel to the output port to absorb a negative voltage spike.
- Choose a large PCB GND plane.
- Connect a low ESR ceramic capacitor larger than 10μF near the OUT pin.
- A ceramic capacitor greater than 10μF is connected near the input pin to absorb and suppress transient voltage spikes and ringing.

The value of the input capacitance can be calculated from the Equation 19:

$$V_{SPIKE_ABSOLUTE} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (19)$$

Where V_{IN} is the rating of the input voltage, I_{LOAD} is the load current, L_{IN} is the effective inductance seen looking into the source, and C_{IN} is the capacitance of the input.

For applications such as USB-C interfaces, the power cord may be plugged into the output of the device. In this case, the voltage stress from OUT to IN may exceed the absolute maximum rating, so it is recommended to add a TVS diode from OUT to IN to clamp the voltage for safety.

APPLICATION INFORMATION (continued)

Figure 23 shows the circuit implementation with optional protection components.

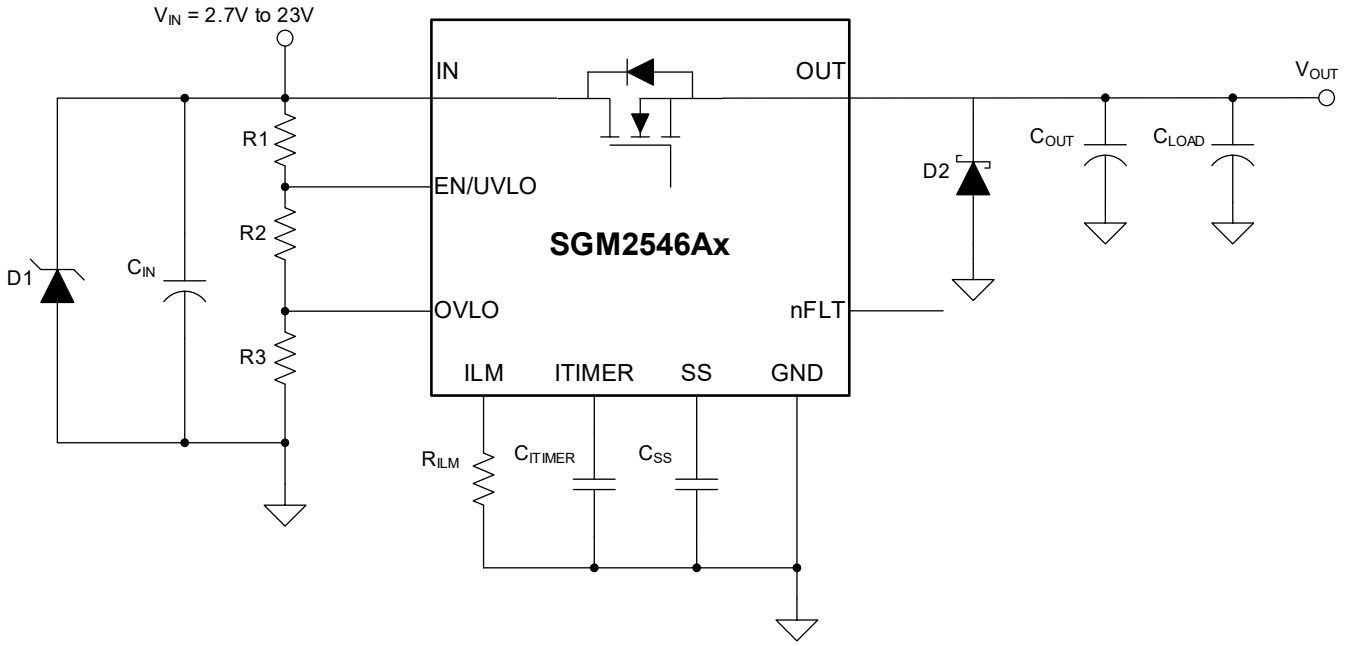


Figure 23. Circuit Implementation with Optional Protection Components

Output Short-Circuit Measurements

The output short-circuit waveform may be affected by factors such as input leads, power supply bypass, layout, device selection, circuit location, and output short-circuit method. It is difficult to obtain repeatable and similar output short-circuit test results. Therefore, the short-circuit results in this datasheet are for informational purposes only. Different short-circuit test results may be achieved because of different test conditions.

Layout Guidelines

In any application, it is recommended to connect a decoupling capacitor of 0.1μF or greater between IN and GND. This decoupling capacitor should be as close as possible to IN and GND pins.

The power path should be as wide and short as possible, with a current carrying capacity of more than twice the device's current limit.

The GND pin of the device must be connected to PCB ground which is a copper plane or island as short as possible.

The IN and OUT pins of the device are used to dissipate heat. Therefore, these two pins should be dissipated as much as possible through the copper plane on the top layer or bottom layer on the PCB. Placing thermal vias on the copper plane improves on-resistance as well as current sensing accuracy.

External components of the device as follows should be placed as close to the corresponding pins as possible:

- R_{ILIM}
- C_{SS}
- C_{ITIMER}
- Resistor dividers of EN/UVLO, OVLO and PGTH

The other end of these components is connected to ground via the shortest possible path. The ILIM pin should have a parasitic capacitance of less than 50pF, and the connection path of this pin should be away from the switching signal.

Protection components such as TVS or Schottky diodes should be connected to the device via a short path to avoid large line inductance. It is important to note that the loop area formed by the protection components should be as small as possible.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

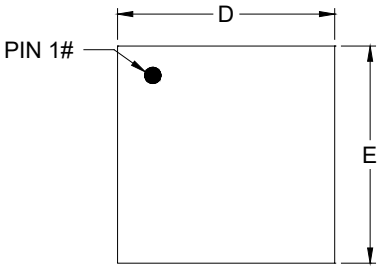
DECEMBER 2025 – REV.A.1 to REV.A.2	Page
Added SGM2546AL/SGM2546BL/SGM2546CL/SGM2546CR Variants	All

APRIL 2025 – REV.A to REV.A.1	Page
Updated Electrical Characteristics	5

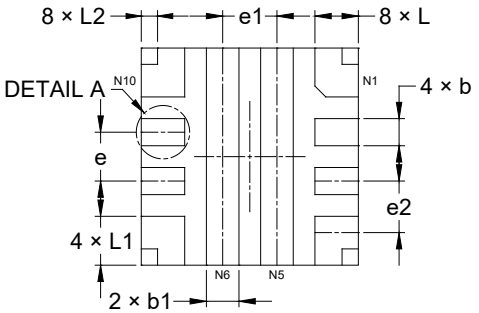
Changes from Original (DECEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

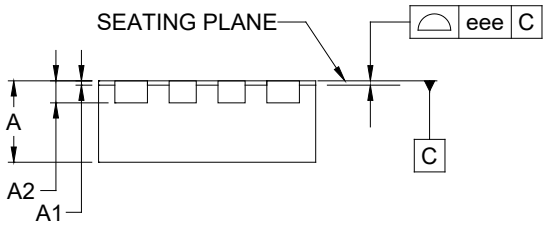
TQFN-2×2-10L



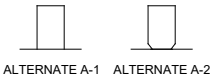
TOP VIEW



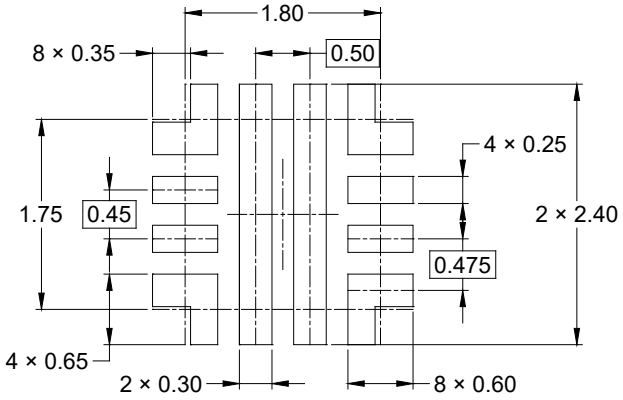
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



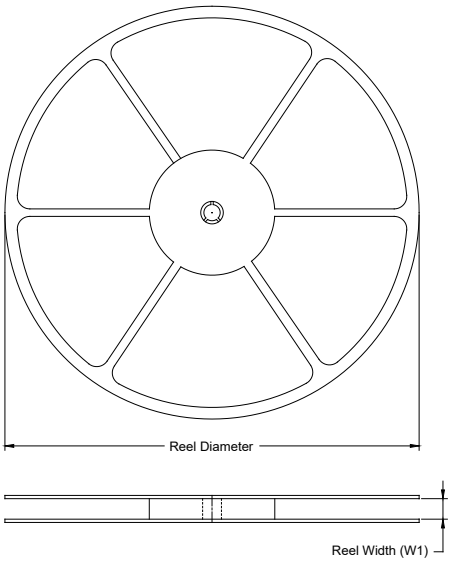
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
b1	0.250	-	0.350
D	1.900	-	2.100
E	1.900	-	2.100
e	0.450 BSC		
e1	0.500 BSC		
e2	0.475 BSC		
L	0.300	-	0.500
L1	0.350	-	0.550
L2	0.150 REF		
eee	0.080		

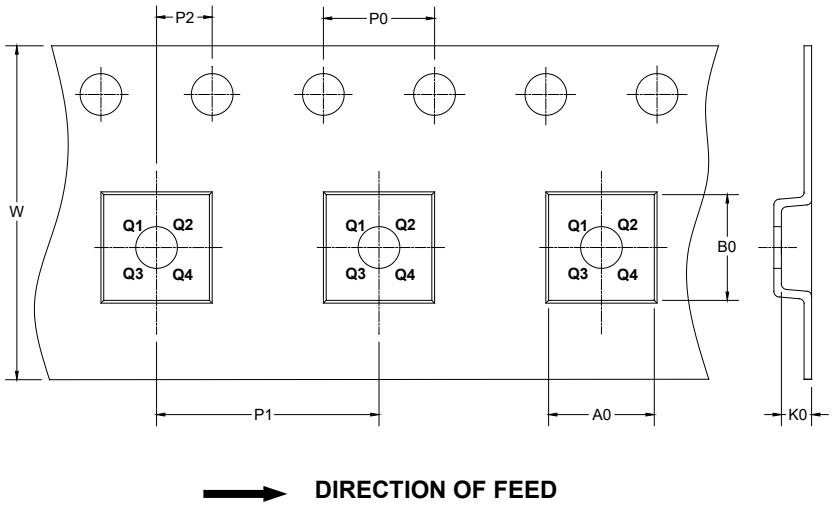
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



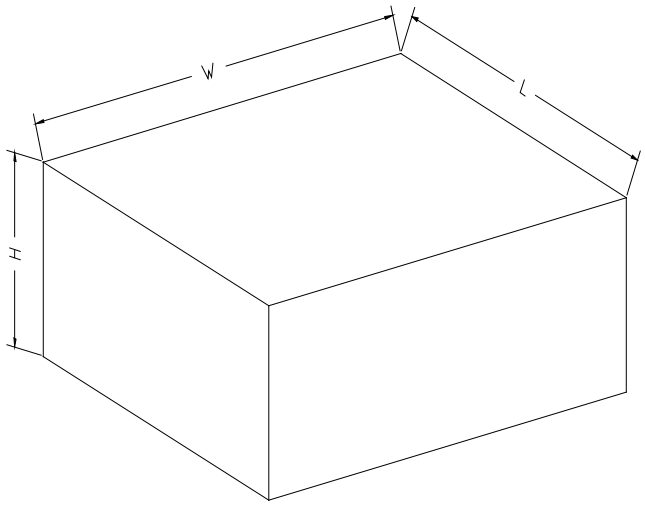
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2×2-10L	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002