1MHz，Rail-to-Rail I/O，Micro Power Operational Amplifier

Description

The ME321 is a rail-to-rail input and output voltage feedback amplifier. It has a wide input common mode voltage range and output voltage swing, and takes the minimum operating supply voltage down to 2.1V. The maximum recommended supply voltage is 5.5V. It is specified over the extended -40℃to +85℃ temperature range.

The ME321 provide 1MHz bandwidth at a low current consumption of 65μA. Very low input bias currents of 10pA enable ME321 to be used for integrators, photodiode amplifiers, and piezoelectric sensors. Rail-to-rail input and output are useful to designers for buffering ASIC in single-supply systems.

Features

- Low Cost
- Rail-to-Rail Input and Output
- 0.8mV Typical VOS
- Unity Gain Stable
- Gain-Bandwidth Product: 1MHz
- Very Low Input Bias Current: 10pA
- Supply Voltage Range: 2.1V ~ 5.5V
- Input Voltage Range:
  -0.1V ~ +5.5V with VS = 5.5V
- Low Supply Current: 65μA(dual)

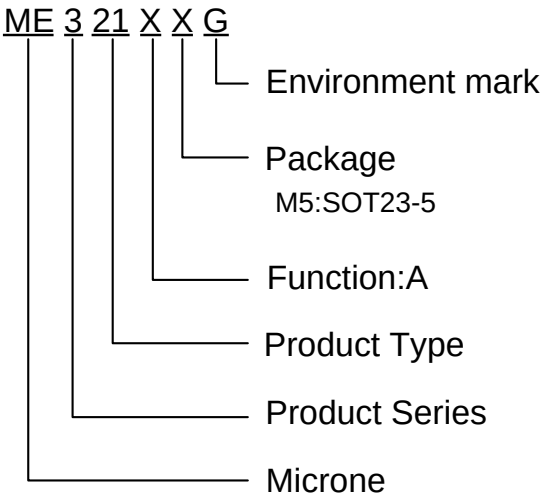
Typical Application

- Sensor Interface
- Piezoelectric Transducer Amplifier
- Mobile Communication
- Audio Output `
- Portable Systems
- Smoke Detectors
- Battery-Powered Equipment

Package

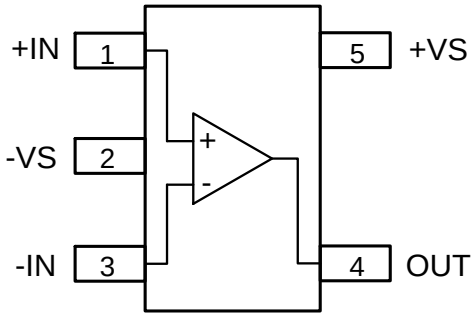
- 5-pin SOT23-5

Selection Guide



product series	Package
ME321AM5G	SOT23-5

Pin Configuration& Pin Assignment



SOT23-5

Pin Assignment

Pin Number SOT23-5	Name	Function
1	+IN	Non-inverting Input
2	-Vs	GND
3	-IN	Inverting Input
4	OUT	Output
5	+Vs	VDD

Absolute Maximum Ratings

Parameter		MIN	MAX	Unit
Supply Voltage		2.1	6	V
Input Voltage		-Vs-0.3	+Vs+0.3	V
HBM		4000V		V
Junction Temperature.		-40	150	℃
Operating Ambient Temperature Range		-40	85	℃
Storage temperature :T_{str}		-55	150	℃
Thermal resistance(Junction to air) θ_{JA}	SOT23-5	210		℃/W
Continuous Total Power Dissipation P_D	SOT23-5	0.6		W
Lead Temperature		260/10S		℃

Note: Use this IC within the stated maximum ratings. Operation beyond these limits may cause degrading or permanent damage to the device.

Electrical Characteristics

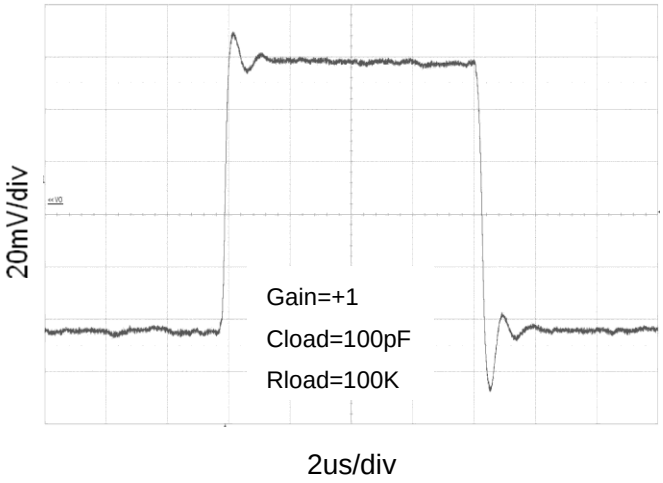
(At TA = 25 ºC ,V_S = +5V, R_L = 100kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.)

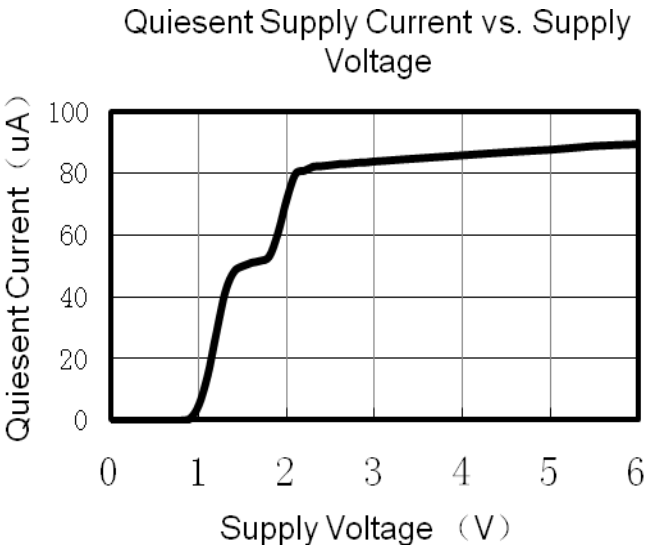
Parameter	Symbol	Conditions	Min	Typical	Max	Units
Input Offset Voltage	V_{OS}	V_{CM} = V_S/2	-4	0.8	+4	mV
Input Bias Current	I_B			10		pA
Input Offset Current	I_{OS}			1		pA
Input Common Mode Voltage Range	V_{CM}	V_S = 5.5V	-0.1		+5.5	V
Common Mode Rejection Ratio	CMRR	V_S = 5.5V, V_{CM} = -0.1V to 4V	73	85		dB
		V_S = 5.5V, V_{CM} = -0.1V to 5.6V	70	80		
Open-Loop Voltage Gain	A_{OL}	R_L= 5kΩ, V_O= +0.1V to +4.9V	80	86		dB
		R_L = 100kΩ, V_O = +0.035V to +4.965V	83	89		
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		μV/℃
Output Voltage Swing from Rail	V_{OH}	R_L = 100kΩ		4.999		V
	V_{OL}	R_L = 100kΩ		1		mV
	V_{OH}	R_L = 10kΩ		4.996		V
	V_{OL}	R_L = 10kΩ		5		mV
Output Current	I_{SOURCE}	R_L = 10Ω to V_S/2	70	85		mA
	I_{SINK}		60	75		
Operating Voltage Range			2.1		5.5	V
Power Supply Rejection Ratio	PSRR	V_S = +2.5V to +5.5V, V_{CM} = +0.5V	61	82		dB

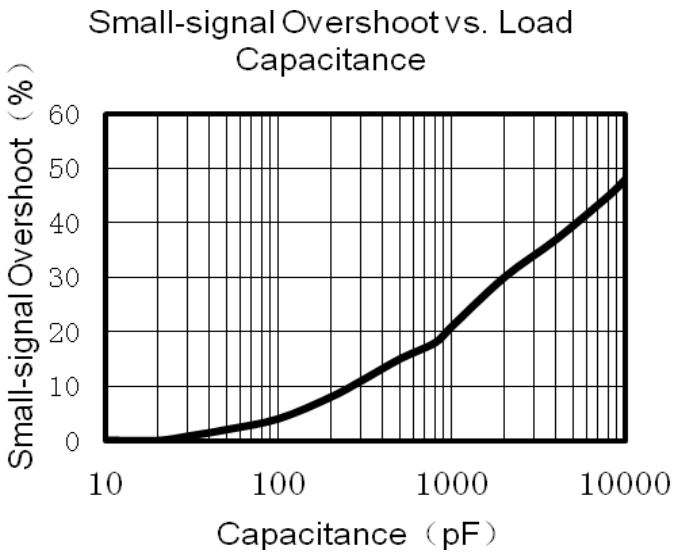
Quiescent Current(dual)	I_Q			65	85	μA
Gain-Bandwidth Product	GBW	R_L = 100kΩ，C_L=100pF		1		MHz
Phase Margin	PM	R_L = 100kΩ，C_L=100pF		63		°
Slew Rate	SR	A_V = 1, V_{OUT} = 1.5V to 3.5V，R_L = 100kΩ，C_L=100pF		0.58		V/μs
Settling Time to 0.1%	t_S	A_V = 1, V_{OUT} = 1.5V to 3.5V，R_L = 100kΩ，C_L=100pF		4.2		μs
Overload Recovery Time		V_{IN} ·Gain > V_S, R_L = 100kΩ，C_L=100pF		2.6		μs
Voltage Noise Density	e_n	f = 1kHz		27		nV / √Hz
		f = 10kHz		20		nV / √Hz

Typical Performance Characteristics

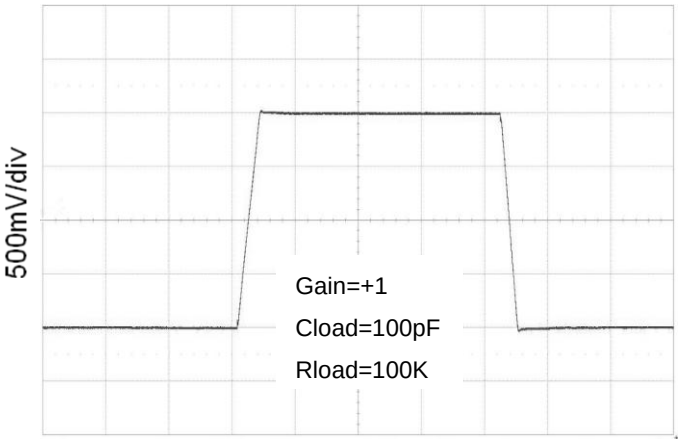
Small-Signal Step Response，100mV Step



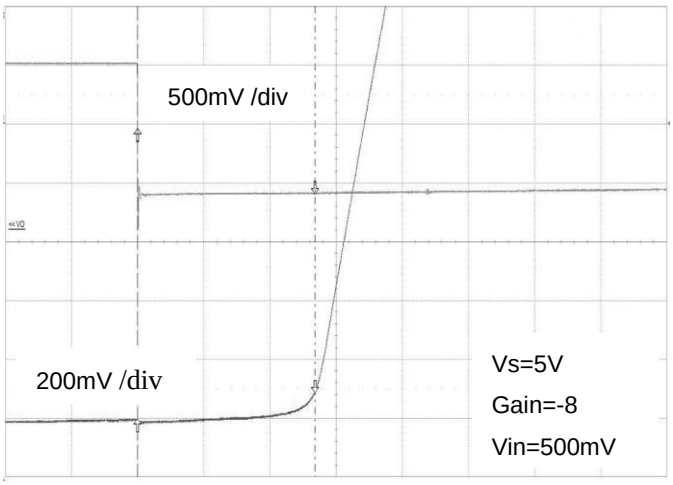




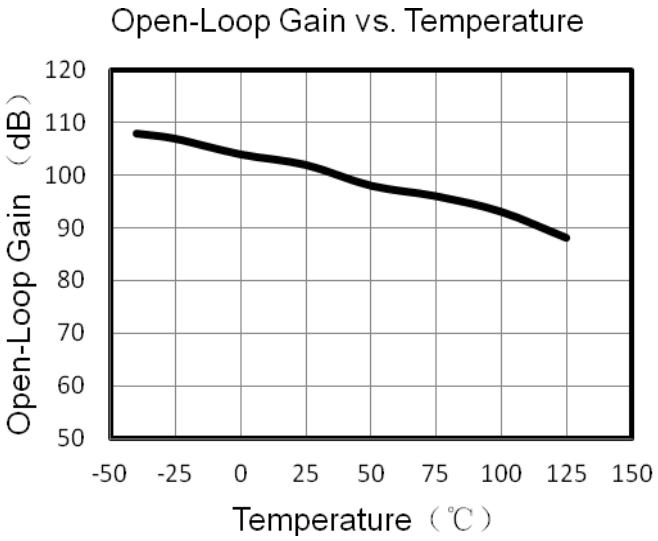
Large-Singal Step Response，2V Step

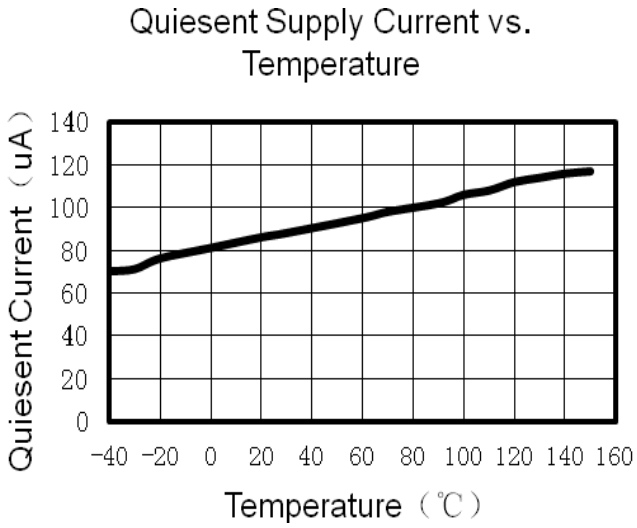


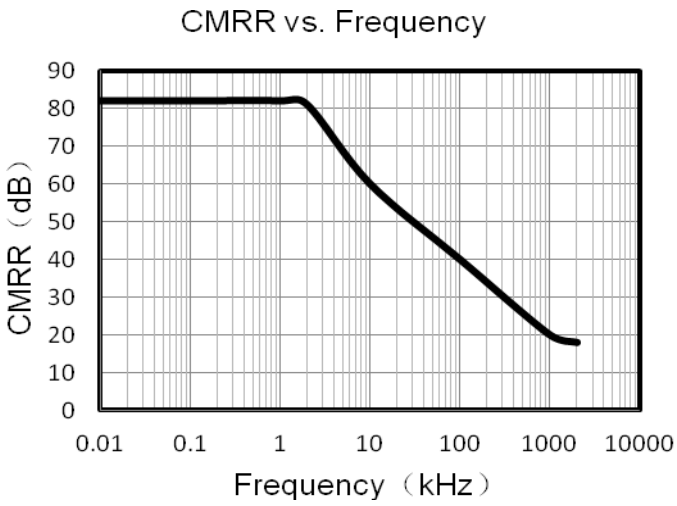
Overload Recovery Time

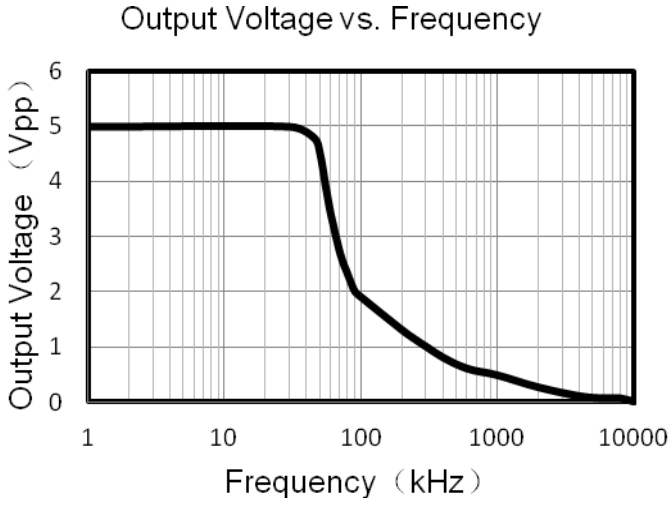

500mV /div
200mV /div
Vs=5V
Gain=-8
Vin=500mV

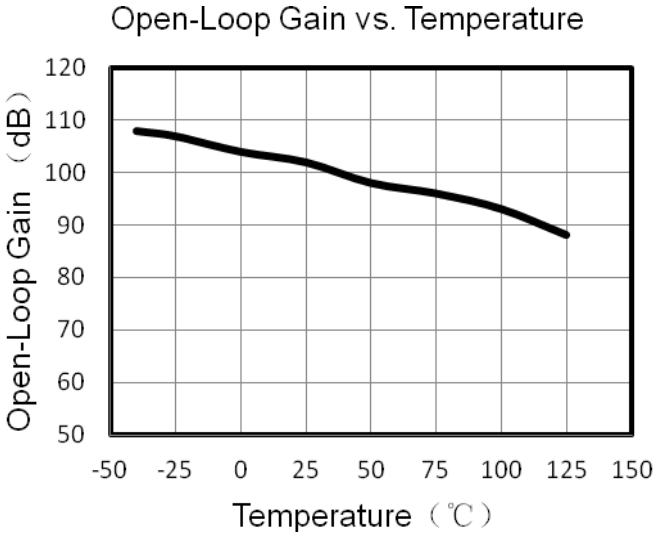
1us/div

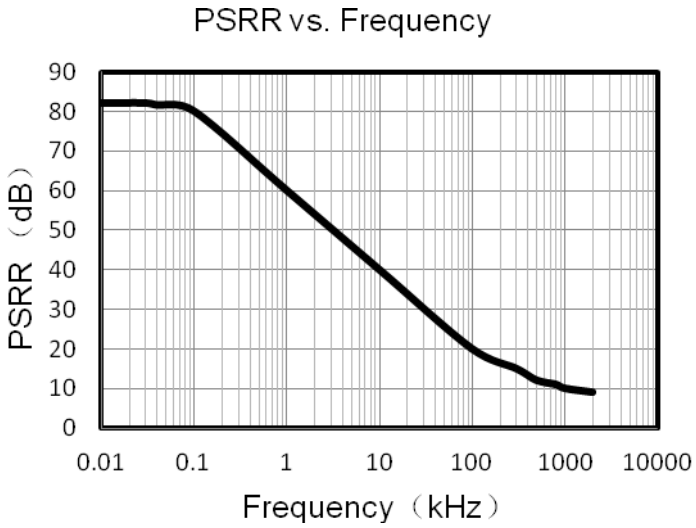

Open-Loop Gain vs. Temperature
Open-Loop Gain （dB）
120
110
100
90
80
70
60
50
-50 -25 0 25 50 75 100 125 150
Temperature （℃）

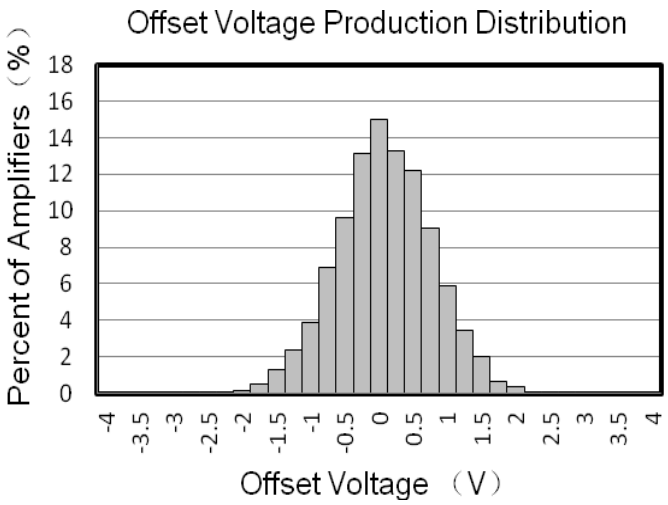

Quiesent Supply Current vs. Temperature
Quiesent Current （uA）
140
120
100
80
60
40
20
0
-40 -20 0 20 40 60 80 100 120 140 160
Temperature （℃）


CMRR vs. Frequency
CMRR （dB）
90
80
70
60
50
40
30
20
10
0
0.01 0.1 1 10 100 1000 10000
Frequency （kHz）


Output Voltage vs. Frequency
Output Voltage （Vpp）
6
5
4
3
2
1
0
1 10 100 1000 10000
Frequency （kHz）


Open-Loop Gain vs. Temperature
Open-Loop Gain （dB）
120
110
100
90
80
70
60
50
-50 -25 0 25 50 75 100 125 150
Temperature （℃）





Applications Information

The ME321 can directly drive 250pF in unity-gain without oscillation. The unity-gain follower (buffer) is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers and this results in ringing or even oscillation. Applications that require greater capacitive driving capability should use an isolation resistor between the output and the capacitive load like the circuit in Figure 1. The isolation resistor R_{ISO} and the load capacitor C_L form a zero to increase stability. The bigger the R_{ISO} resistor value, the more stable VOUT will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_{LOAD}.

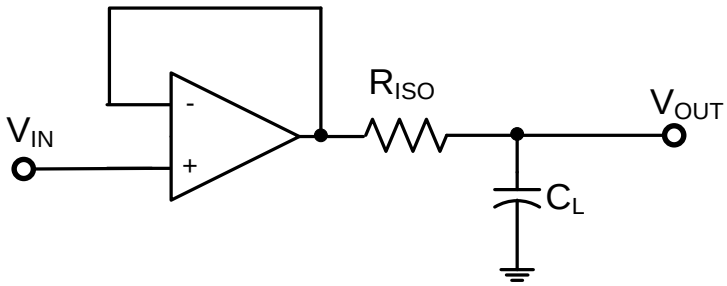


Figure 1. Indirectly Driving Heavy Capacitive Load

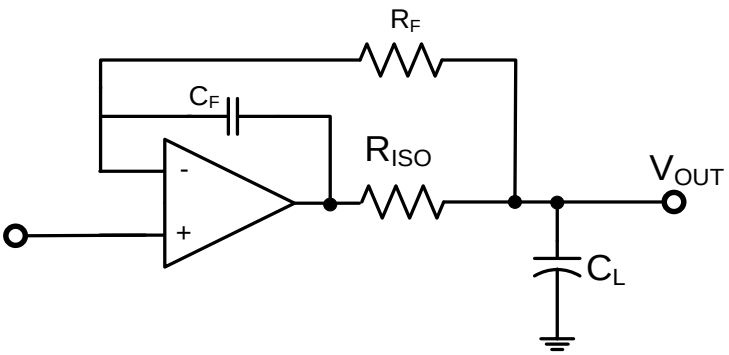


Figure 2. Indirectly Driving Heavy Capacitive Load with DC Accuracy

An improved circuit is shown in Figure 2. It provides DC accuracy as well as AC stability. RF provides the DC accuracy by connecting the inverting signal with the output. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

For non-buffer configuration, there are two other ways to increase the phase margin: (a) by increasing the amplifier's gain or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

Power-Supply Bypassing and Layout

The ME321 can operate from either a single +2.1V to +5.5V supply or dual ±1.05V to ±2.75V supplies. For single-supply operation, bypass the power supply +VS with a 0.1μF ceramic capacitor which should be placed close to the +VS pin. For dual-supply operation, both the +VS and the -VS supplies should be bypassed to ground with separate 0.1μF ceramic capacitors. 2.2μF tantalum capacitor can be added for better performance.

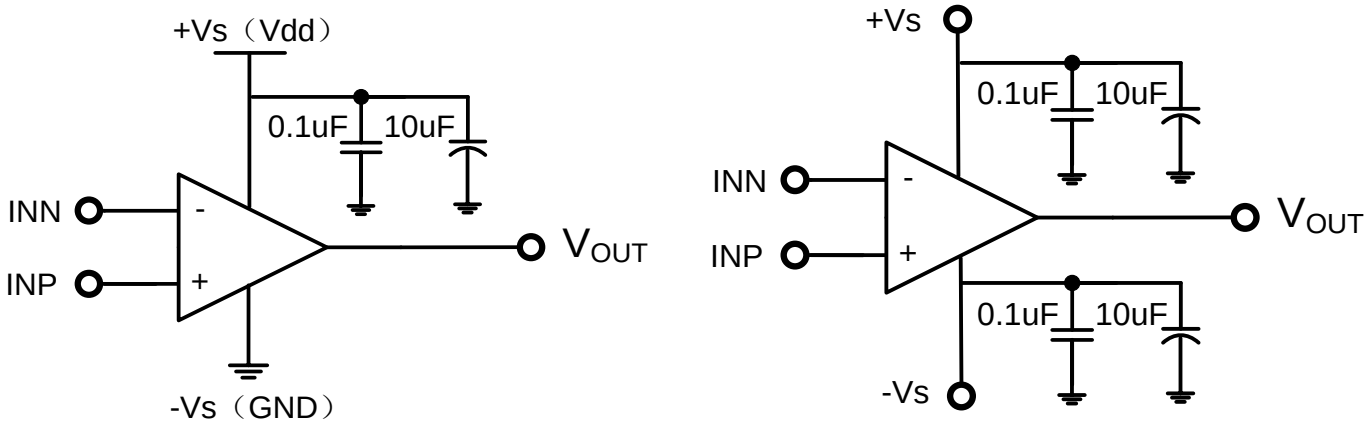


Figure 3. Amplifier with Bypass Capacitors

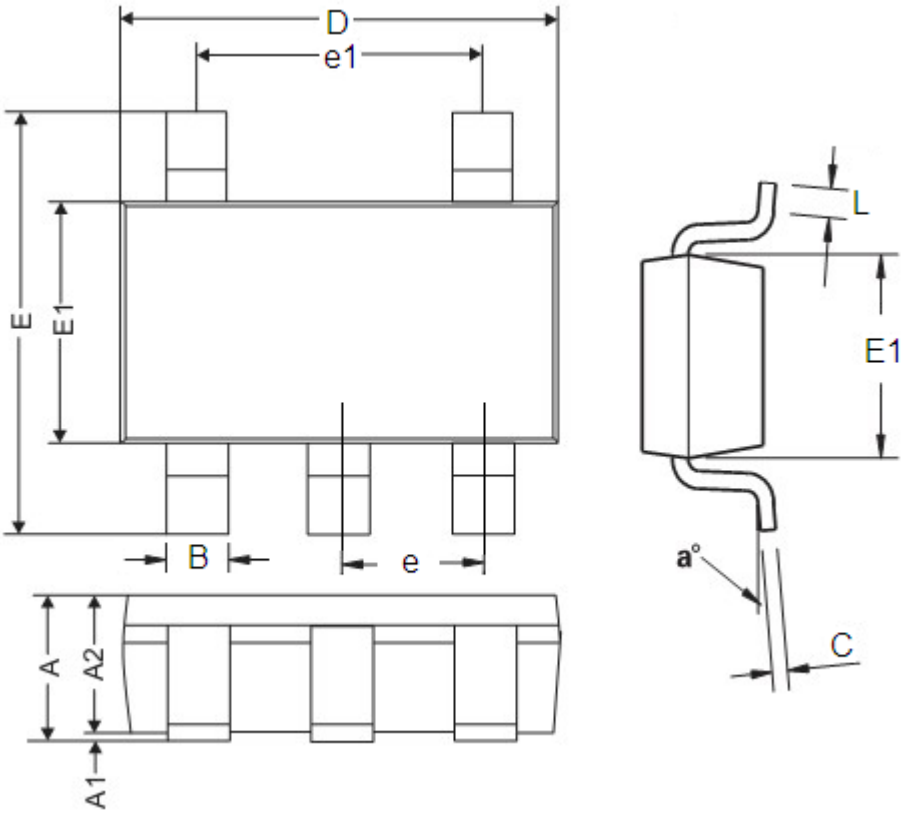
Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

Package Information

- **Package type: SOT23-5**



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	1.05	1.45	0.0413	0.0571
A1	0	0.15	0.0000	0.0059
A2	0.9	1.3	0.0354	0.0512
A3	0.6	0.7	0.0236	0.0276
b	0.25	0.5	0.0098	0.0197
c	0.1	0.23	0.0039	0.0091
D	2.82	3.05	0.1110	0.1201
e1	1.9(TYP)		0.0748(TYP)	
E	2.6	3.05	0.1024	0.1201
E1	1.5	1.75	0.0512	0.0689
e	0.95(TYP)		0.0374(TYP)	
L	0.25	0.6	0.0098	0.0236
L1	0.59(TYP)		0.0232(TYP)	
θ	0	8°	0.0000	8°
c1	0.2(TYP)		0.0079(TYP)	

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