# 3-Phase High Voltage Gate Drive IC

## General description

The PN7335 is a three-phase gate drive IC which can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 V. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3 V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an over-current or under-voltage shutdown has occurred. Over-current fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

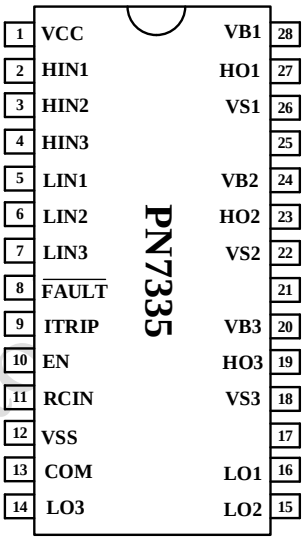
## Features

- Operation to +600 V
- Typically 200 mA/350 mA Source/Sink current
- 3.3 V/5 V/15 V input logic compatible
- dV/dt Immunity ±50 V/nsec
- Typically – 7 V negative Vs bias capability
- Gate drive supply range from 10 V to 20 V
- UVLO for all channels
- Cross-conduction prevention logic
- Over-current shutdown turns off all six drivers
- Externally adjustable Fault-clear timing
- Built-in advanced input filter
- Matched propagation delay for all channels
- Built-in bootstrap diodes

## Application

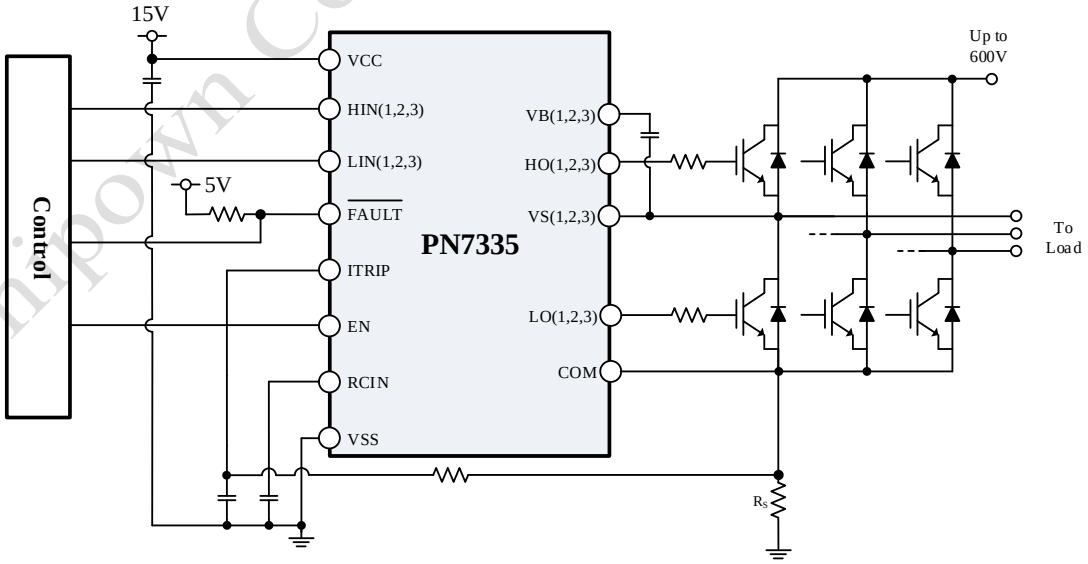
- Sewing Machine / Power Toll
- Air Conditioners
- Washing Machines
- Refrigerator
- General Purpose Inverters

## Package/Order Information




| Order code | Package |
|---|---|
| PN7335SA-A1 | SOP28 |

## Schematic Diagram of Typical Application



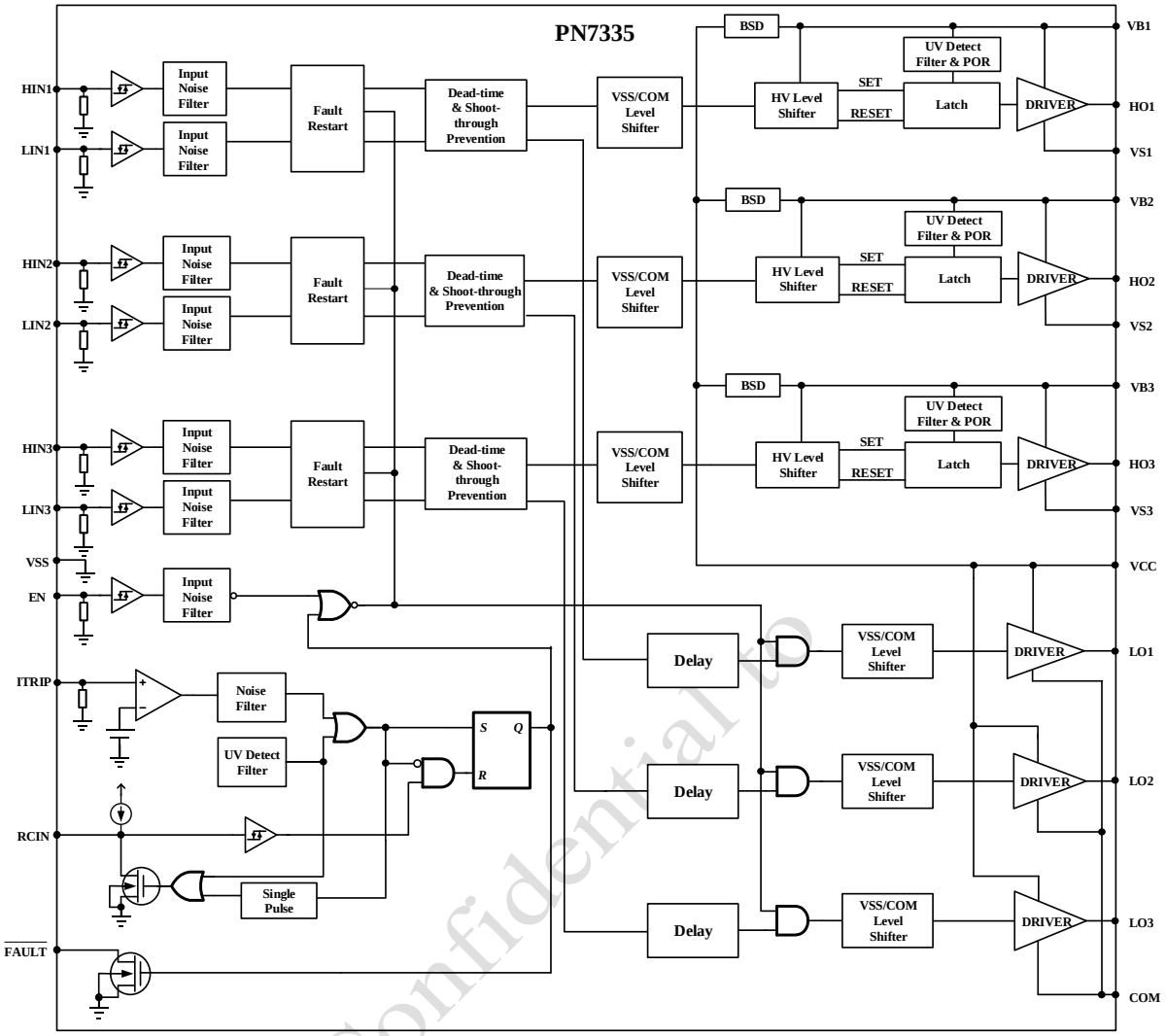

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## Pin Definitions

| Pin Name | Pin Number | Pin Function Description |
|---|---|---|
| VCC | 1 | Low side and logic fixed supply voltage |
| HIN1 | 2 | Signal Input for 1 Phase High-side |
| HIN2 | 3 | Signal Input for 2 Phase High-side |
| HIN3 | 4 | Signal Input for 3 Phase High-side |
| LIN1 | 5 | Signal Input for 1 Phase Low-side |
| LIN2 | 6 | Signal Input for 2 Phase Low-side |
| LIN3 | 7 | Signal Input for 3 Phase Low-side |
| $\overline{\text{FAULT}}$ | 8 | Indicates over-current (ITRIP)or low-side under-voltage lockout |
| ITRIP | 9 | Analog input for overcurrent shutdown. |
| EN | 10 | Logic input to enable I/O functionality |
| RCIN | 11 | External RC network input used to define FAULT CLEAR delay |
| VSS | 12 | Logic ground |
| COM | 13 | Low side gate drivers return |
| LO3 | 14 | Low side gate driver outputs for 3 Phase |
| LO2 | 15 | Low side gate driver outputs for 2 Phase |
| LO1 | 16 | Low side gate driver outputs for 1 Phase |
| VS3 | 18 | High voltage floating supply return for 3 Phase |
| HO3 | 19 | High side gate driver outputs for 3 Phase |
| VB3 | 20 | High side floating supply for 3 Phase |
| VS2 | 22 | High voltage floating supply return for 2 Phase |
| HO2 | 23 | High side gate driver outputs for 2 Phase |
| VB2 | 24 | High side floating supply for 2 Phase |
| VS1 | 26 | High voltage floating supply return for 1 Phase |
| HO1 | 27 | High side gate driver outputs for 1 Phase |
| VB1 | 28 | High side floating supply for 1 Phase |

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## Functional Block Diagram




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## Absolute Maximum Ratings

Exceeding these ratings may damage the device.
The absolute maximum ratings are stress ratings only at $T_A$=25 ℃, unless otherwise specified.

| Symbol | Definition | MIN. | MAX. | Units |
|---|---|---|---|---|
| $V_{B(1,2,3)}$ | High side floating supply | -0.3 | 625 | V |
| $V_{S(1,2,3)}$ | High side floating supply return | $V_B$ - 25 | $V_B$ + 0.3 | |
| $V_{HO(1,2,3)}$ | High side gate drive output | $V_S$ - 0.3 | $V_B$ + 0.3 | |
| $V_{CC}$ | Main power supply (reference Vss) | -0.3 | 20 | |
| | Low side supply (reference COM) | -0.3 | 25 | |
| $V_{LO(1,2,3)}$ | Low side gate drive output | COM - 0.3 | $V_{CC}$ + 0.3 | |
| $V_{IN}$ | Logic input of HIN & LIN | $V_{SS}$ - 0.3 | $V_{CC}$ + 0.3 | |
| $V_{SS}$ | Logic ground | $V_{CC}$ - 20 | $V_{CC}$ + 0.3 | |
| $V_{RCIN}$ | RCIN input voltage | $V_{SS}$ | $V_{CC}$ | |
| $V_{FLT}$ | $\overline{FAULT}$ output voltage | $V_{SS}$-0.3 | $V_{CC}$ + 0.3 | |
| $dV_S/dt$ | Allowable Offset Supply Voltage Transient | — | 50 | V/ns |
| ESD | HBM Model | 2.5 | — | kV |
| | Machine Model | 200 | — | V |
| $P_D$ | Package Power Dissipation @ $T_A$ ≤25°C (28 Lead SOP) | — | 1.6 | W |
| $R_{thJA}$ | Thermal Resistance Junction to Ambient (28 Lead SOP) | — | 78 | ℃ /W |
| $T_J$ | Junction Temperature | — | 150 | ℃ |
| $T_S$ | Storage Temperature | -55 | 150 | |

## Recommended Operating Conditions

| Symbol | Definition | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{B(1,2,3)}$ | High side floating supply | $V_S$ +10 | $V_S$ +20 | V |
| $V_{S(1,2,3)}$ | High side floating supply return | COM -7 | 600 | |
| $V_{HO(1,2,3)}$ | High side gate drive output voltage | $V_{S(1,2,3)}$ | $V_{B(1,2,3)}$ | |
| $V_{CC}$ | Low side supply (reference COM) | 10 | 20 | |
| | Main power supply (reference Vss) | 10 | 18 | |
| $V_{LO(1,2,3)}$ | Low side gate drive output voltage | 0 | $V_{CC}$ | |
| $V_{IN}$ | Logic input voltage(HIN & LIN) | 0 | $V_{CC}$ | |
| $V_{SS}$ | Logic ground | -5 | 5 | |
| $V_{RCIN}$ | RCIN input voltage | $V_{SS}$ | $V_{CC}$ | |
| $V_{FLT}$ | $\overline{FAULT}$ output voltage | $V_{SS}$ | $V_{CC}$ | |
| $T_A$ | Ambient temperature | -40 | 125 | ℃ |

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## Dynamic Electrical Characteristics

($V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15V, $C_L$ = 1000 pF and $T_A$ = 25 ℃ unless otherwise specified.)

| Symbol | Definition | MIN. | TYP. | MAX. | Units |
|---|---|---|---|---|---|
| $t_{ON}$ | Turn on propagation delay | 400 | 530 | 750 | ns |
| $t_{OFF}$ | Turn off propagation delay | 400 | 530 | 750 | |
| $t_R$ | Turn on rising time | - | 80 | 190 | |
| $t_F$ | Turn off falling time | - | 50 | 75 | |
| $t_{IN,FLT}$ | Input filter time (HIN&LIN) | 200 | 350 | 510 | |
| $t_{EN}$ | Enable low to output shutdown propagation delay | 350 | 460 | 650 | |
| $t_{EN,FLT}$ | Enable input filter time | 100 | 280 | - | |
| $t_{UVCC}$ | UVCC filter time | - | 7 | - | μs |
| $t_{UVBS}$ | UVBS filter time | - | 7 | - | |
| $t_{UVCC,FO}$ | UVCC to FAULT shutdown propagation delay | - | 7 | - | |
| $t_{UVCC,LO}$ | UVCC to LO shutdown propagation delay | - | 7 | - | |
| $t_{UVBS,HO}$ | UVBS to HO shutdown propagation delay | - | 7 | - | |
| $t_{FLTCLR}$ | $\overline{FAULT}$ Clear time at RCIN after ITRIP-fault (RCIN: C = 1nF) | 2 | 2.5 | 3 | ms |
| $t_{ITRIP}$ | ITRIP to output shutdown propagation delay | 420 | 620 | 970 | ns |
| $t_{IT,FLT}$ | ITRIP filter time | - | 400 | - | |
| $t_{FO}$ | ITRIP to $\overline{FAULT}$ propagation delay | 400 | 600 | 950 | |
| DT | Dead time | 150 | 275 | 420 | |
| MT | Delay matching time ($t_{ON}$, $t_{OFF}$) | - | - | 90 | |
| PM | Pulse width distortion[1] | - | - | 75 | |

Notes:
1. PM is defined as $PW_{IN}$-$PW_{OUT}$.

## Static Electrical Characteristics

($V_{BIAS}$ ($V_{CC}$, $V_{BS}$) = 15V, $C_L$ = 1000 pF and $T_A$ = 25 ℃ unless otherwise specified.)

| Symbol | Definition | MIN. | TYP. | MAX. | Units |
|---|---|---|---|---|---|
| $V_{UVCC+}$ | $V_{CC}$ supply under-voltage positive going threshold | 8 | 8.9 | 9.8 | V |
| $V_{UVCC-}$ | $V_{CC}$ supply under-voltage negative going threshold | 7.4 | 8.2 | 9.0 | |
| $V_{UVCCHY}$ | $V_{CC}$ supply under-voltage hysteresis | 0.3 | 0.7 | - | |
| $V_{UVBS+}$ | $V_{BS}$ supply under-voltage positive going threshold | 8.1 | 8.9 | 9.7 | |
| $V_{UVBS-}$ | $V_{BS}$ supply under-voltage negative going threshold | 7.5 | 8.3 | 9.1 | |
| $V_{UVBSHY}$ | $V_{BS}$ supply under-voltage hysteresis | - | 0.6 | - | |
| $I_{LK}$ | High-side floating supply leakage current | - | - | 50 | μA |
| $I_{QBS}$ | Quiescent $V_{BS}$ supply current (per 1phase) | - | 110 | 150 | |
| $I_{QCC}$ | Quiescent $V_{CC}$ supply current | - | 0.3 | 1 | mA |
| $I_{PBS}$ | Operating $V_{BS}$ supply current | - | 400 | 600 | μA |
| $I_{PCC}$ | Operating $V_{CC}$ supply current (per 1phase) | - | 1.3 | 1.8 | mA |

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| Symbol | Definition | MIN. | TYP. | MAX. | Units |
|---|---|---|---|---|---|
| $V_{OH}$ | High level output voltage drop, $V_{BIAS}$ - $V_O$ | - | 0.9 | 1.4 | V |
| $V_{OL}$ | Low level output voltage drop, $V_O$ | - | 0.4 | 0.6 | |
| $I_{O+}$ | Output high short circuit pulsed current | 120 | 200 | - | mA |
| $I_{O-}$ | Output low short circuit pulsed current | 250 | 350 | - | |
| $V_{IH}$ | High level input threshold voltage | 2.5 | - | - | V |
| $V_{IL}$ | Low level input threshold voltage | - | - | 0.8 | |
| $V_{CLAMP}$ | Input clamp voltage (HIN, LIN, ITRIP, EN) | 5.2 | 5.6 | 5.9 | |
| $I_{HIN+}$ | Input bias current (HO = High) | - | 700 | 900 | μA |
| $I_{HIN-}$ | Input bias current (HO = Low) | - | - | 1 | |
| $I_{LIN+}$ | Input bias current (LO = High) | - | 700 | 900 | |
| $I_{LIN-}$ | Input bias current (LO = Low) | - | - | 1 | |
| $V_{RCIN,TH}$ | RCIN positive going threshold | - | 5.35 | - | V |
| $V_{RCIN,HY}$ | RCIN hysteresis | - | 3 | - | |
| $I_{RCIN}$ | RCIN internal current source | 2 | 3 | 4 | μA |
| $R_{RCIN,ON}$ | RCIN low on resistance | - | 50 | 100 | Ω |
| $V_{IT,TH+}$ | ITRIP positive going threshold | 0.42 | 0.46 | 0.5 | V |
| $V_{IT,TH-}$ | ITRIP negative going threshold | - | 0.4 | 0.49 | |
| $V_{IT,HY}$ | ITRIP hysteresis | - | 0.06 | - | |
| $I_{ITRIP+}$ | “High” ITRIP input bias current | - | 5 | 40 | μA |
| $I_{ITRIP-}$ | “Low” ITRIP input bias current | - | - | 1 | |
| $V_{EN,TH+}$ | Enable positive going threshold | 2.5 | - | - | V |
| $V_{EN,TH-}$ | Enable negative going threshold | - | - | 0.8 | |
| $I_{EN+}$ | “High” Enable input bias current | - | 5 | 40 | μA |
| $I_{EN-}$ | “Low” Enable input bias current | - | - | 1 | |
| $R_{FO,ON}$ | $\overline{FAULT}$ low on resistance | - | 50 | 100 | Ω |
| $R_{BSD}$ | Internal Bootstrap Equivalent Resistor Value | - | 280 | - | Ω |
| $V_{F,BSD}$ | Bootstrap diode forward voltage between VB and VCC | | 0.7 | | V |
| $I_{F,BSD}$ | Bootstrap diode forward current between VB and VCC ($V_F$=4V) | - | 14 | 25 | mA |

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## Function Timing Diagram

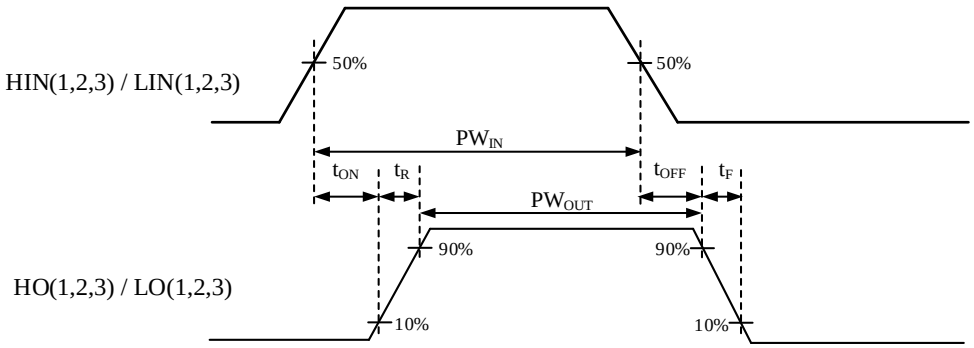



Fig.1 Switching timing waveform

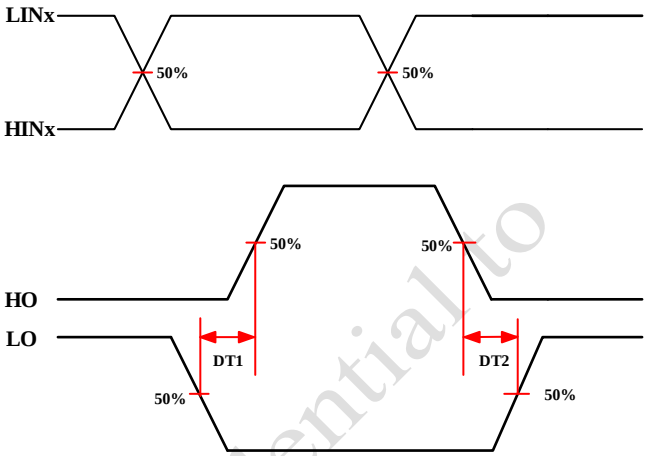



Fig.2 Dead time definition

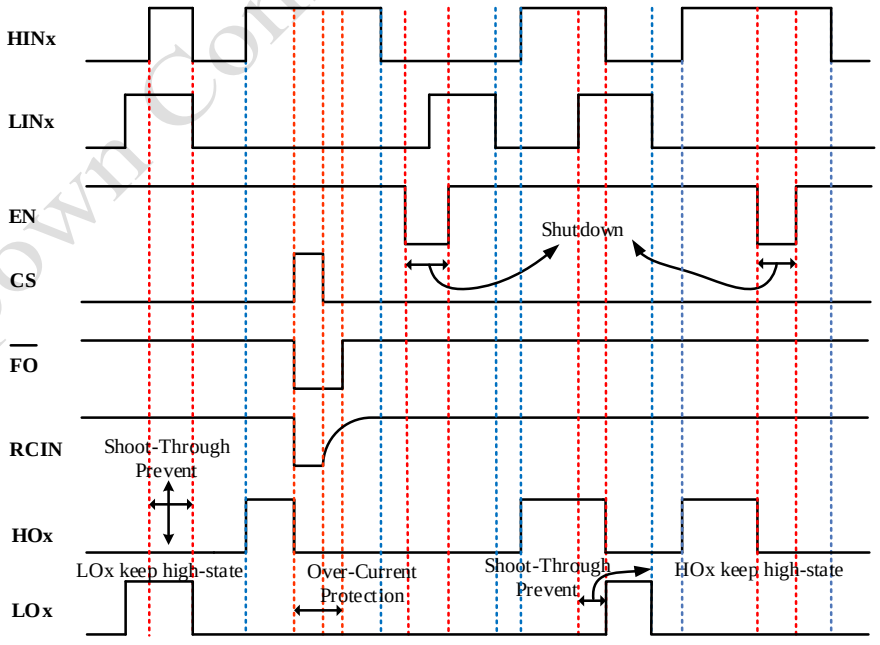



Fig.3 Input / Output timing waveform

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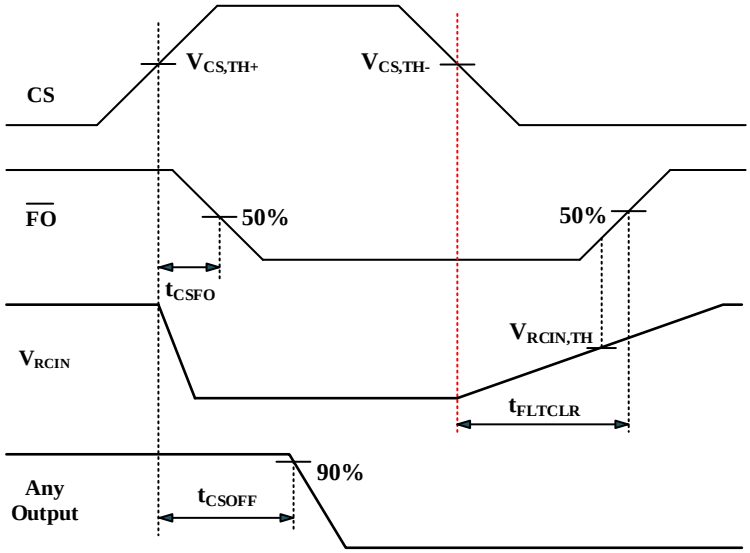



Fig.4 Delay Time During Over-Current Protection

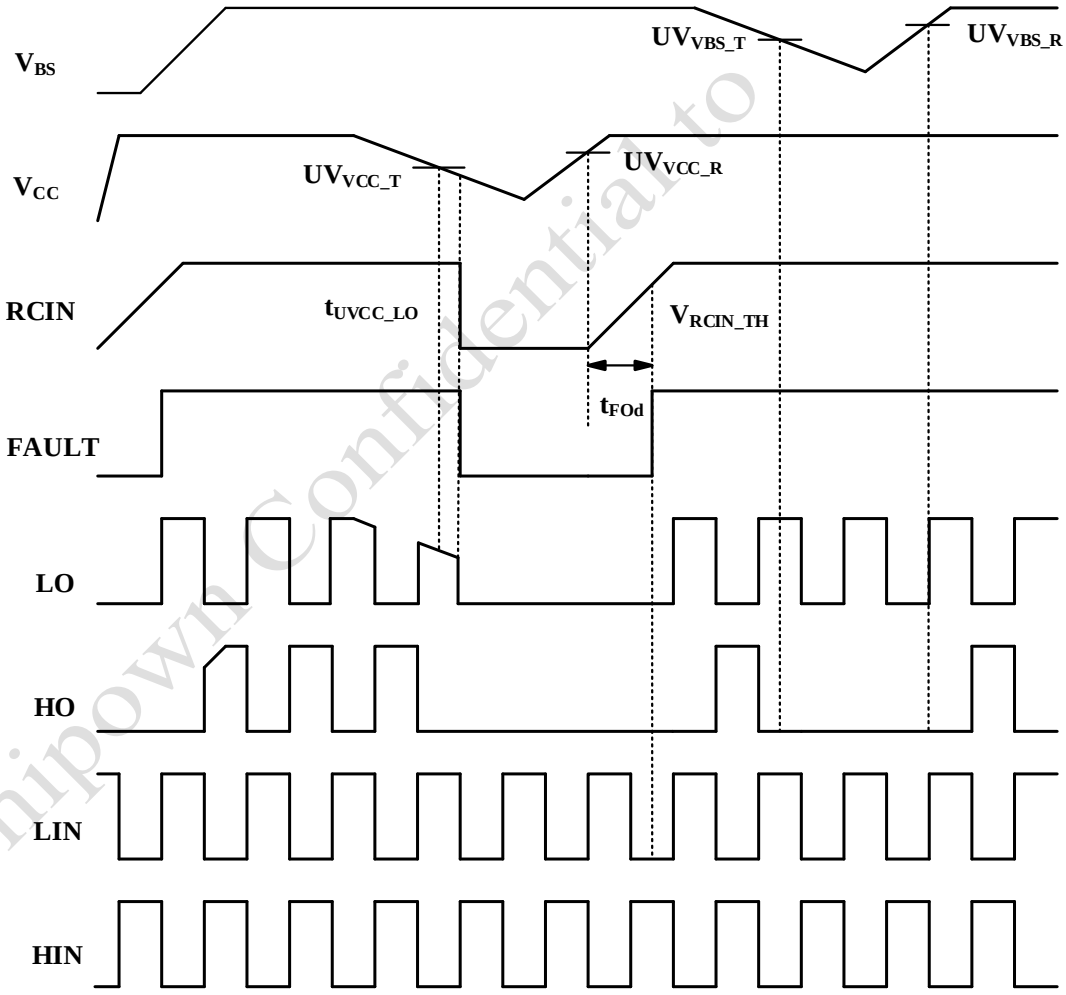



Fig.5 $V_{CC}$ and $V_{BS}$ under-voltage lockout protection

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## Characterization Curves

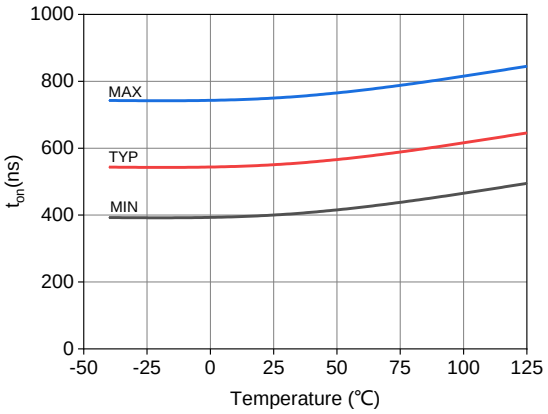



Fig6. $t_{ON}$ vs. temperature

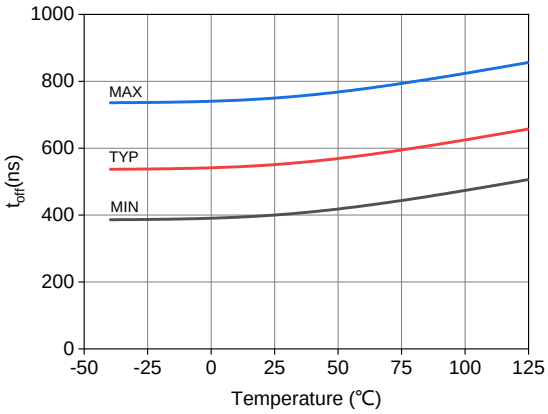



Fig 7. $t_{OFF}$ vs. temperature

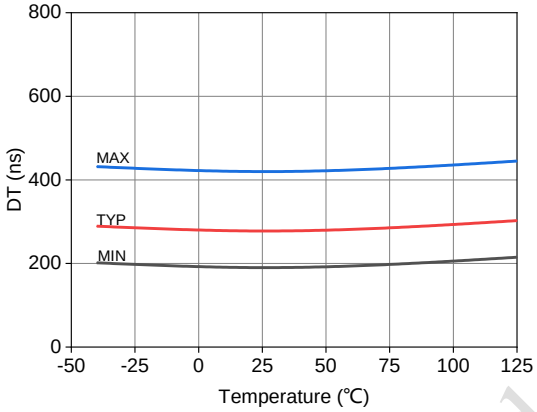



Fig 8. DT vs. temperature

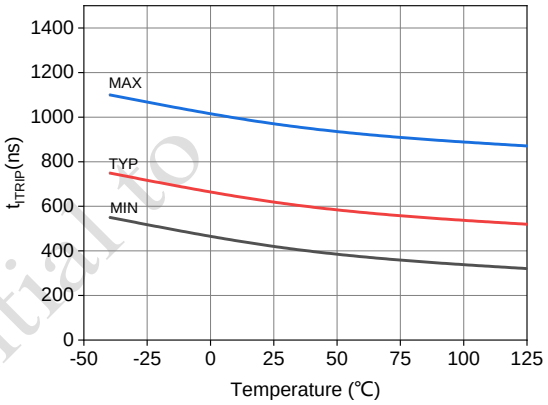



Fig 9. $t_{TRIP}$ vs. temperature

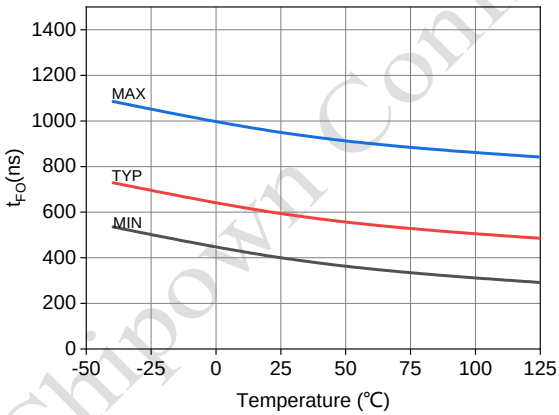



Fig 10. $t_{FO}$ vs. temperature

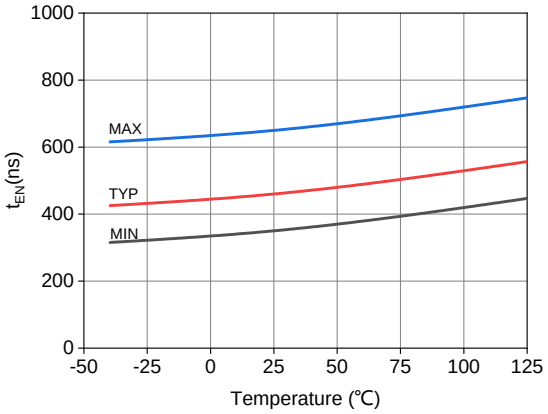



Fig 11. $t_{EN}$ vs. temperature

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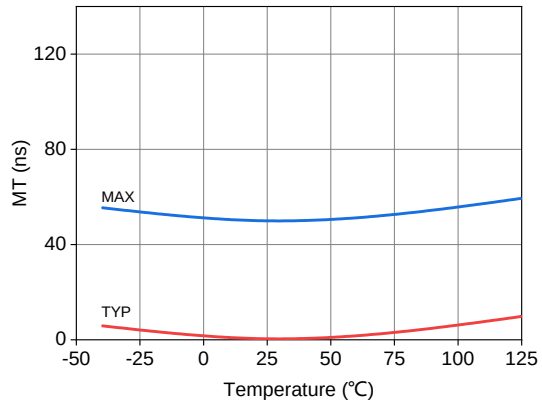



Fig 12. MT vs. temperature

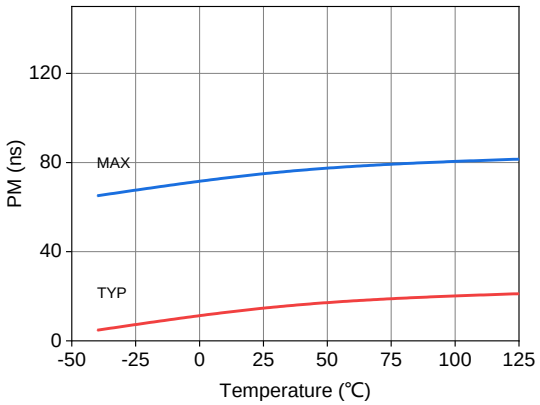



Fig 13. PM vs. temperature

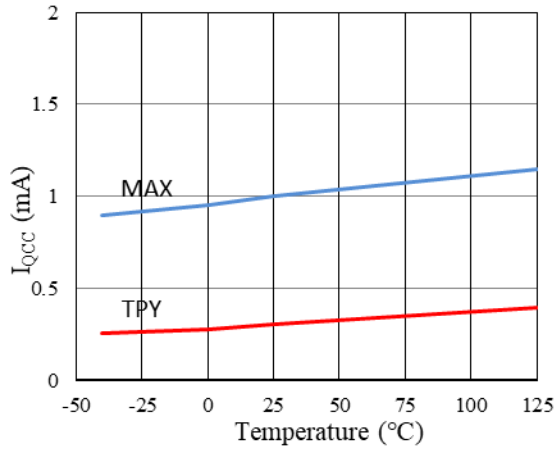



Fig 14. $I_{QCC}$ vs. temperature

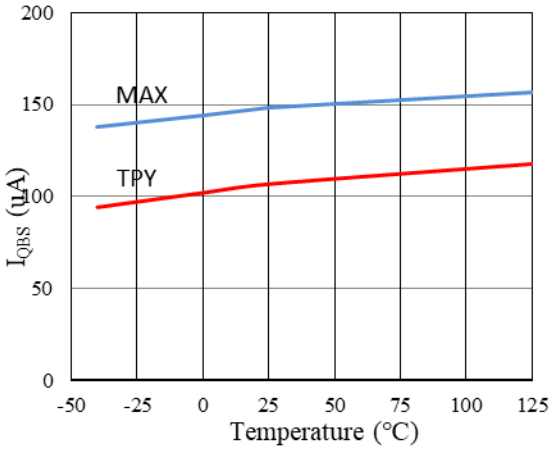



Fig 15 .$I_{QBS}$ vs. temperature

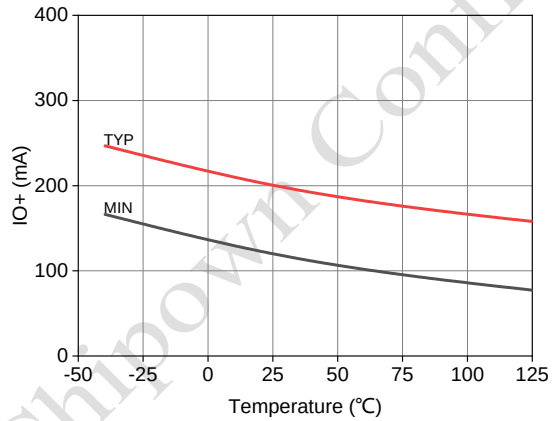



Fig 16. $I_{O+}$ vs. temperature

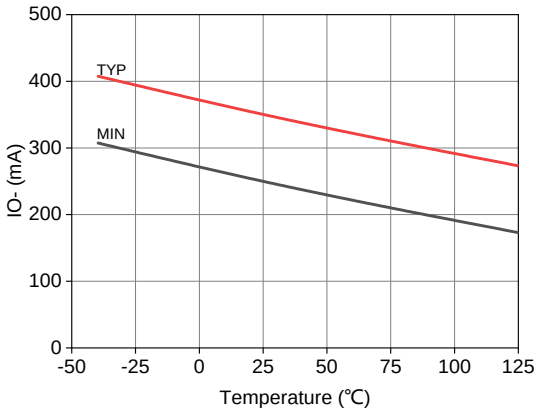



Fig 17. $I_{O-}$ vs. temperature

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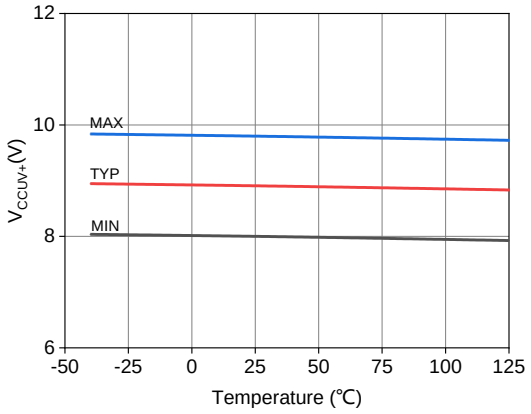



Fig 18. $UV_{VCC+}$ vs. temperature

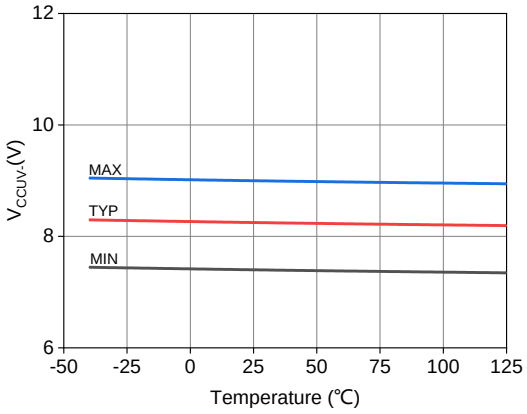



Fig 19. $UV_{VCC-}$ vs. temperature

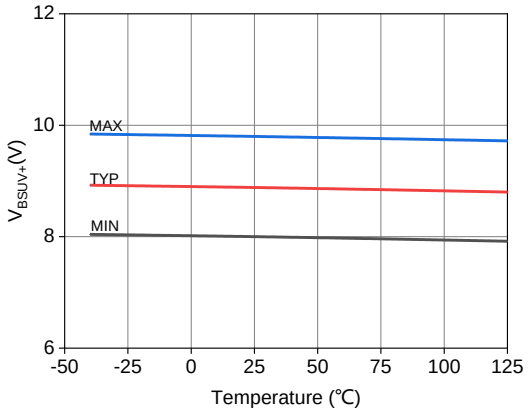



Fig 20. $UV_{VBS+}$ vs. temperature

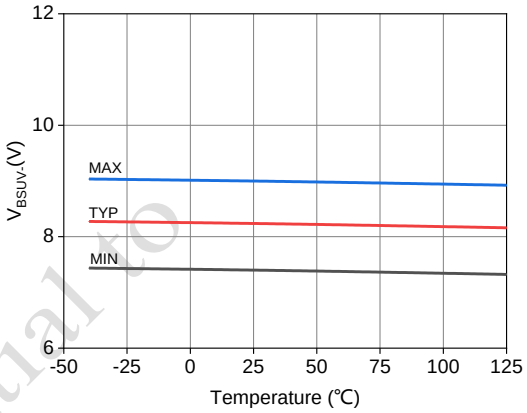



Fig 21. $UV_{BS-}$ vs. temperature

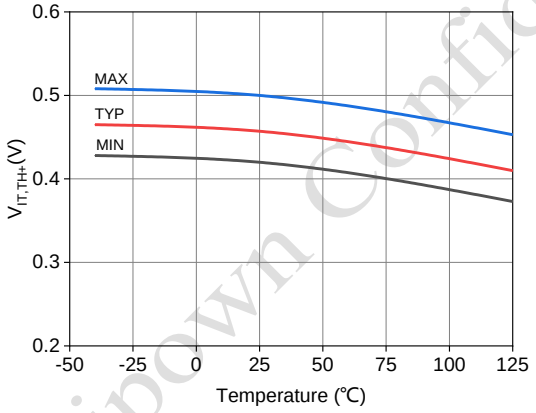



Fig 22. $V_{IT,TH+}$ vs. temperature

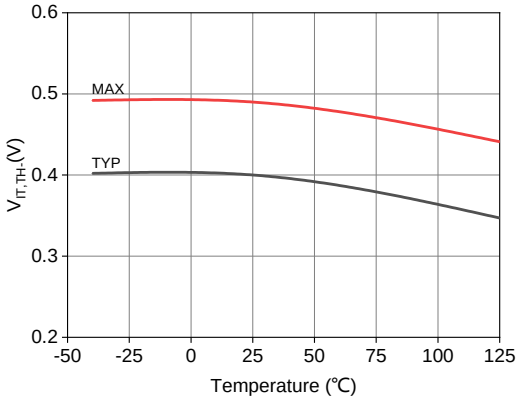



Fig 23. $V_{IT,TH-}$ vs. temperature

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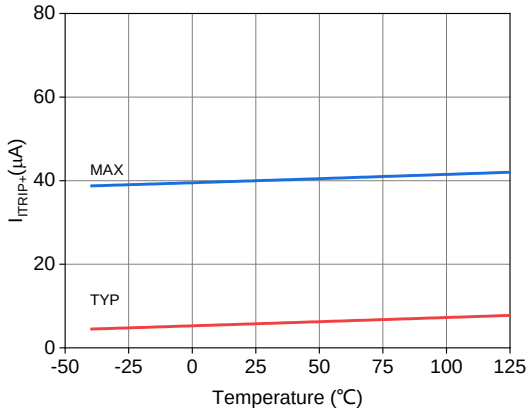



Fig 24 .$I_{ITRIP+}$ vs. temperature

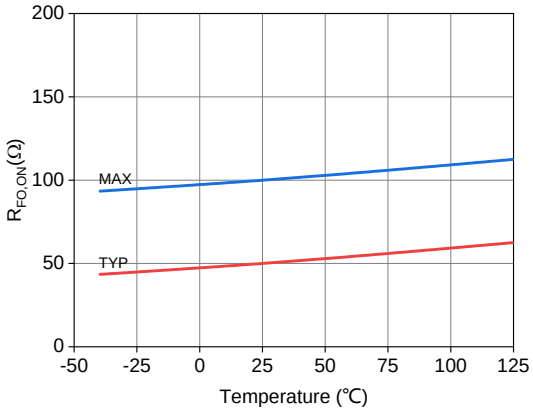



Fig 25. $R_{FO,ON}$ vs. temperature

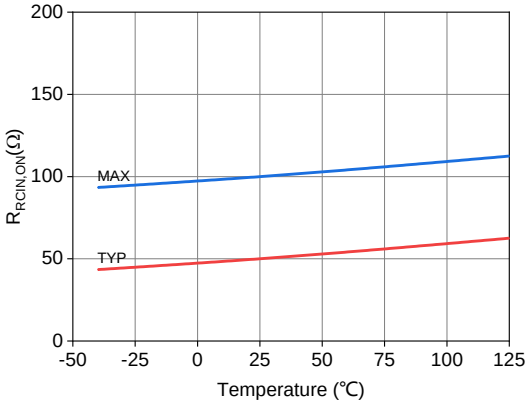
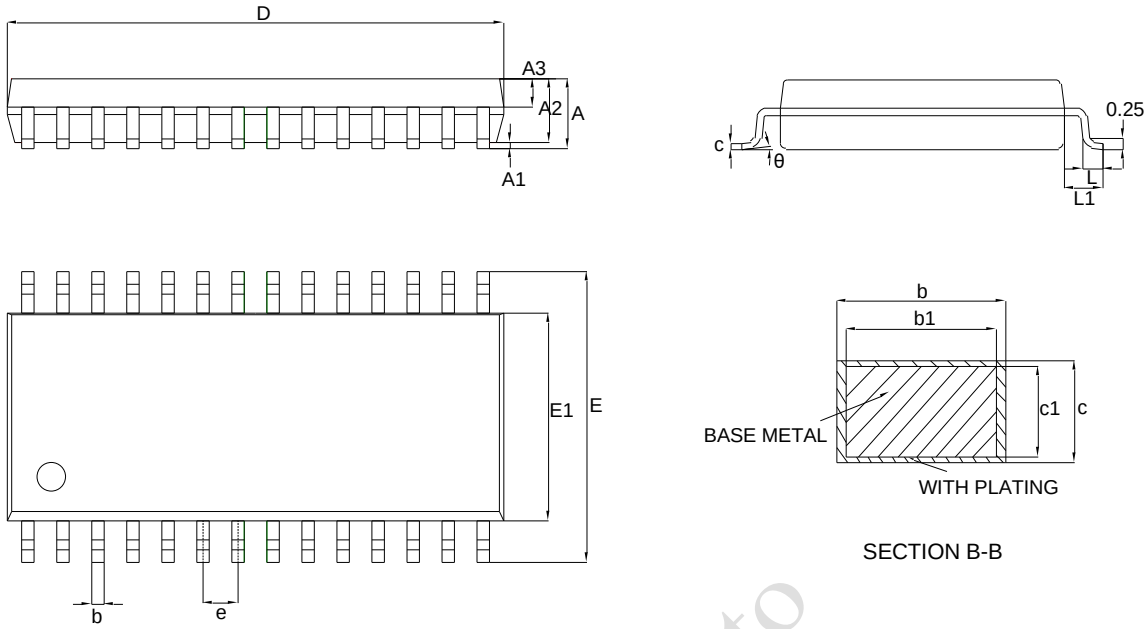



Fig 26. $R_{RCIN,ON}$ vs. temperature

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# Package Information

## Package Information SOP28




| Size / Symbol | Min. (mm) | Typ. (mm) | Max. (mm) | Size / Symbol | Min. (mm) | Typ. (mm) | Max. (mm) |
|---|---|---|---|---|---|---|---|
| A | - | - | 2.65 | D | 17.90 | 18.00 | 18.10 |
| A1 | 0.10 | - | 0.30 | E | 10.10 | 10.30 | 10.50 |
| A2 | 2.25 | 2.30 | 2.35 | E1 | 7.40 | 7.50 | 7.60 |
| A3 | 0.97 | 1.02 | 1.07 | e | 1.27BSC | | |
| b | 0.39 | - | 0.47 | L | 0.70 | - | 1.00 |
| b1 | 0.38 | 0.41 | 0.44 | L1 | 1.40REF | | |
| c | 0.25 | - | 0.29 | θ | 0 | - | 8° |
| c1 | 0.24 | 0.25 | 0.26 | | | | |

| Top mark | Package |
|---|---|
| PN<br>PN7335<br>YWWXXXXX | SOP28 |

Note：Y：Year Code； WW：Week Code；XXXXX：Internal Code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

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## Important Notice

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