High Side & Low Side Gate Driver

General description

The PN7114 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. The floating channel can be used to drive an N-channel power MOSFET in the high side configuration which operates up to 600V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

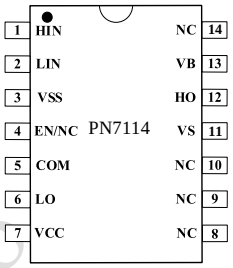
Application

- Power Supplies for Telecom and Datacom
- Half-Bridge and Full-Bridge Converters
- Motor Controls
- Lighting Ballast

Features

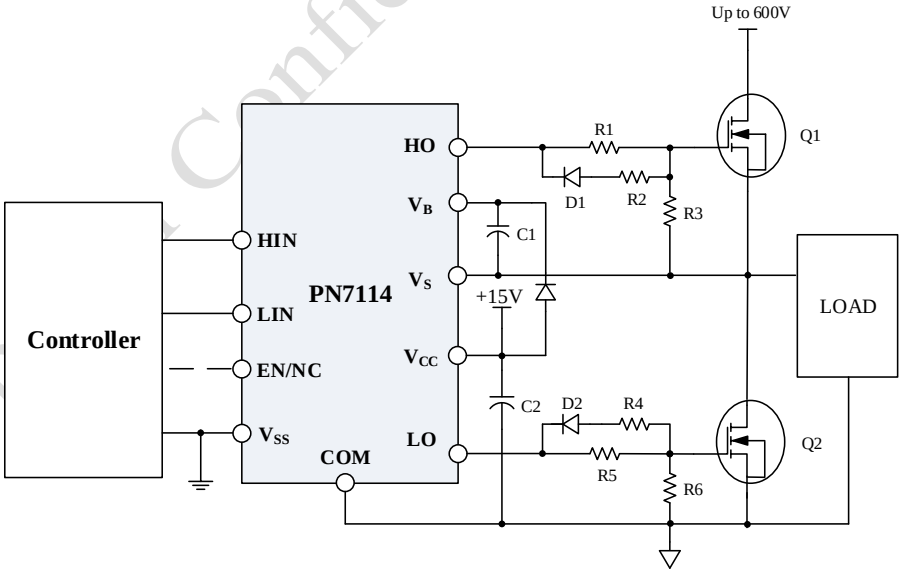
- Fully operational to +600V
- 3.3V and 5V logic compatible
- Floating channel designed for bootstrap operation
- Gate drive supply range from 10V to 20V
- UVLO for both channels
- 2.5A (Typ.) Sink, 2.5A (Typ.) Source output current capability
- Optional enable function
- Matched propagation delay for both channels

Package/Order Information



Order code	Package
PN7114SK-A1	SOP14
PN7114ASK-A1	SOP14

Schematic Diagram of Typical Application

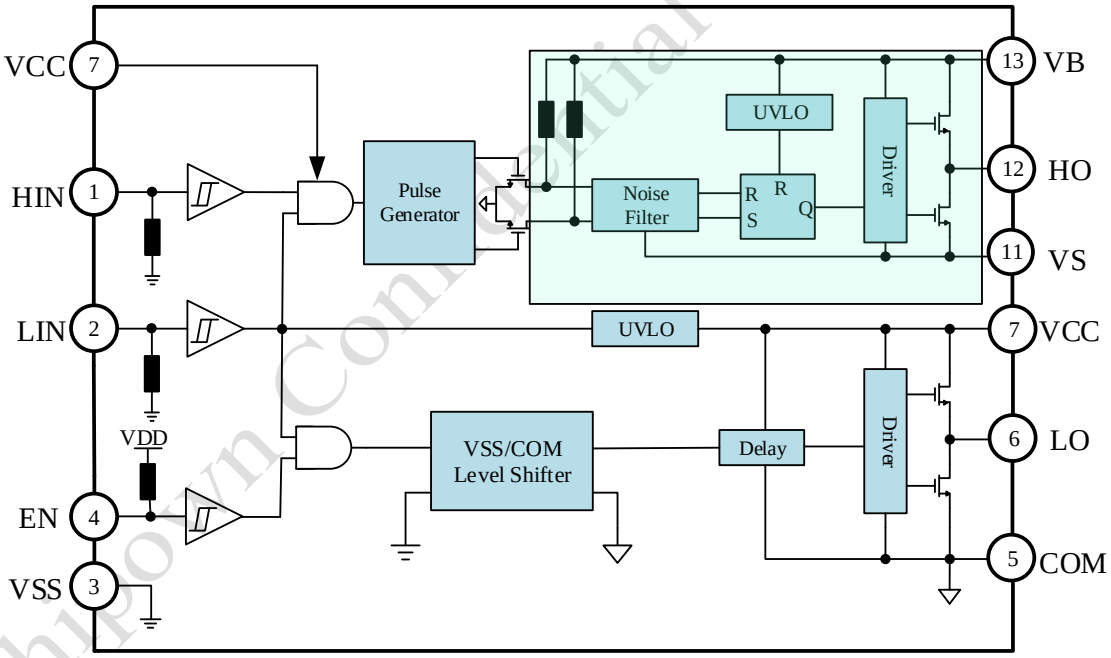


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Pin Definitions

Pin Name	Pin Number	Pin Function Description
HIN	1	Logic input for high side gate drive output (HO), in phase
LIN	2	Logic input for low side gate drive output (LO), in phase
VSS	3	Ground
EN/NC	4	PN7114A: Enable input for high side and low side drive. This pin biased LOW, logic input for high side and low side drive shutdown, This pin biased HIGH or floating enanles high side and low side drive. PN7114: This pin no connection.
COM	5	Low side return
LO	6	Low side gate drive output, in phase with LIN
VCC	7	Low side supply
NC	8,9,10,14	No connection
VS	11	High side floating supply return
HO	12	High side gate drive output, in phase with HIN
VB	13	High side floating supply

Block Diagram



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Absolute Maximum Ratings (1)

All voltages are referenced to COM, unless otherwise specified.

Symbol	Definition	MIN.	MAX.	Units
V_B(2)(5)	High side floating supply	-0.3	625	V
V_S(2)	High side floating supply return	V_B - 25	V_B + 0.3	
V_{HO}(2)	High side gate drive output	V_S -0.3	V_B + 0.3	
V_{CC}(2)(5)	Low side supply	-0.3	25	
V_{LO}(2)	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}(2)	Logic input	-0.3	V_{CC} + 0.3	
VSS	Logic ground	-5	5	
dV_S/dt(5)	Allowable offset supply voltage transient	-	50	V/ns
ESD(3)	HBM Model	2	-	kV
	CDM Model	1000	-	V
T_J	Junction Temperature	-	150	℃
T_S	Storage Temperature	-55	150	

Note:
(1) Stresses outside the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to the Absolute Maximum Ratings for extended periods may affect device reliability.
(2) All of these pins can withstand -1V @ repetitive pulse less than 20μs (duty less than 1%) and ±200mA less than 10ms without damage. V_S pin can withstand -19V @ repetitive pulse less than 10ns (duty less than 1%). VHO and VLO pins can withstand -3V @ repetitive pulse less than 10ns (duty less than 1%).
(3) This device series incorporates ESD protection and is tested by the following methods:
ESD Human Body Model tested per ANSI/ESDA/JEDEC JS-001-2017.
ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS-002-2018.
(4) VCC/VBS ports contain clamping diode, the clamping voltage ensured by design.
(5) Ensured by design.

Recommended Operating Conditions

All voltages are referenced to COM unless otherwise specified.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply	V_S +10	V_S +20	V
V_S	High side floating supply return	-5	600	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	10	20	
V_{LO}	Low side gate drive output voltage	COM	V_{CC}	
V_{IN}	Logic input voltage(HIN & LIN& EN)	VSS	V_{CC}	
T_A	Ambient temperature	-40	125	℃

Thermal Information

Symbol	Definition	TPY.	Units
θ_{JA}(1)	Junction to ambient thermal resistance	120	℃/W

Note:
(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

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Dynamic Electrical Characteristics

(T_J=25 ℃, V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000pF, f=100kHz, Duty cycle = 50%, LIN/HIN=0 to 3.3V (slew rate =1V/ns), all voltages are referenced to COM (except V_{BS} referenced to V_S) unless otherwise specified.)

Symbol	Definition	Test Conditions	MIN.	TYP.	MAX.	Units
t_{on}	Turn-on propagation delay	VS=0V(DC)	-	135	320	ns
t_{off}	Turn-off propagation delay	VS=600V(DC)	-	130	300	
MT(1)	Delay matching		-	-	30	
t_r	Turn-on rise time	Output 10% to 90%	-	20	35	
t_f	Turn-off fall time	Output 90% to 10%	-	15	28	
t_{EN}	Enable low to output shutdown propagation delay		-	145	200	

Note:
(1) MT Definition: $|t_{on_HO} - t_{on_LO}|$ or $|t_{off_HO} - t_{off_LO}|$.
(2) The parameter values are obtained under the corresponding test conditions mentioned.

Static Electrical Characteristics

(T_J=25 ℃, V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF, all voltages are referenced to COM (except V_{BS} referenced to V_S) unless otherwise specified. Typical values are at 25 ℃)

Symbol	Definition	MIN.	TYP.	MAX.	Units
V_{IH}	Logic “1”(HIN& LIN&EN) input voltage	2.8	-	-	V
V_{IL}	Logic “0” (HIN & LIN&EN) input voltage	-	-	1.0	
V_{OH}	High level output voltage, V_{BIAS} – V_O at I_O=2mA	-	-	2.5	
V_{OL}	Low level output voltage, I_O=2mA	-	-	0.15	
I_{QCC}	Quiescent V_{CC} supply current, V_{IH}=V_{IL}=0V	-	140	200	μA
I_{QBS}	Quiescent V_B supply current, V_{IH}=V_{IL}=0V	-	90	150	
I_{LK}	Leakage current from V_B to GND, V_B=600V	-	-	25	
I_{IN+}	Logic “1” input bias current, V_{IH}=V_{IL}=5V	-	25	50	μA
I_{IN-}	Logic “0” input bias current, V_{IH}=V_{IL}=0V	-	-	5	
I_{EN+}	Logic “1” input bias current, V_{EN} =5V	-	-	5	
I_{EN-}	Logic “0” input bias current, V_{EN} =0V	-50	-25	-	
V_{BSU+}	V_{BS} supply UVLO threshold	7	8.7	9.7	V
V_{BSU-}		6.6	8.3	9.4	
V_{CCU+}	V_{CC} supply UVLO threshold	7.2	8.6	9.7	
V_{CCU-}		6.8	8.2	9.5	
I_{O+}(1)	Output high short circuit pulsed current	2.0	2.5	-	A
I_{O-}(1)	Output low short circuit pulsed current	2.0	2.5	-	

Note:
(1) Ensured by design.
(2) The parameter values are obtained under the corresponding test conditions mentioned.

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Function Timing Diagram

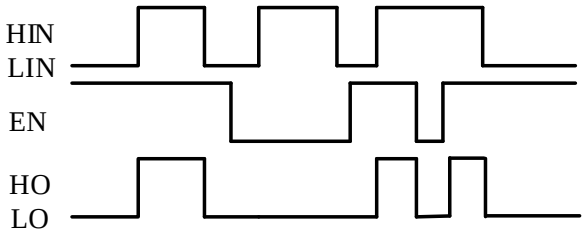


Fig.1 Input and output logic

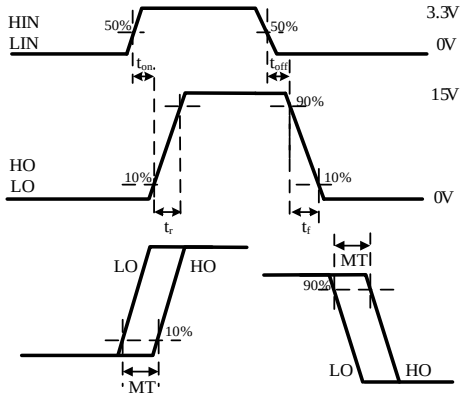
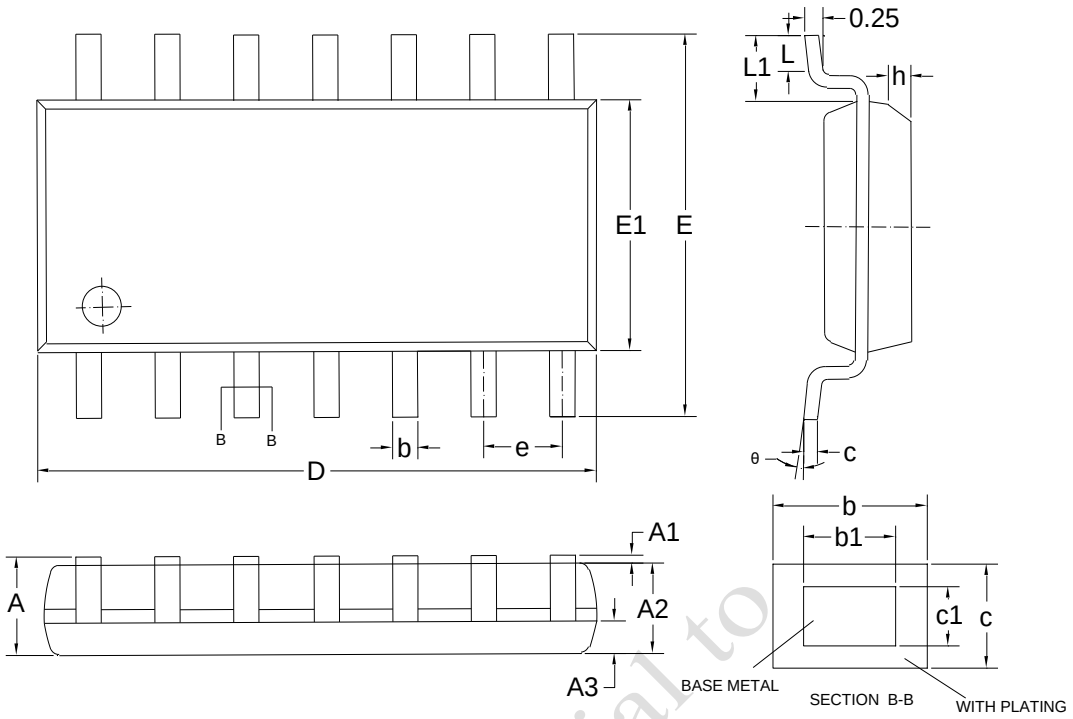


Fig.2 Propagation Delay, Rise Time, Fall Time Timing and Delay Matching

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Package Information

Package Information SOP14



Size / Symbol	Min. (mm)	Typ. (mm)	Max. (mm)	Size / Symbol	Min. (mm)	Typ. (mm)	Max. (mm)
A	—	—	1.75	D	8.55	8.65	8.75
A1	0.10	—	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.80	3.90	4.00
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	—	0.47	h	0.25	—	0.50
b1	0.38	0.41	0.44	L	0.50	—	0.80
c	0.20	—	0.24	L1	1.05REF		
c1	0.19	0.20	0.21	θ	0	—	8 °

Top mark	Package
PN PN7114 YWWXXXXX	SOP14
PN PN7114A YWWXXXXX	SOP14

Note: Y: Year Code; WW: Week Code; XXXXX: Internal Code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

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