High Side & Low Side Gate Driver

General description

The PN7113 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. The floating channel can be used to drive an N-channel power MOSFET in the high side configuration which operates up to 600V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

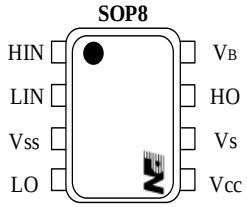
Application

- Power supplies for Telecom and Datacom
- Half-Bridge and Full-Bridge Converters
- Motor Controls
- Lighting ballast

Features

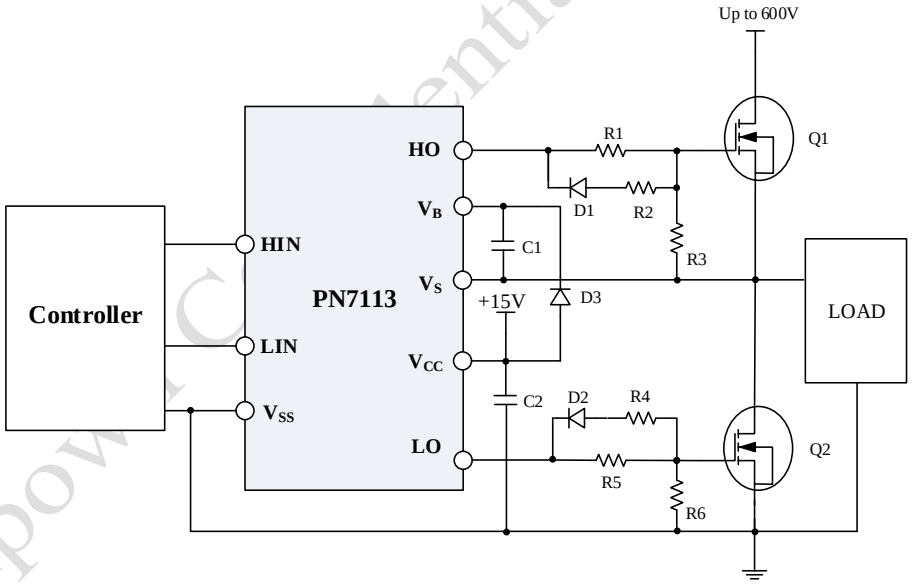
- Fully operational to +600V
- 3.3V and 5V logic compatible
- Floating channel designed for bootstrap operation
- Gate drive supply range from 10V to 20V
- UVLO for both channels
- 2.5A (typ.) Output Current Capability
- Matched propagation delay for both channels

Package/Order Information



Order code	Package
PN7113SE-A1	SOP8

Typical Application

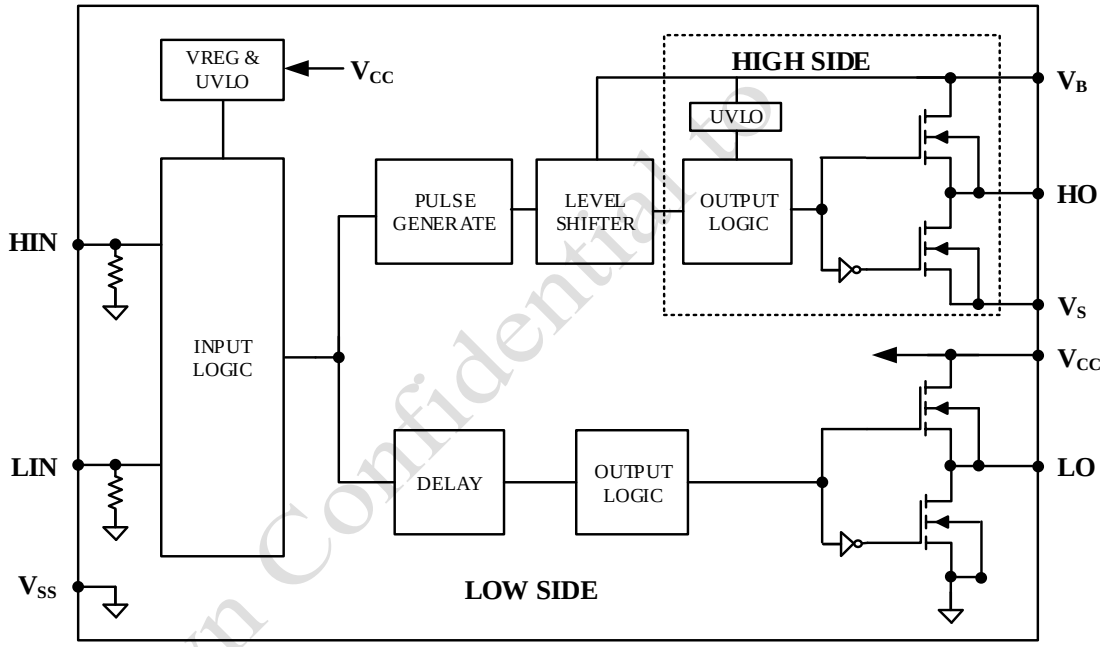


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Pin Definitions

Pin Name	Pin Number	Pin Function Description
HIN	1	Logic input for high side gate drive output (HO)
LIN	2	Logic input for low side gate drive output (LO)
V_{SS}	3	Ground
LO	4	Low side gate drive output, in phase with LIN
V_{CC}	5	Low side supply
V_S	6	High side floating supply return
HO	7	High side gate drive output, in phase with HIN
V_B	8	High side floating supply

Block Diagram



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Absolute Maximum Ratings(1)

T_A =25 ℃, all voltages are referenced to VSS unless otherwise specified.

Symbol	Definition	MIN.	MAX.	Units
V_B(2)	High side floating supply	-0.3	625.0	V
V_S(2)(4)	High side floating supply return	V_B – 25.0	V_B + 0.3	
V_{HO}(2)	High side gate drive output	V_S -0.3	V_B + 0.3	
V_{CC}(2)(4)	Low side supply	-0.3	25.0	
V_{LO}(2)	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}(2)	Logic input	-0.3	V_{CC} + 0.3	
dV_S/dt(5)	Allowable Offset Supply Voltage Transient	-	50.0	V/ns
ESD(3)	HBM Model	2.0	-	kV
	CDM Model	500.0	-	V
P_D	Package Power Dissipation @ T_A ≤25°C	-	1.25	W
R_{thJA}	Thermal Resistance Junction to Ambient	-	120	℃ /W
T_J	Junction Temperature	-	150	℃
T_S	Storage Temperature	-55	150	

Note:

1. Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

2. All of these pins can withstand -1V @ repetitive pulse less than 20us and ±200mA less than 10ms without damage. V_S pin can withstand -19V @ repetitive pulse less than 10ns. VHO and VLO pins can withstand -3V @ repetitive pulse less than 10ns.

3. This device series incorporates ESD protection and is tested by the following methods:
ESD Human Body Model tested per ANSI/ESDA/JEDEC JS-001-2017 (EIA/JESD22−A114)
ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS-001-2018 (EIA/JESD22−C101E)

4. VCC/VBS ports contain catching diode, the clamp voltage Ensure by design.

5. Ensure by design.

Recommended Operating Conditions

All voltages are referenced to VSS unless otherwise specified.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply	V_S +10	V_S +20	V
V_S	High side floating supply return	-8	600	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	10	20	
V_{LO}	Low side gate drive output voltage	GND	V_{CC}	
V_{IN}	Logic input voltage(HIN & LIN)	GND	V_{CC}	
T_A	Ambient temperature	-40	125	℃

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Dynamic Electrical Characteristics

(-40 ℃≤T_J≤125 ℃, V_{BIAS} (VCC, VBS) = 15V, C_L = 1000 pF, f=100kHz, Duty cylce = 50%,LIN/HIN=0 to 3.3V (slew rate =1V/ns), all voltages are referenced to VSS unless otherwise specified. Typical values are at 25 ℃)

Symbol	Definition	Test Conditions	MIN.	TYP.	MAX.	Units
t_{on}	Turn-on propagation delay	VS=0V(DC)	-	135	317	ns
t_{off}	Turn-off propagation delay	VS=600V(DC)	-	130	294	
MT(2)	Delay matching		-	-	30	
t_r	Turn-on rise time	Output 10% to 90%	-	20	33	
t_f	Turn-off fall time	Output 90% to 10%	-	15	28	

Note:
1. HIN/LIN logic level is 3.3V.
2. MT Definition:
Turn-on propagation delay (HO) minus Turn-on propagation delay (LO);
Turn-off propagation delay (HO) minus Turn-off propagation delay (LO);
3. The parameter values are obtained under the corresponding test conditions mentioned.

Static Electrical Characteristics

(-40 ℃≤T_A≤125 ℃, V_{BIAS} (VCC, VBS) = 15V, C_L = 1000 pF, all voltages are referenced to VSS unless otherwise specified. Typical values are at 25 ℃)

Symbol	Definition	Test Conditions	MIN.	TYP.	MAX.	Units
V_{IH}	Logic “1”(HIN& LIN) input voltage		2.7	-	-	V
V_{IL}	Logic “0” (HIN & LIN) input voltage		-	-	0.5	
V_{OH}	High level output voltage, V_{BIAS} – V_O	I_O=20mA	-	-	3	
V_{OL}	Low level output voltage,	I_O=20mA	-	-	0.15	
I_{QCC}	Quiescent VCC supply current	V_{HIN}=V_{LIN}=0V	-	120	253	μA
I_{QBS}	Quiescent VB supply current	V_{HIN}=V_{LIN}=0V	-	75	181	
I_{LK}	Leakage current from VB to GND	VB=600V	-	-	23	
$R_{DS(ON)}$	Drain-source on state resistance (All output MOSFETs)		0.5	1.1	2.5	Ω
I_{IN+}	Logic “1” input bias current	V_{HIN}=V_{LIN}=5V	-	25	50	μA
I_{IN-}	Logic “0” input bias current	V_{HIN}=V_{LIN}=0V	-	-	5	
V_{BSU+}	VBS supply UVLO threshold	VBS rising	6.5	8.4	9.7	V
V_{BSU-}		VBS falling	6.3	8.0	9.4	
V_{CCU+}	VCC supply UVLO threshold	VCC rising	6.9	8.4	9.7	
V_{CCU-}		VCC falling	6.5	8.0	9.5	
t_{VBSuv}	VBS supply UVLO Filter Time, VBS supply is rising		-	3	10	μs
t_{VCCuv}	VCC supply UVLO Filter Time, VCC supply is rising		-	3	10	
I_{O+}(1)	Output high short circuit pulsed current	VO=0V, VIN=VDD PW≤10μs	2.0	2.5	-	A
I_{O-}(1)	Output low short circuit pulsed current	VO=15V, VIN=0V PW≤10μs	2.0	2.5	-	

Note:
1. Ensure by design.
2. The parameter values are obtained under the corresponding test conditions mentioned.

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Truth Table

Input		Output	
HIN	**LIN**	**HO**	**LO**
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

Note:
1. Without interlocking function on “HO” and “LO” internal circuit.
2. Test Conditions: V_{BIAS} (VCC, VBS) = 15V, V_{BIAS} (HIN, LIN) = 0V/3.3V.

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Function Timing Diagram

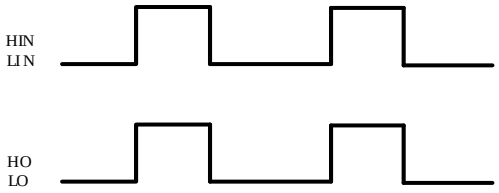


Fig.1 Input and output logic

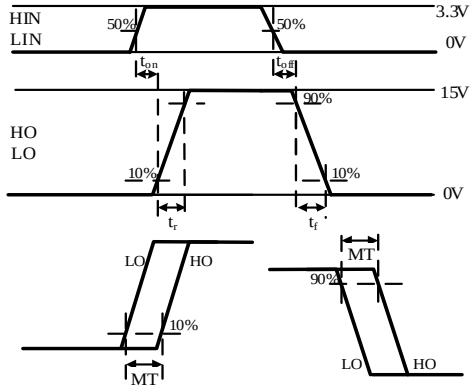
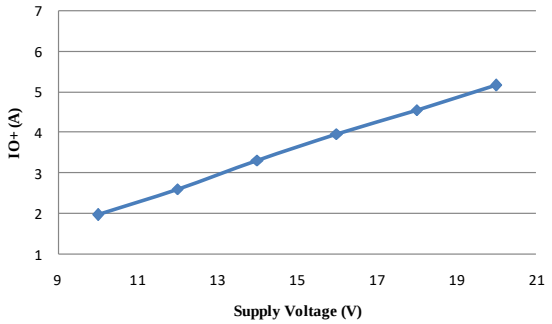
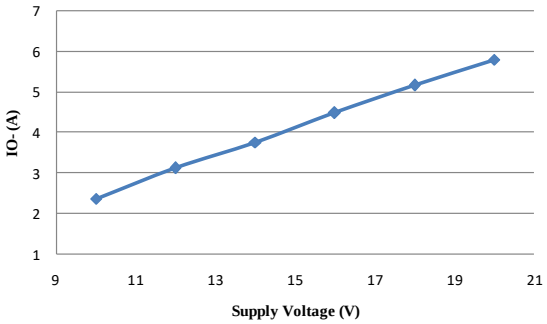


Fig.2 Propagation Delay, Rise Time, Fall Time Timing and Delay Matching

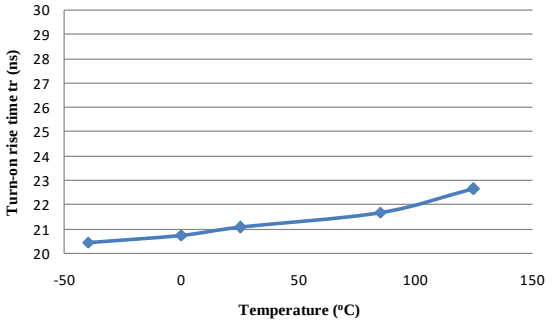


(a) Output high short circuit pulsed current

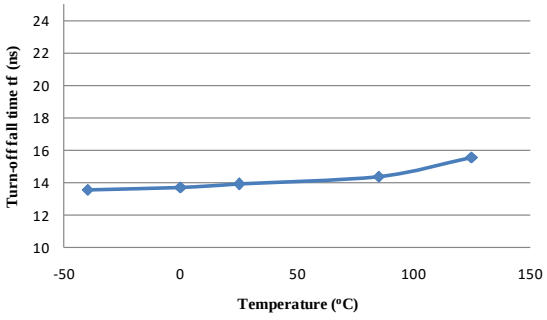


(b) Output low short circuit pulsed current

Fig.3 Output current vs. Supply voltage

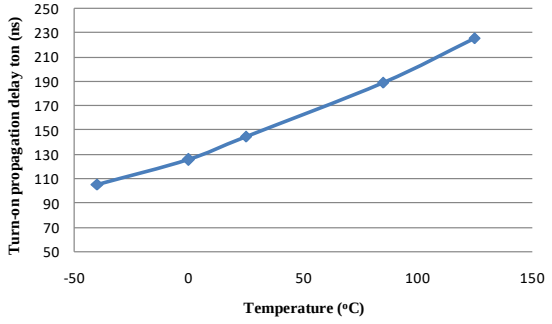


(a) Turn-on rise time

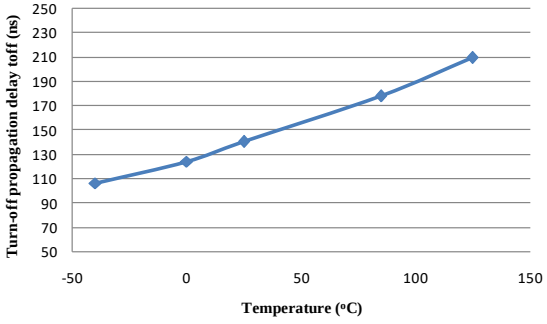


(b) Turn-off fall time

Fig.4 Turn-on rise time and turn-off fall time vs. Temperature

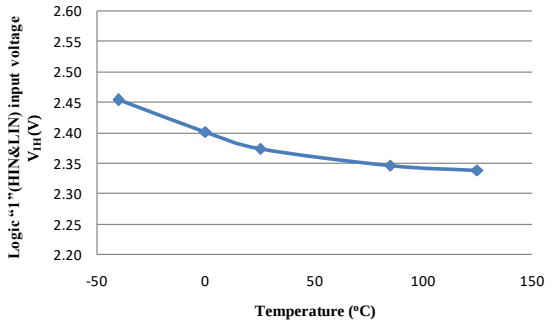


(a) Turn-on propagation delay

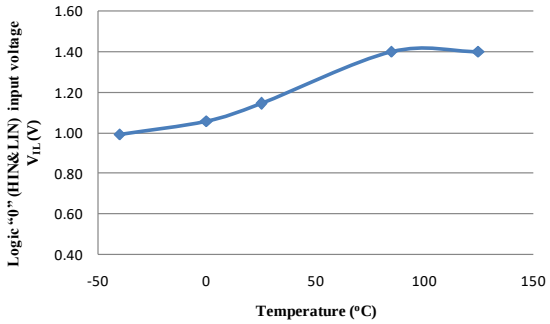


(b) Turn-off propagation delay

Fig.5 Propagation delay time vs. Temperature

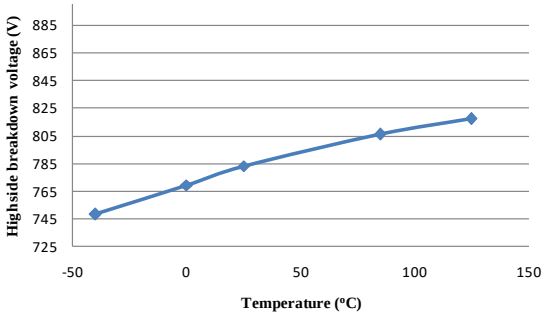


(a)Logic "1"(HIN&LIN) input voltage

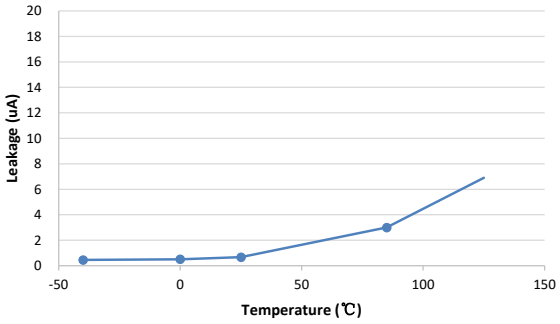


(b) Logic "0"(HIN& LIN) input voltage

Fig.6 Input threshold voltage vs. Temperature

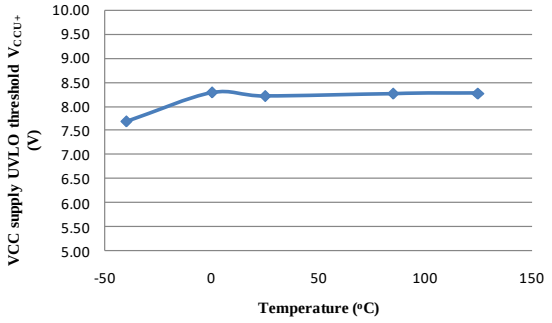


(a) Breakdown voltage

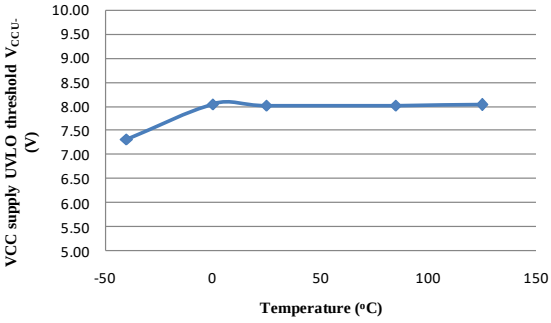


(b) Leakage

Fig.7 High side breakdown voltage and leakage vs. Temperature

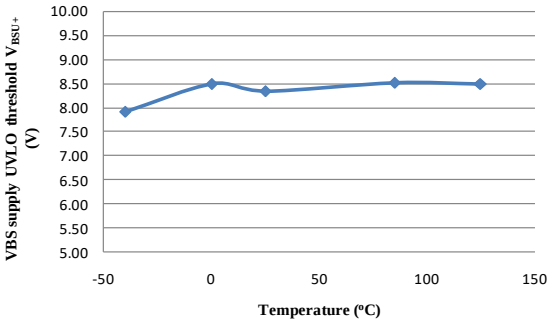


(a) VCC supply UVLO threshold VCCU+

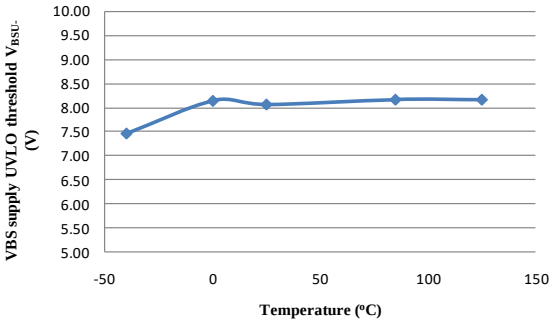


(b) VCC supply UVLO threshold VCCU-

Fig.8 VCC supply UVLO threshold vs. Temperature

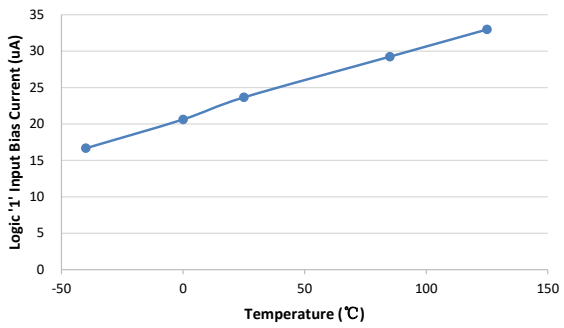


(a) VBS supply UVLO threshold VBSU+

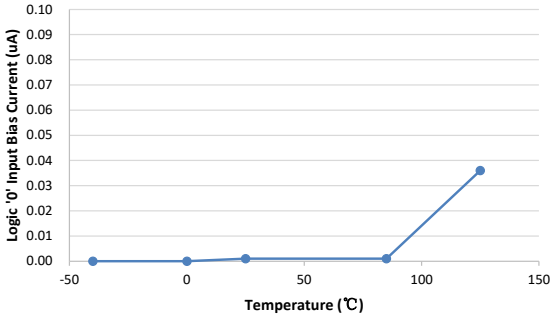


(b) VBS supply UVLO threshold VBSU-

Fig.9 VBS supply UVLO threshold vs. Temperature

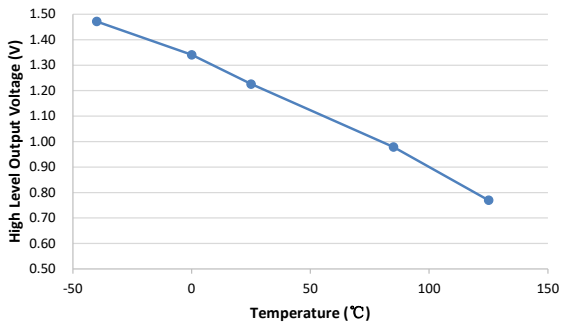


(a) Logic "1" input bias current

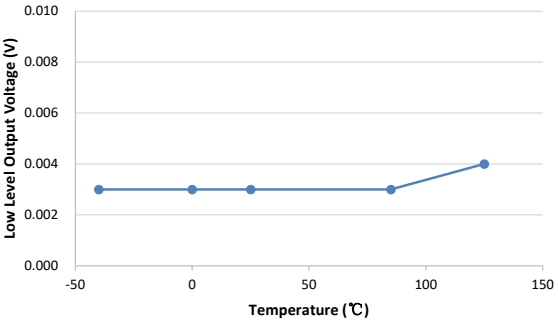


(b) Logic "0" input bias current

Fig.10 Input bias current vs. Temperature

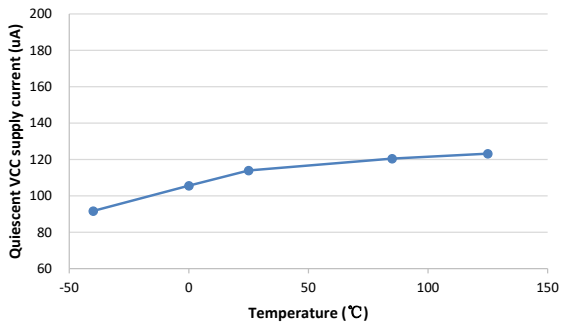


(a) High level output voltage

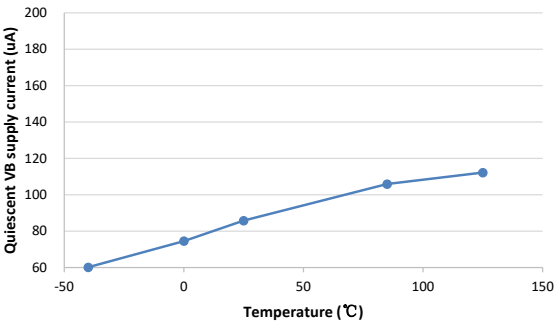


(b) Low level output voltage

Fig.11 V_{OH} and V_{OL} vs. Temperature



(a) Quiescent VCC supply current



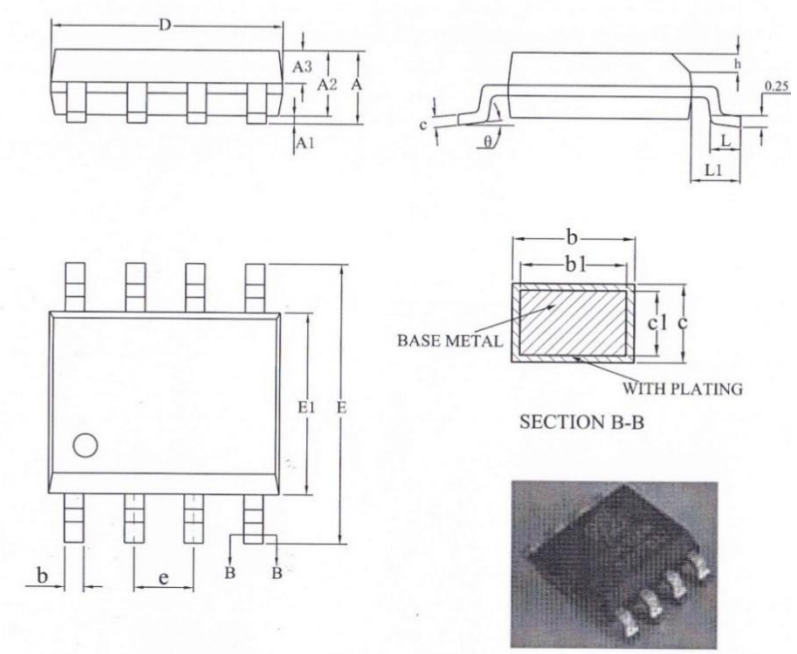
(b) Quiescent VB supply current

Fig.12 Quiescent supply current vs. Temperature

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Package Information

Package Information SOP8



Size / Symbol	Min. (mm)	Typ. (mm)	Max. (mm)	Size / Symbol	Min. (mm)	Typ. (mm)	Max. (mm)
A	—	—	1.75	D	4.80	4.90	5.00
A1	0.10	—	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.80	3.90	4.00
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	—	0.47	h	0.25	—	0.50
b1	0.38	0.41	0.44	L	0.50	—	0.80
c	0.20	—	0.24	L1	1.05REF		
c1	0.19	0.20	0.21	θ	0	—	8°

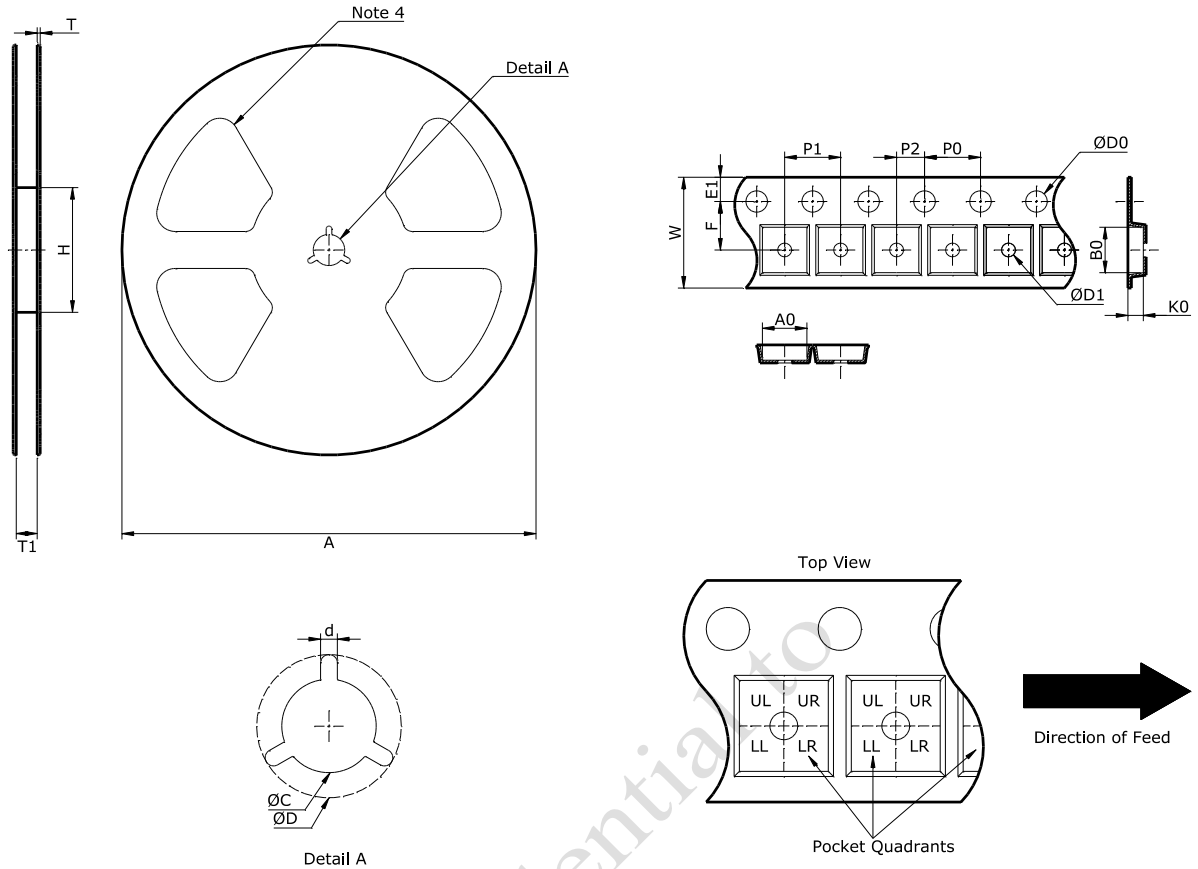
Top mark	Package
PN PN7113 YWWXXXXX	SOP8

Note：Y：Year Code；WW：Week Code；XXXXX：Internal Code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

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Tape and Reel Information



SOP8 Package									
A (mm)	**T (mm)**	**T1 (mm)**	**H (mm)**	**ØC (mm)**	**ØD (mm)**	**d (mm)**	**A0 (mm)**	**B0 (mm)**	**K0 (mm)**
330 ±1.0	3 +1/-0	12.4 +1/-0	100 ±0.5	12.00 +0.5/-0.2	17.70 ±0.40	2.00 +0.5/-0.2	6.60 ±0.1	5.3 ±0.1	1.9 ±0.1
W (mm)	**F (mm)**	**E1 (mm)**	**P0 (mm)**	**P1 (mm)**	**P2 (mm)**	**ØD0 (mm)**	**ØD1 (mm)**	**Pin 1 Quadrant**	
12.00 ±0.1	5.50 ±0.1	1.75 ±0.10	4.00 ±0.10	8.0 ±0.1	2.0 ±0.1	1.5 +0.1/-0	1.55 ±0.05	UL	

Notes:
1. This drawing is subjected to change without notice.
2. All dimensions are nominal and in mm.
3. This drawing is not in scale and for reference only.
4. The number of flange openings depends on the reel size and assembly site. This drawing shows an example only.

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