High Side & Low Side Gate Driver IC

General Description

The PN7011 is a high voltage, high speed driver with independent high and low side referenced output channels. The floating channel can be used to drive a power switch in the high side configuration which operates up to 150V. This device offers several significant performances, peak output pull-up and pull-down current has been increased to 4A source and 4A sink, and thereby allows for driving large power MOSFETs with minimized switching losses during the transition through the miller plateau of the MOSFET. The input structure can directly handle -10VDC, which increases robustness and also allows direct interface to gate-drive transformers without using rectification diodes. The inputs are also independent of supply voltage and have a 18V maximum rating. Propagation delays are matched to simplify use in high frequency applications.

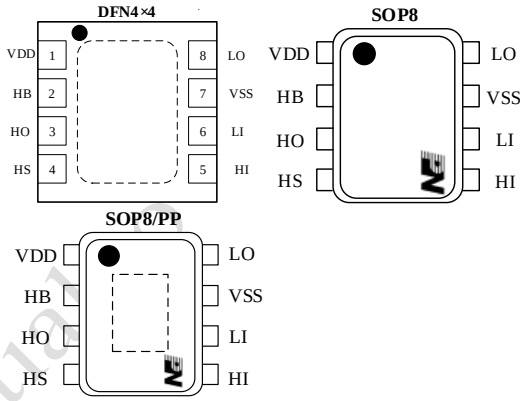
Application

- Power supplies for Telecom, Datacom, and Merchant Battery Charger
- Half-bridge and Full-bridge converters
- Push-pull converters
- High voltage synchronous-Buck converters
- Active-clamp forward converters

Features

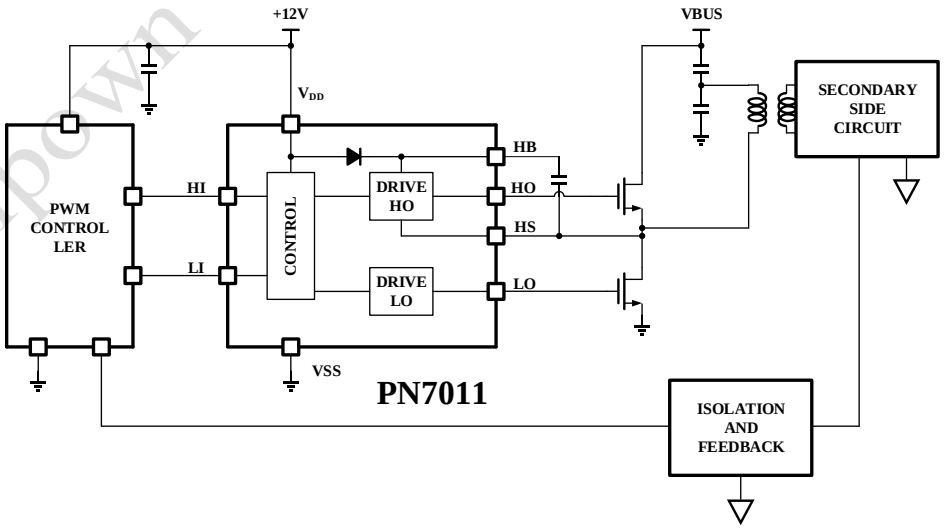
- Fully operational to +150V DC
- Drives two N-channel MOSFETs in High-side and Low-side configuration with independent inputs
- Input pins can tolerate -10V to 18V and are independent of supply voltage range
- Floating channel designed for bootstrap operation
- Gate drive supply range from 9V to 17V
- UVLO for both channels
- 4A Sink, 4A source output current capability
- Matched propagation delay for both channels

Package/Order Information



Order code	Package
PN7011DF-A1	DFN4×4
PN7011SE-A1	SOP8
PN7011SP-A1	SOP8/PP

Typical Circuit

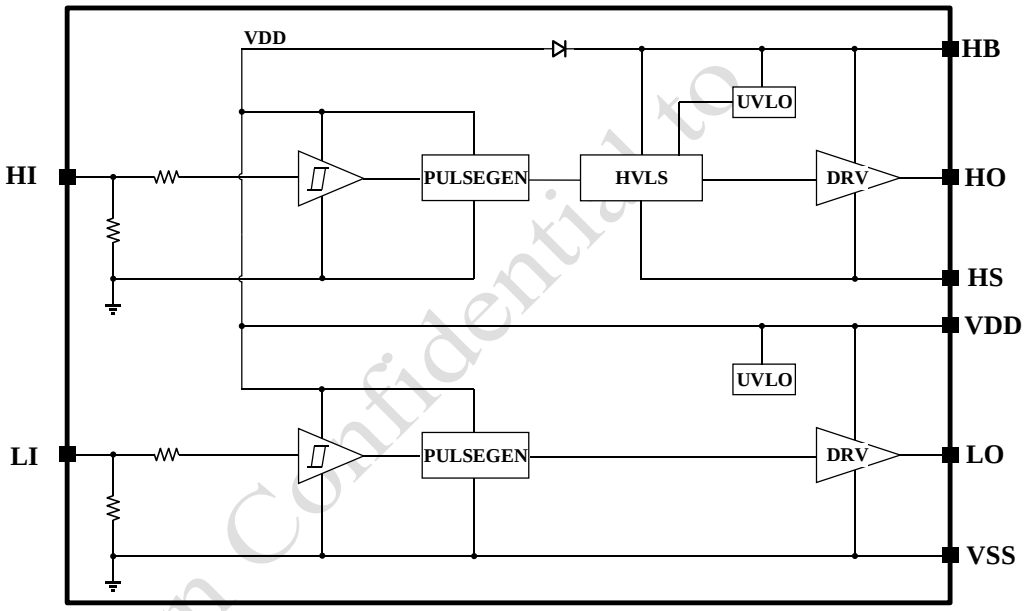


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Pin Definitions

Pin Name	Pin Number	Pin Function Description
VDD	1	Positive supply to lower-gate driver
HB	2	High side bootstrap supply
HO	3	High side gate drive output, in phase with HIN
HS	4	High side floating supply return
HI	5	Logic input for high side gate driver output (HO), in phase
LI	6	Logic input for low side gate driver output (LO), in phase
VSS	7	Negative supply terminal for the device that is generally grounded
LO	8	Low side gate drive output, in phase with LIN

Block Diagram



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Absolute Maximum Ratings

Exceeding these ratings may damage the device.
The absolute maximum ratings are stress ratings only at T_A=25 ℃, unless otherwise specified.

Symbol	Definition	MIN.	MAX.	Units
V_{HB}	Voltage on HB	-0.3(1)	160	V
V_{HS}	Voltage on HS (DC)	-1	150	
	Voltage on HS (Repetitive pulse < 100ns)	- (24-VDD)	150	
VDD	Supply voltage range	-0.3(1)	18	
V_{BS}	Supply voltage range between HB and HS	-0.3(1)	18	
V_{HO}	High side gate drive output(DC)	-0.3	V_{HB} + 0.3	
	High side gate drive output (Repetitive pulse < 100ns)	V_{HS}-2	V_{HB} + 0.3	
V_{LO}	Low side gate drive output(DC)	-0.3	VDD + 0.3	
	Low side gate drive output (Repetitive pulse < 100ns)	-2	VDD	
V_{IN}	Input voltage on LI and HI(DC)	-10	18	
dV_S/dt	Allowable Offset Supply Voltage Transient	-	50	V/ns
ESD	HBM Model	2	-	kV
	CDM Model	1	-	
T_J	Junction Temperature	-40	150	℃
T_S	Storage Temperature	-65	150	

Note:
1. -1V @ repetitive pulse less than 20us, less than-1V @ the absolute value of the current flowing into the chip pin is not greater than 100mA;
2. The chip pins can withstand ±200mA/10ms without damage.

Recommended Operating Conditions

Symbol	Definition	Min.	Typ.	Max.	Units
VDD	Supply voltage Range	9	12	17	V
V_{BS}	Supply voltage Range (V_{HB} - V_{HS})	9	12	17	
V_{HS}	Voltage on HS (DC)	-1	-	150	
V_{HS}	Voltage on HS (repetitive pulse < 100ns)	-(24V -VDD)	-	150	
V_{HB}	Voltage on HB	V_{HS} + 10	-	V_{HS} + 17	
V_{IN}	Logic input voltage (HIN & LIN)	0	-	VDD	
T_J	Operating junction temperature	-40	-	140	℃

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Dynamic Electrical Characteristics

(V_{BIAS} (VDD, V_{HB}) = 12V, V_{HS}=V_{SS}=0V, LO and HO with 1nF load, T_A= T_J = -40℃ to 150℃, (unless otherwise specified)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
T_{DLFF}	V_{LI} falling to V_{LO} falling	10	30	42	ns
T_{DHFF}	V_{HI} falling to V_{HO} falling	10	30	42	
T_{DLRR}	V_{LI} rising to V_{LO} rising	10	30	42	
T_{DHRR}	V_{HI} rising to V_{HO} rising	10	30	42	
T_{MON}	Delay matching From HO OFF to LO ON	-	3	10	
T_{MOFF}	Delay matching From LO OFF to HO ON	-	3	10	
T_R	LO rise time	-	7.2	-	
	HO rise time	-	7.2	-	
T_F	LO fall time	-	5.5	-	
	HO fall time	-	5.5	-	
T_{P_MIN}	Minimum input pulse width that changes the output	-	-	50	

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Static Electrical Characteristics

(V_{BIAS} (VDD, V_{HB}) = 12V, V_{HS}=V_{SS}=0V, LO and HO with 1nF load, T_A= T_J = -40℃ to 150℃, unless otherwise specified)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{HIT}	Logic “1”(HI& LI) input voltage	1.9	2.3	2.7	V
V_{LIT}	Logic “0” (HI & LI) input voltage	1.3	1.6	1.9	
V_{IHYS}	Input voltage hysteresis	-	0.7	-	
I_{IN+}	Logic “1” input bias current, IN=5V	-	65	110	μA
I_{IN-}	Logic “0” input bias current, IN=0V	-	-	5	
R_{IN}	Input pull-down resistance	-	78	-	kΩ
I_{DD}	VDD quiescent current	50	150	250	μA
I_{DDO}	VDD operating current (f = 500 kHz, C_{LOAD} = 0)	2.1	2.6	6.5	mA
I_{HB}	Boot voltage quiescent current	40	65	110	μA
I_{HBO}	Boot voltage operating current (f = 500kHz, C_{LOAD}=0)	1.5	2.5	5.1	mA
I_{LK}	Leakage current (V_{HS}=V_{HB}=150V)	-	-	1	μA
V_{HBR}	V_{HB} UVLO rising threshold	6.2	7	7.8	V
V_{HBF}	V_{HB} UVLO falling threshold	5.2	6	6.8	
V_{HBHYS}	V_{HB} UVLO threshold hysteresis	-	1	-	
VDD_R	VDD UVLO rising threshold	6.3	7.3	8.5	
VDD_F	VDD UVLO falling threshold	5.7	6.7	7.9	
VDD_{HYS}	VDD UVLO threshold hysteresis	-	0.6	-	
V_F	BSD low-current forward voltage at 100uA	-	0.65	0.8	
V_{FI}	BSD high-current forward voltage at 100 mA	-	1.1	1.95	
R_D	Dynamic resistance, ΔVF/ΔI from 100mA to 80 mA	0.6	1.5	2	Ω
V_{OH}	High level output voltage, I_{HO} = -100mA,	-	-	0.29	V
V_{OL}	Low level output voltage, I_{HO}=100mA	-	-	0.19	
I_{O+}	Output high short circuit pulsed current	-	4	-	A
I_{O-}	Output low short circuit pulsed current	-	4	-	

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Function Timing Diagram

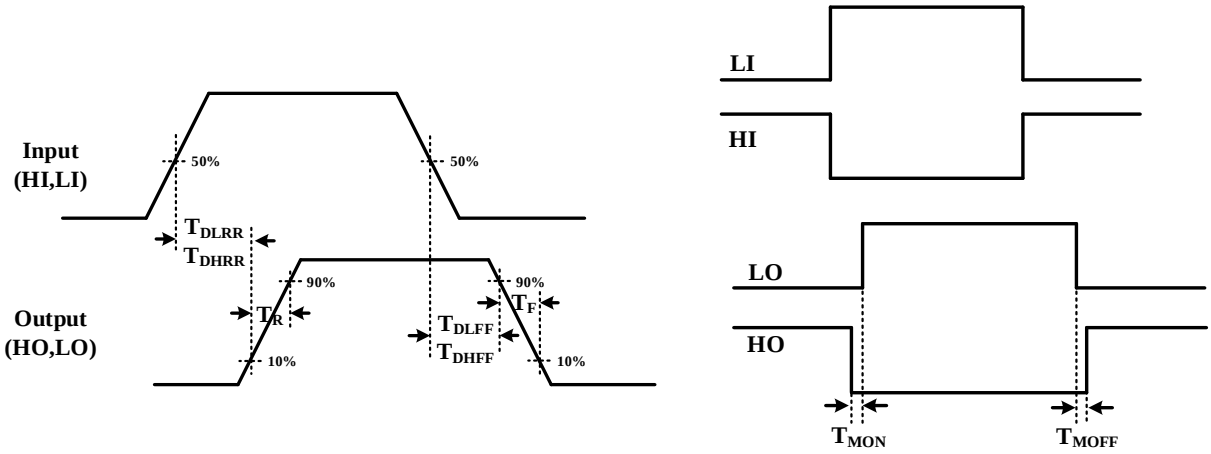


Fig.1. Dynamic timing diagram

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Characterization Curves

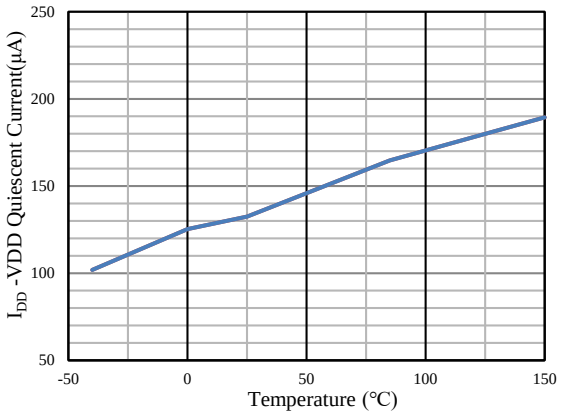


Figure 2. I_{DD} vs Temperature

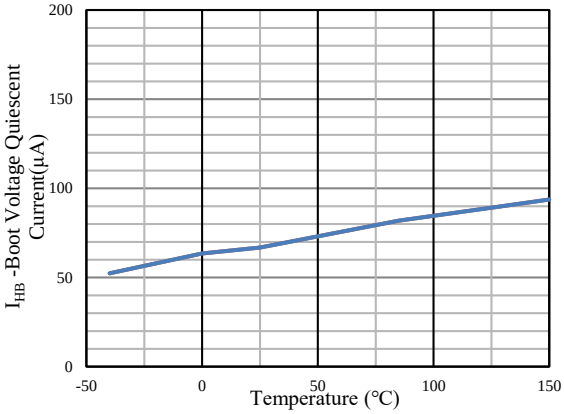


Figure 3. I_{HB} vs Temperature

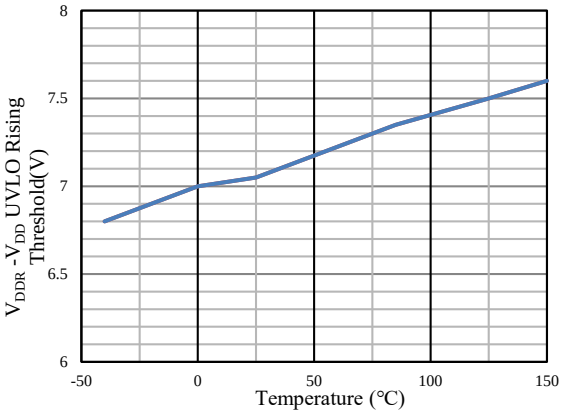


Figure 4. VDD_R vs Temperature

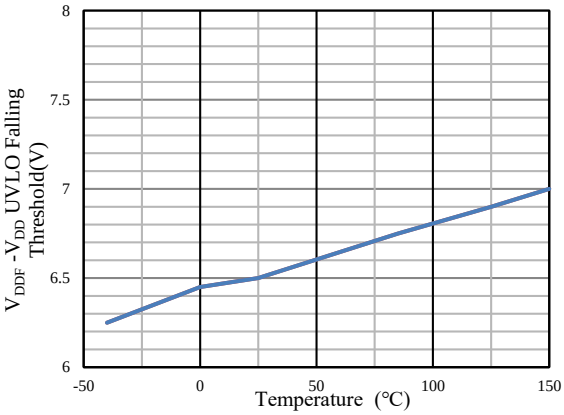


Figure 5. VDD_F vs Temperature

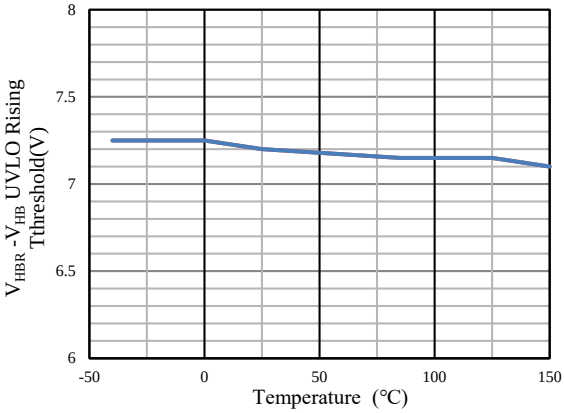


Figure 6. V_{HBR} vs Temperature

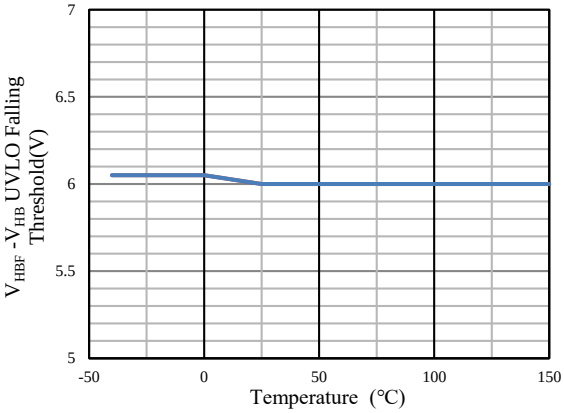


Figure 7. V_{HBF} vs Temperature

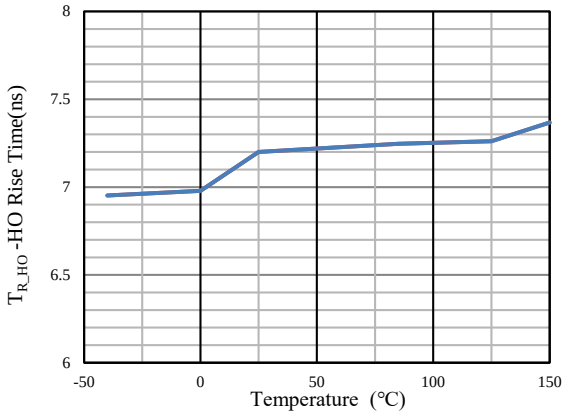


Figure 8. T_R (HO) vs Temperature

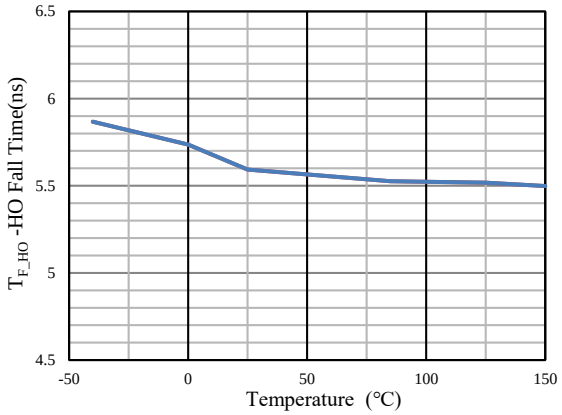


Figure 9. T_F (HO) vs Temperature

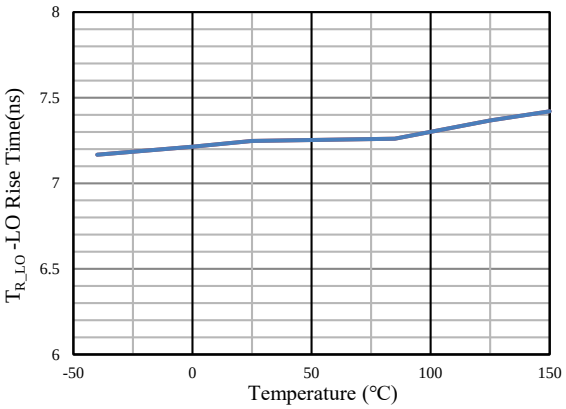


Figure 10. T_R (LO) vs Temperature

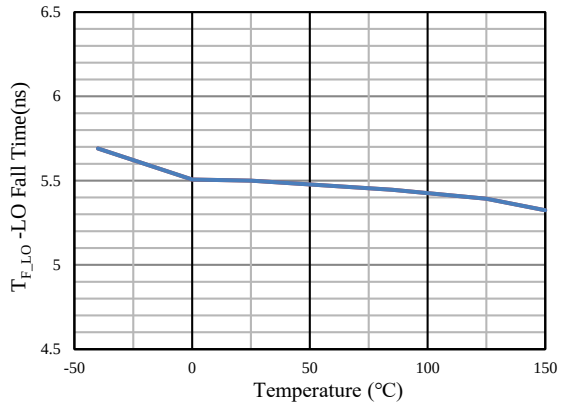


Figure 11. T_F (LO) vs Temperature

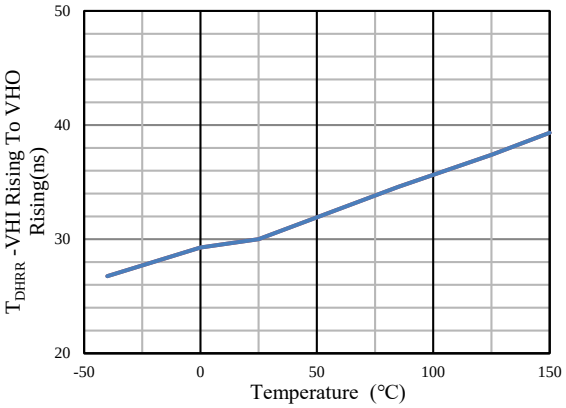


Figure 12. T_{DHRR} vs Temperature

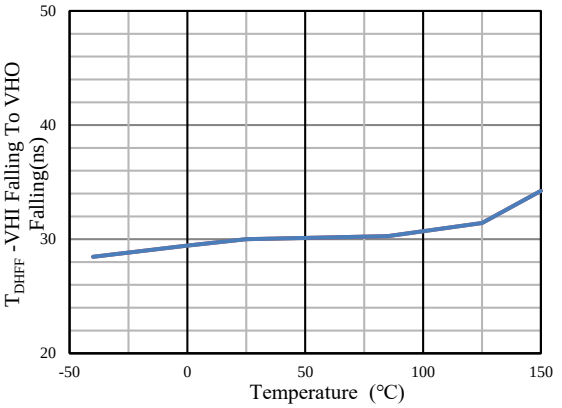


Figure 13. T_{DHFF} vs Temperature

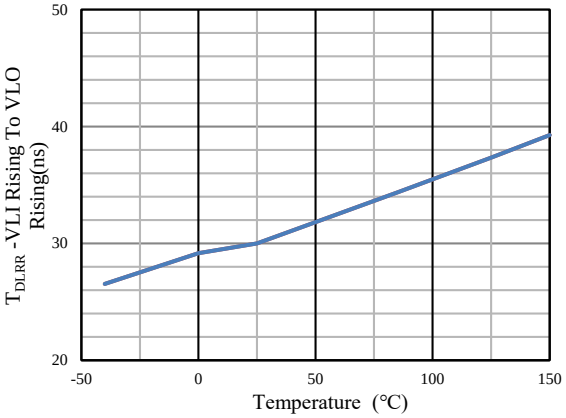


Figure 14. T_{DLRR} vs Temperature

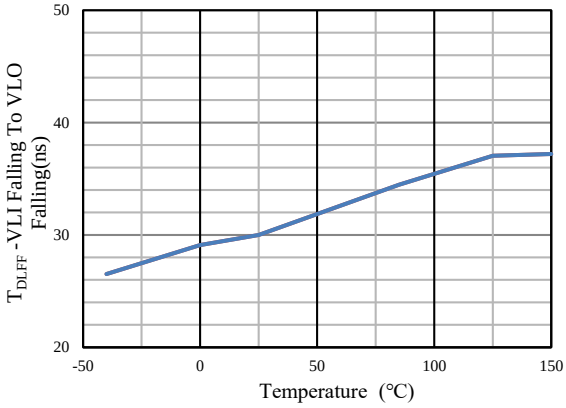


Figure 15. T_{DLFF} vs Temperature

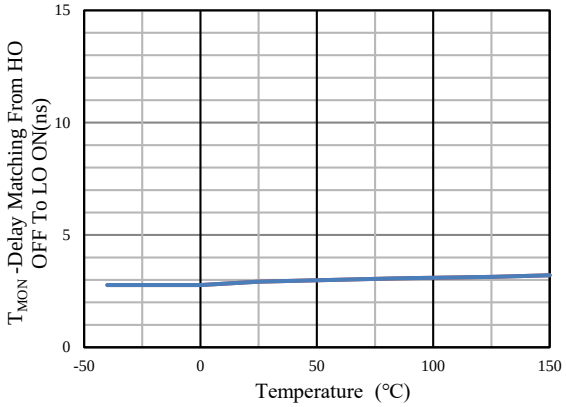


Figure 16. T_{MON} vs Temperature

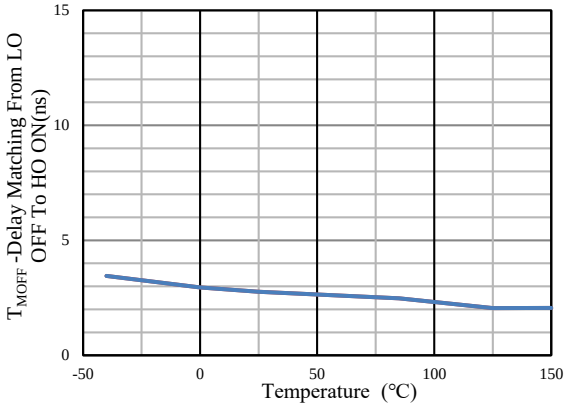
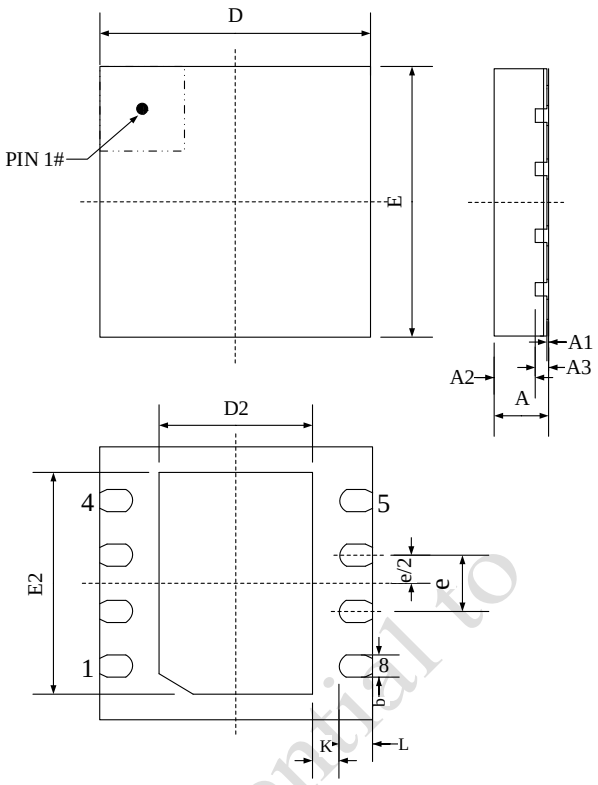


Figure 17. T_{MOFF} vs Temperature

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Package Information

Package Information DFN4×4



Size / Symbol	Min. (mm)	Typ. (mm)	Max. (mm)	Size / Symbol	Min. (mm)	Typ. (mm)	Max. (mm)
A	0.800	0.850	0.900	E	4BSC		
A1	0.000	0.020	0.050	e	0.8BSC		
A2	----	0.650	----	D2	2.300	2.400	2.500
A3	0.203REF			E2	3.300	3.400	3.500
b	0.250	0.300	0.350	L	0.300	0.400	0.500
D	4BSC			K	0.4REF		

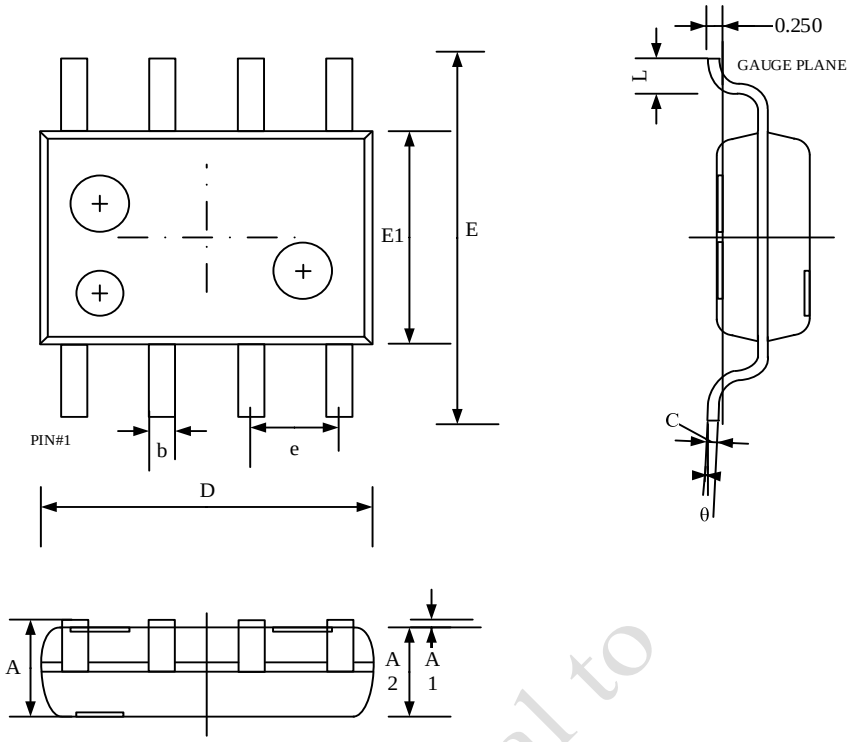
Top mark	Package
PN PN7011 YWWXXXXX	DFN4×4

Note: Y: Year Code; WW: Week Code; XXXXX: Internal Code

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Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

Package Information SOP8



Size / Symbol	Min. (mm)	Max. (mm)	Size / Symbol	Min. (mm)	Max. (mm)
A	1.300	1.750	E	5.800	6.25
A1	0.000	0.250	E1	3.750	4.150
A2	1.250	1.600	e	1.27	
b	0.306	0.510	L	0.400	1.270
c	0.150	0.250	θ	0 °	12 °
D	4.700	5.100			

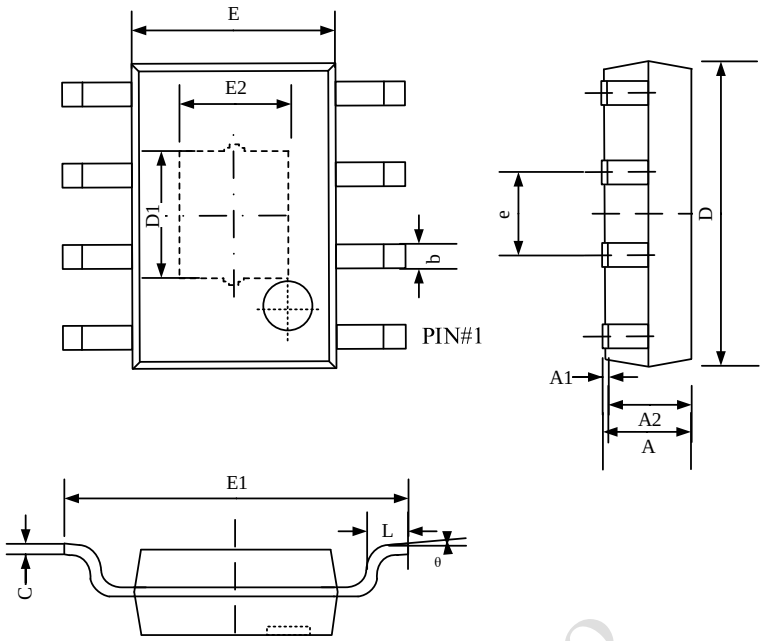
Top mark	Package
PN PN7011 YWWXXXXX	SOP8

Note：Y：Year Code；WW：Week Code；XXXXX：Internal Code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

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Package Information SOP8/PP (90×90)



Size / Symbol	Min. (mm)	Max. (mm)	Size / Symbol	Min. (mm)	Max. (mm)
A	1.300	1.750	E	3.800	4.000
A1	0.000	0.200	E1	5.800	6.200
A2	1.300	1.550	E2	2.034	2.400
b	0.306	0.510	e	1.27	
c	0.170	0.250	L	0.400	1.270
D	4.700	5.100	θ	0°	8°
D1	2.034	2.400			

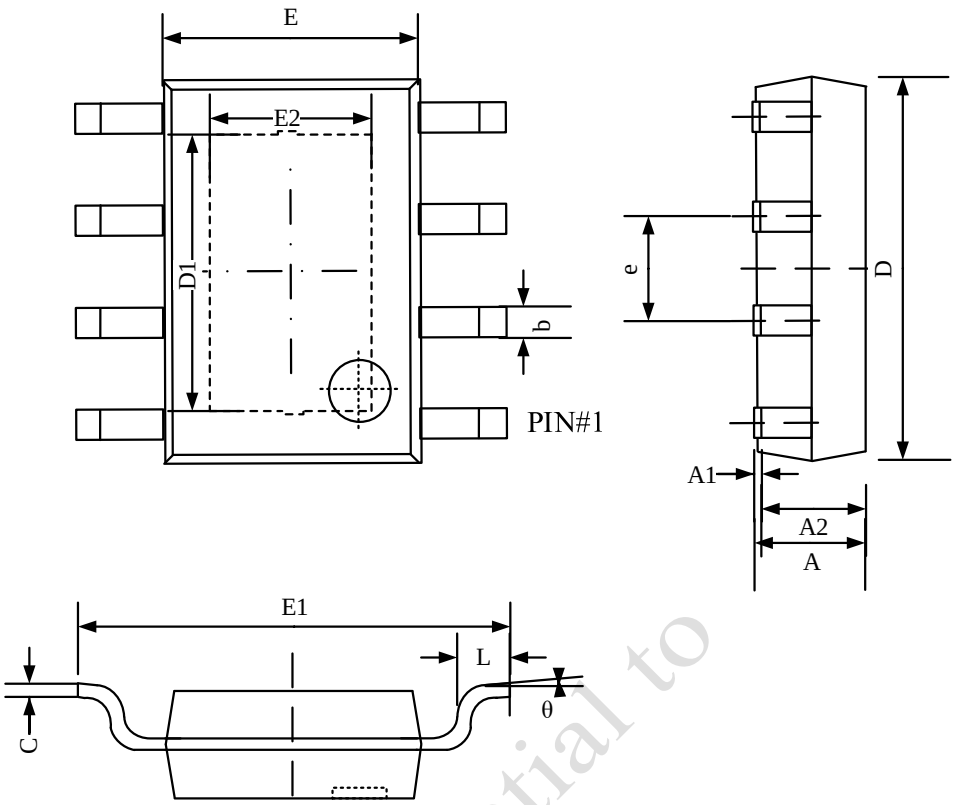
Top mark	Package
PN PN7011 YWWXXXXX	SOP8/PP

Note：Y：Year Code；WW：Week Code；XXXXX：Internal Code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

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Package Information SOP8/PP (95×130)



Size / Symbol	Min. (mm)	Max. (mm)	Size / Symbol	Min. (mm)	Max. (mm)
A	1.300	1.750	E	3.800	4.020
A1	0.000	0.200	E1	5.800	6.250
A2	1.300	1.550	E2	2.032	2.534
b	0.306	0.510	e	1.27	
c	0.156	0.250	L	0.400	1.270
D	4.700	5.100	θ	0°	18°
D1	3.100	3.467			

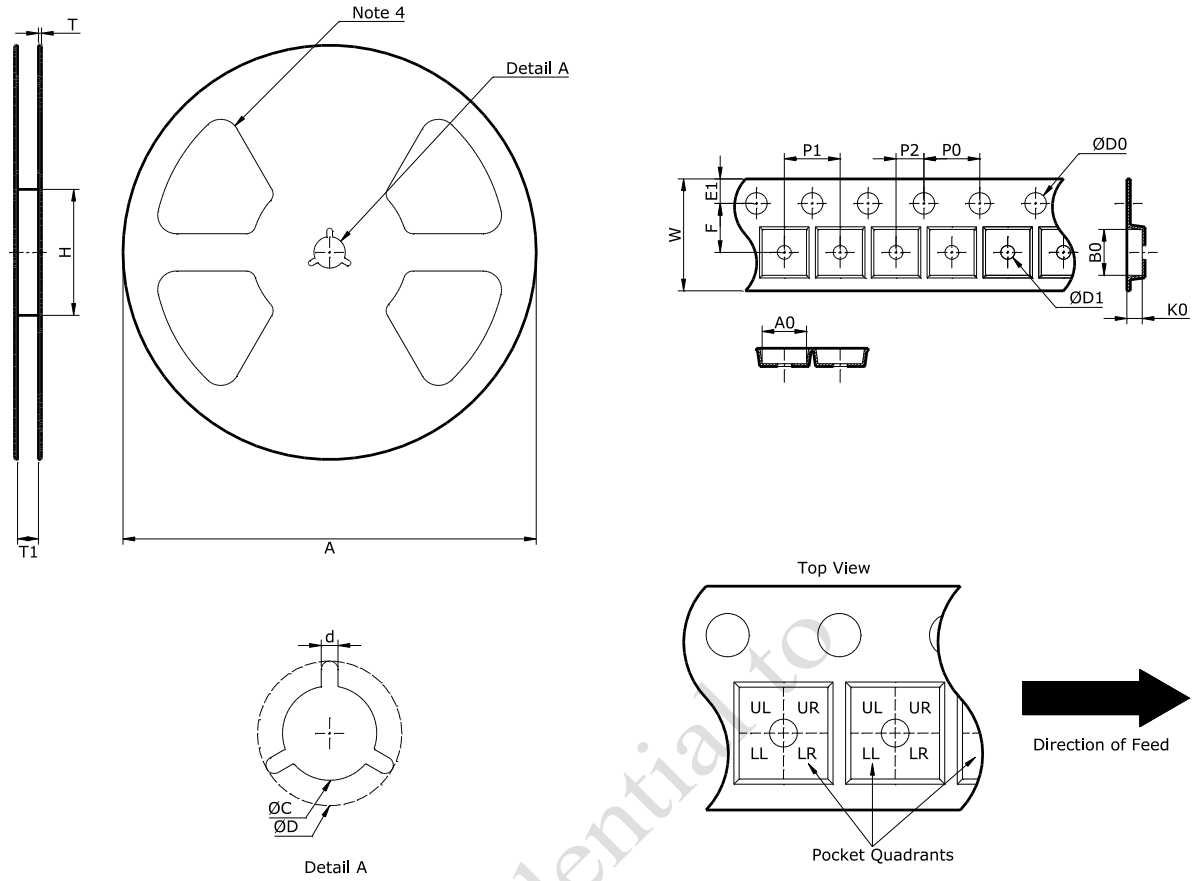
Top mark	Package
PN PN7011 YWWXXXXX	SOP8/PP

Note：Y：Year Code；WW：Week Code；XXXXX：Internal Code

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Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

Tape and Reel Information



SOP8 / SOP8/PP Package								
A (mm)	**T (mm)**	**T1 (mm)**	**H (mm)**	**ØC (mm)**	**d (mm)**	**A0 (mm)**	**B0 (mm)**	**K0 (mm)**
330 ±2.0	3max	14 +4.5/-4	100 ±2	13.4 +0.2/-0.6	2.5 ±1	6.60 +0.1/-0.3	5.3 +0.2/-0.1	2 ±0.2
W (mm)	**F (mm)**	**E1 (mm)**	**P0 (mm)**	**P1 (mm)**	**P2 (mm)**	**ØD0 (mm)**	**ØD1 (mm)**	**Pin 1 Quadrant**
12.00 ±0.3	5.50 ±0.1	1.75 ±0.10	4.00 ±0.10	8.0 ±0.1	2.0 ±0.1	1.5 +0.1/-0	1.5 +0.25/-0	UL

Notes:
1. This drawing is subjected to change without notice.
2. All dimensions are nominal and in mm.
3. This drawing is not in scale and for reference only. Customer can contact Chipown sales representative for further details.
4. The number of flange openings depends on the reel size and assembly site. This drawing shows an example only.

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