200V 3-Phase Gate Driver IC

General description

The ID2016 is a gate driver IC designed for three phase brushless DC motor driver applications. It is capable of driving three half bridges consisting of six N-channel power MOSFETs. iDriver's high-voltage process and common-mode noise canceling technique provide stable operation of high-side drivers under high dv/dt noise circumstances. Internal protection features include dead-time for over-shoot prevention, and VCC, VBS under voltage lockout.

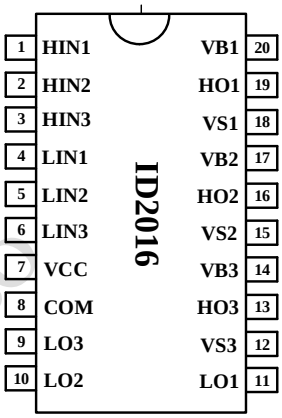
Features

- Fully operational to 200 V
- 3.3 V and 5 V input logic compatible
- VCC voltage range from 5.5 V to 16 V
- Built-in UVLO protections for all channels
- Built-in shoot-through prevention circuit for all channels with 200 ns typical dead time
- Typical 1 A/1 A sinking / sourcing output current
- Typically -7 V negative Vs bias capability

Application

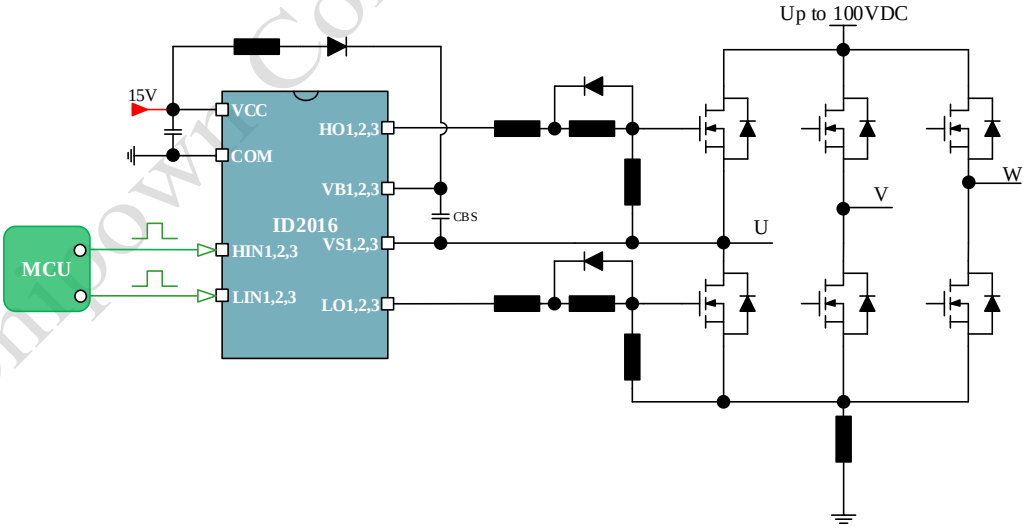
- BLDC Motor Controls
- Power tools
- E-bikes
- Servo Controls

Package/Order Information



Order code	Package
ID2016SDC-R1	TSSOP20

Schematic Diagram of Typical Application



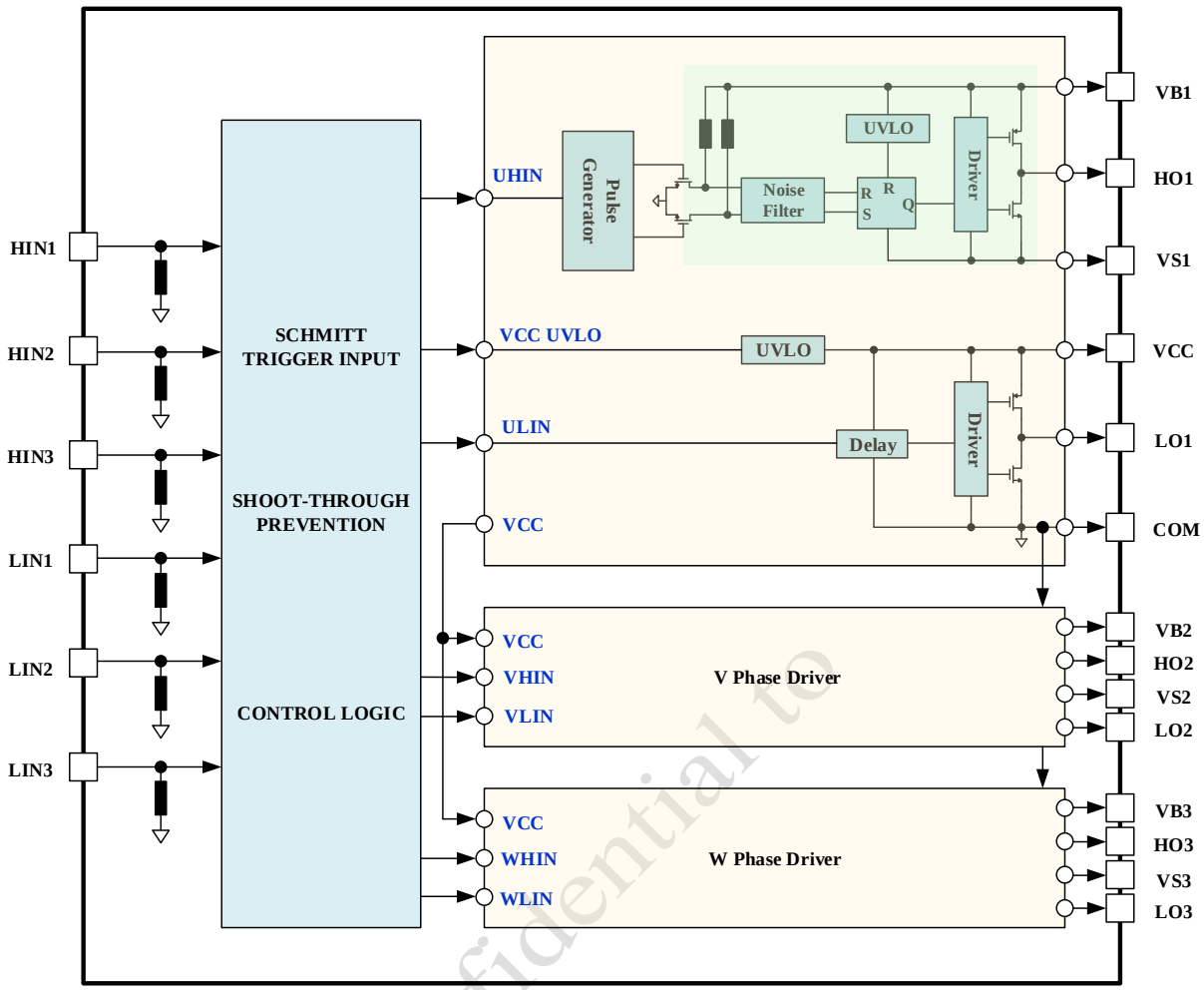
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Pin Definitions

Pin Name	Pin Number	Pin Function Description
HIN1	1	Logic input 1 for high-side gate 1 driver
HIN2	2	Logic input 2 for high-side gate 2 driver
HIN3	3	Logic input 3 for high-side gate 3 driver
LIN1	4	Logic input 1 for low-side gate 1 driver
LIN2	5	Logic input 2 for low-side gate 2 driver
LIN3	6	Logic input 3 for low-side gate 3 driver
VCC	7	Logic and all low-side gate drivers power supply voltage
COM	8	Ground
LO3	9	Low-side gate driver 3 output
LO2	10	Low-side gate driver 2 output
LO1	11	Low-side gate driver 1 output
VS3	12	High-side driver 3 floating offset voltage
HO3	13	High-side gate driver 3 output
VB3	14	High-side driver 3 floating supply voltage
VS2	15	High-side driver 2 floating offset voltage
HO2	16	High-side gate driver 2 output
VB2	17	High-side driver 2 floating supply voltage
VS1	18	High-side driver 1 floating offset voltage
HO1	19	High-side gate driver 1 output
VB1	20	High-side driver 1 floating supply voltage

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Block Diagram



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Absolute Maximum Ratings (1)

T_A =25 ℃, all voltages are referenced to VSS unless otherwise specified.

Symbol	Definition	MIN.	MAX.	Units
V_{CC}(4)	Supply voltage of LDO and gate driver	-0.3	20	V
$HIN_{1,2,3}$	Logic inputs for high-side gate driver outputs	-0.3	Vcc+0.3	
$LIN_{1,2,3}$	Logic inputs for low-side gate driver outputs	-0.3	Vcc+0.3	
$VB_{1,2,3}$(4)	High-side gate drive floating supply	-0.3	220	
$VS_{1,2,3}$	High voltage floating supply return	V_B-20	V_B+0.3	
$HO_{1,2,3}$	High-side driver outputs	V_S-0.3	V_B+0.3	
$LO_{1,2,3}$	Low-side driver outputs	-0.3	Vcc+0.3	
P_D	Package Power Dissipation @ $T_A \leq 25°C$	--	0.625	W
R_{thJA}	Thermal Resistance, Junction to Ambient	--	200	℃ /W
ESD(3)	HBM Model	2.5	--	kV
	CDM Model	200	--	V
T_J	Junction Temperature	--	150	℃
T_S	Storage Temperature	-55	150	

Note:
(1). Stresses outside the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to the Absolute Maximum Ratings for extended periods may affect device reliability.
(2). VHO and VLO pins can withstand -2V @ repetitive pulse less than 500ns (duty less than 1%).
(3). This device series incorporates ESD protection and is tested by the following methods:
ESD Human Body Model tested per ANSI/ESDA/JEDEC JS-001-2017.
ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS-002-2018.
(4). VCC/VBS ports contain clamping diode, the clamping voltage ensured by design.

Recommended Operating Conditions

Symbol	Definition	Min.	Max.	Units
V_{cc}	Supply voltage of LDO and gate driver	5.5	16	V
$HIN_{1,2,3}$	Logic inputs for high-side gate driver outputs	V_S	V_B	
$LIN_{1,2,3}$	Logic inputs for low-side gate driver outputs	0	Vcc	
$VB_{1,2,3}$	High-side gate drive floating supply	V_S+5.5	V_S+20	
$VS_{1,2,3}$	High voltage floating supply return	-7	200	
$HO_{1,2,3}$	High-side driver outputs	V_S	V_B	
$LO_{1,2,3}$	Low-side driver outputs	0	Vcc	
T_A	Ambient temperature	-40	125	℃

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Dynamic Electrical Characteristics

V_{BIAS} (Vcc, $V_{BS1, 2, 3}$) = 15V, C_L = 1000 pF and T_A = 25 ℃ unless otherwise specified.

Symbol	Definition	MIN	TYP.	MAX.	Units
t_{ON}	High-side and Low-side Turn-on Propagation Delay	--	150	300	ns
t_{OFF}	High-side and Low-side Turn-off Propagation Delay	--	150	300	
t_R	Turn-on Rise Time	--	40	60	
t_F	Turn-off Fall Time	--	25	40	
DT	Dead Time | HO - LO |	100	200	300	
	Dead Time | LO - HO |	100	200	300	
MT_t_{ON}	Turn-on Delay Matching | tON(H) - tOFF(L) |	--	--	30	
MT_t_{OFF}	Turn-off Delay Matching | tOFF(H) - tON(L) |	--	--	30	

Static Electrical Characteristics

(V_{BIAS} (V_{CC}, $V_{BS1, 2, 3}$) = 15 V, T_A=25 ℃, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND. The V_O and I_O parameters are referenced to GND and $V_{S1, 2, 3}$ and are applicable to respective outputs $L_{O1, 2, 3}$ and $H_{O1, 2, 3}$.

Symbol	Definition	MIN.	TYP.	MAX.	Units
I_{QCC}	Quiescent V_{CC} supply current	--	300	400	μA
I_{QBS}	Quiescent V_{BS} supply current per phase	--	30	60	
I_{LK}	Leakage Current (V_B=V_S=220 V)	--	0.1	10	
V_{CCUV+}	V_{CC} Under-Voltage Positive-Going Threshold	3.9	4.5	5.1	V
V_{CCUV-}	V_{CC} Under-Voltage Negative-Going Threshold	3.7	4.3	4.9	
U_{VHYS+}	V_{CC} threshold hysteresis	--	0.2	--	
V_{BSUV+}	V_{BS} Under-Voltage Positive-Going Threshold	3.3	4.0	4.7	
V_{BSUV-}	V_{BS} Under-Voltage Negative-Going Threshold	3.1	3.8	4.5	
U_{VBSHYS}	V_{BS} threshold hysteresis	--	0.2	--	
V_{IH}	High level input threshold voltage	2.5	--	--	
V_{IL}	Low level input threshold voltage	--	--	0.8	
R_{INPD}	Input pull down resistance	--	200	--	kΩ
I_{IN+}	INPUT bias current (HO=high)	--	25	40	μA
I_{IN-}	INPUT bias current (HO=low)	--	--	2	
I_{O+}(1)	Output high short circuit pulsed current	---	1	--	A
I_{O-}(1)	Output low short circuit pulsed current	--	1	--	
V_{OH}	High level output voltage (I_O=2 mA)	--	0.1	0.3	V
V_{OL}	Low level output voltage (I_O=2 mA)	--	0.05	0.3	

Note:
(1). Ensured by design.

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Function Timing Diagram

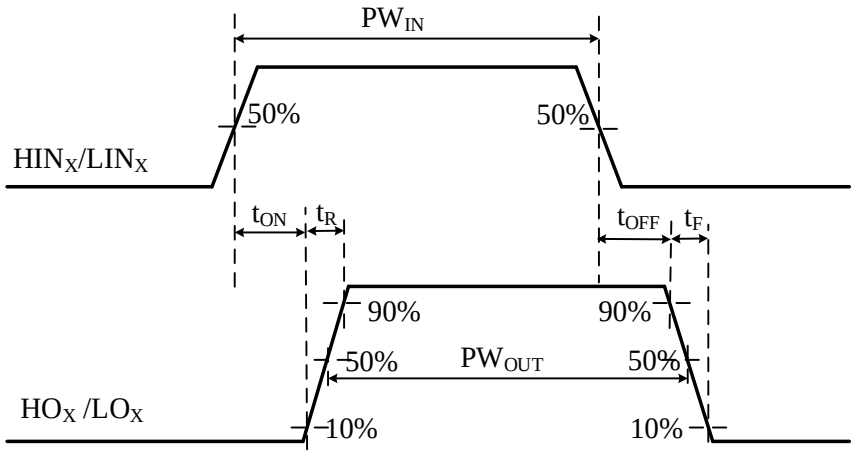


Fig.1 Switching Time Waveform Definitions

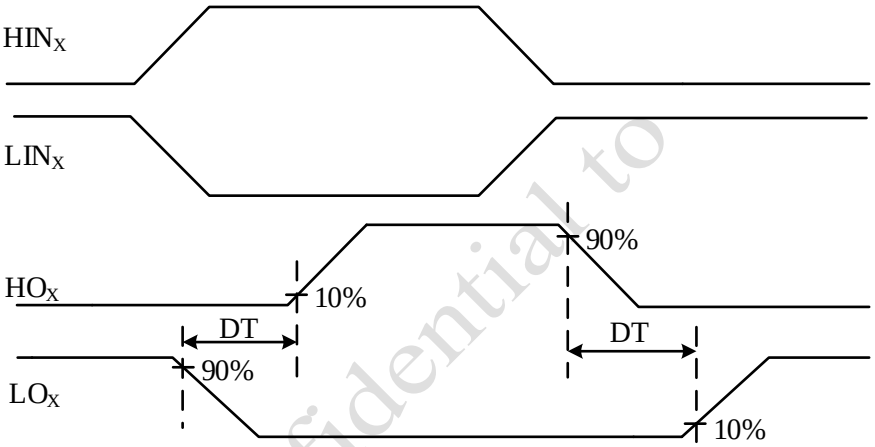


Fig.2 Dead time Waveform Definitions

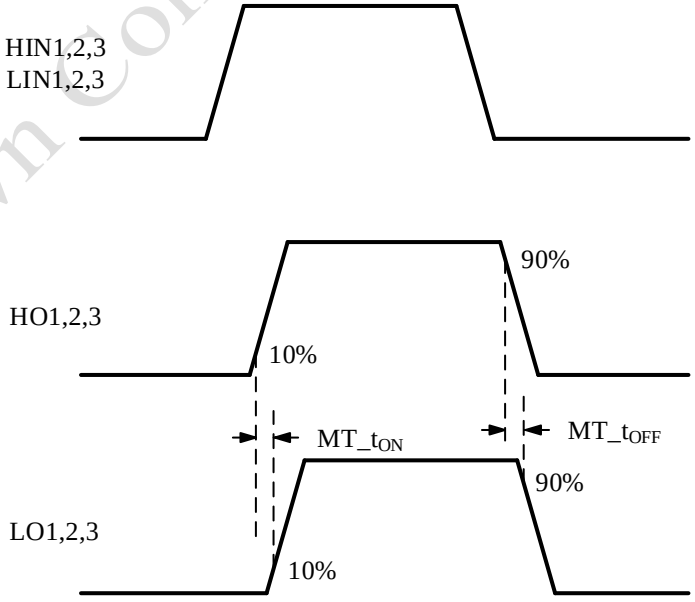
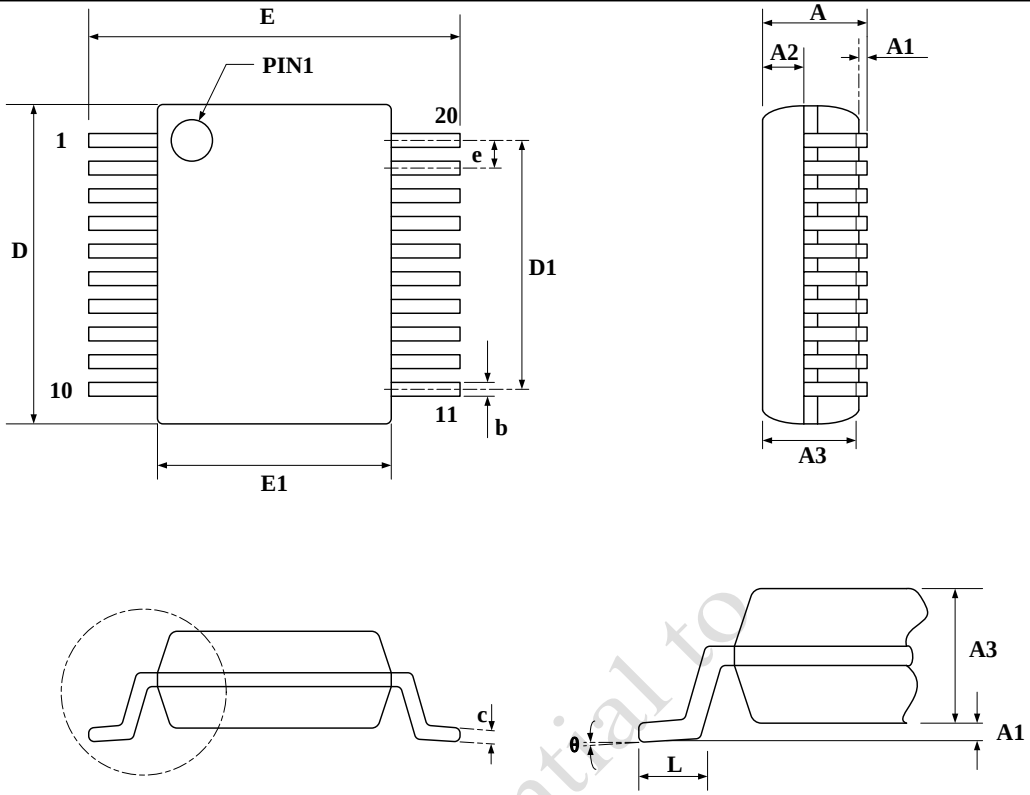


Fig.3 Matching time Waveform Definitions

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Package Information

TSSOP20 Package Outlines and Dimensions



Symbol \ Size	Min. (mm)	Max. (mm)	Symbol \ Size	Min. (mm)	Max. (mm)
A	--	1.20	E	6.20	6.60
A1	0.05	0.15	E1	4.30	4.50
A2	0.80	1.05	e	0.65(BSC)	
b	0.19	0.30	L	0.45	0.75
c	0.14	0.16	θ	0 °	8 °
D	6.40	6.60			

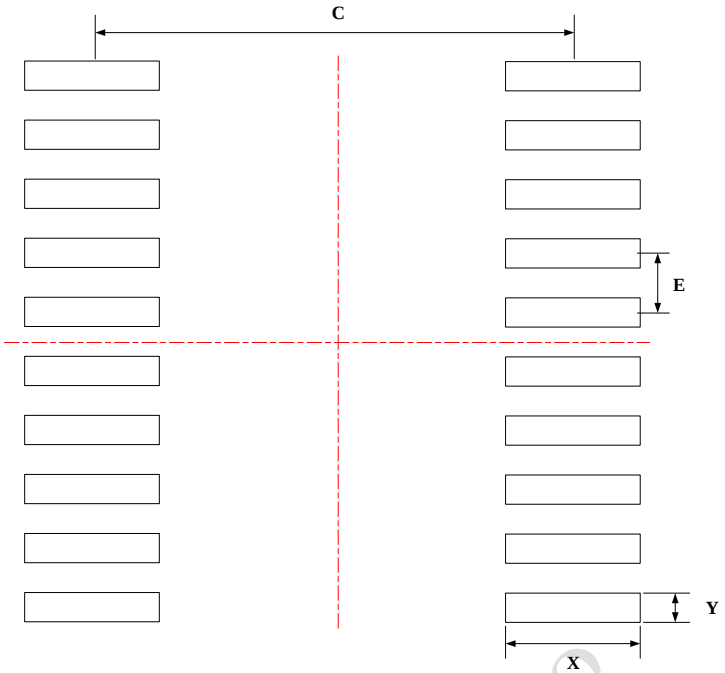
Top mark	Package
iDR. ID2016 YWWXXXXX	TSSOP20

Note: Y: Year Code; WW: Week Code; XXXXX: Internal Code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

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TSSOP20 Package PCB Footprint



TSSOP20 PCB Land Pattern Dimensions

Symbol	Dimension	
	Min	Max
c	5.50	5.60
E	0.65(BSC)	
X	1.55	1.60
Y	0.25	0.30

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