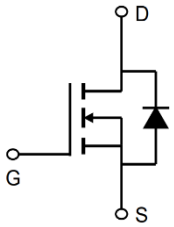
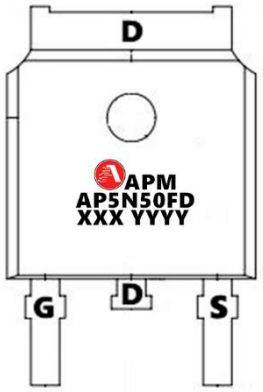
AP5N50FD

500V N+FRD-Channel Enhancement Mode MOSFET

Description

The AP5N50FD is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.





General Features

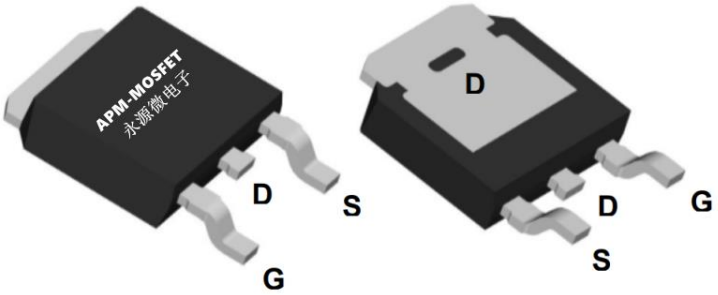
V_{DS} = 500V I_D =5A

$R_{DS(ON)}$ < 1.8Ω @ V_{GS}=10V **（Type：1.3Ω）**

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP5N50FD	TO-252-3L	AP5N50FD XXX YYYY	2500

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage	500	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V	5	A
I_D@T_C=100℃	Drain Current, V_{GS} @ 10V	3	A
IDM	Pulsed Drain Current	25	A
VGS	Gate-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy	247	mJ
P_D@T_C=25℃	Power Dissipation	32.9	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	℃
RthJC	Thermal Resistance, Junction-to-Case	1.5	℃/W
RthJA	Thermal Resistance, Junction-to-Ambient	33	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	500	550	--	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}=650V, V_{GS}= 0V, T_J=25ºC	--	--	1	μA
IGSS	Gate-Source Leakage	V_{GS} = ±30V	--	--	±100	nA
VGS(th)	Gate-Source Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2.0	3.0	4.0	V
RDS(on)	Drain-Source On-Resistance (Note3)	V_{GS}=10V, I_D=2.5A	--	1.3	1.8	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=25V, f=1.0MHz	--	516	--	pF
C_{oss}	Output Capacitance		--	59	--	
C_{rss}	Reverse Transfer Capacitance		--	8	--	
Q_g	Total Gate Charge	V_{DD}=240V, I_D=5A, V_{GS}=10V	--	5	--	nC
Q_{gs}	Gate-Source Charge		--	4	--	
Q_{gd}	Gate-Drain Charge		--	14	--	
td(on)	Turn-on Delay Time	V_{DD}=250V, I_D=5A, R_G=10Ω V_{GS}=10V	--	12	--	ns
t_r	Turn-on Rise Time		--	13	--	
td(off)	Turn-off Delay Time		--	49	--	
t_f	Turn-off Fall Time		--	19	--	
IS	Continuous Body Diode Current	T_C=25 ºC	--	--	5.0	A
ISM	Pulsed Diode Forward Current		--	--	25	A
V_{SD}	Body Diode Voltage	T_J=25ºC, I_{SD}=5A, V_{GS}=0V	--	--	1.4	V
trr	Reverse Recovery Time	V_{GS}=0V,I_S=5A, di_F/dt =100A /μs	--	86	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.2	--	μC

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The EAS data shows Max. rating . IAS = 4.5A, VDD = 50V, RG = 25 Ω, Starting TJ = 25 ºC

3、The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

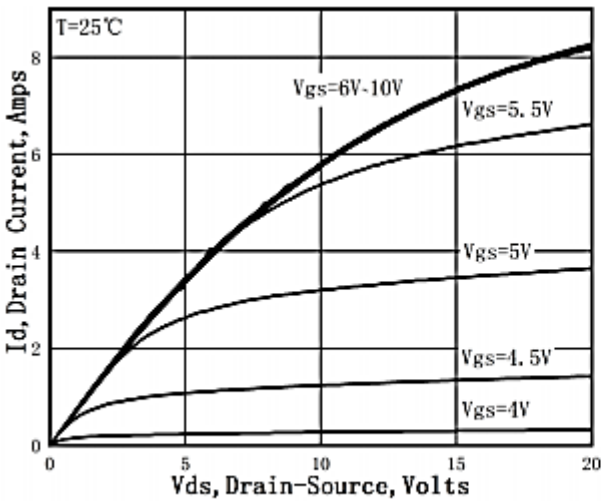


Figure 1.On-Region Characteristics

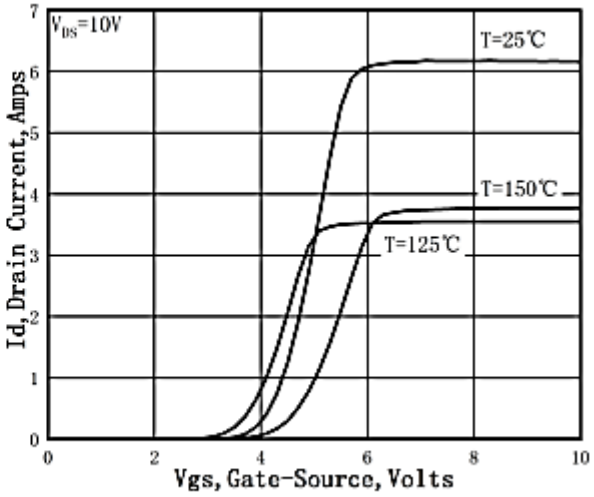


Figure 2. Transfer Characteristics

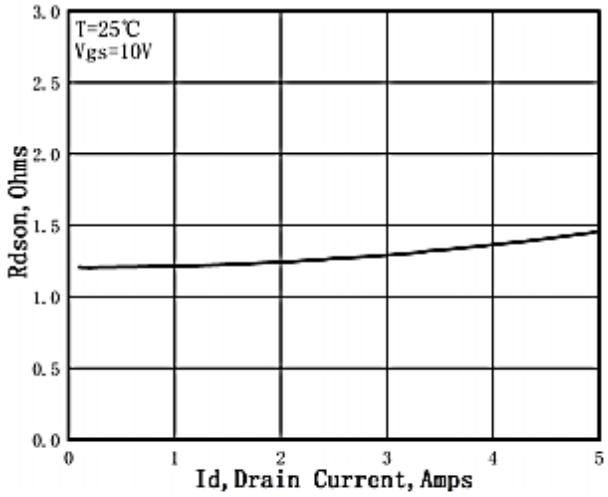


Figure 3.Static Drain-Source On Resistance

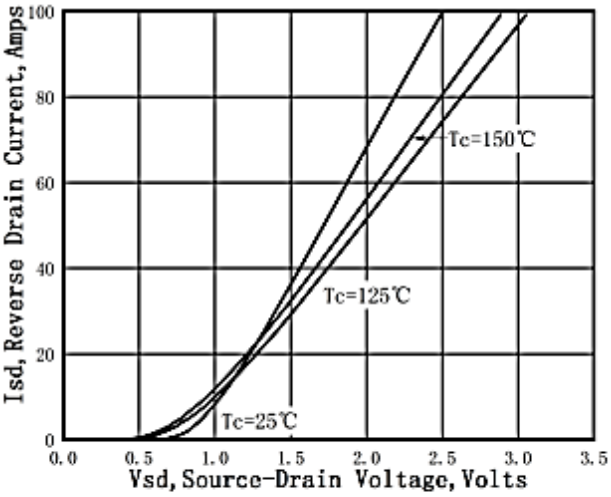


Figure 4. Typical Body Diode Transfer

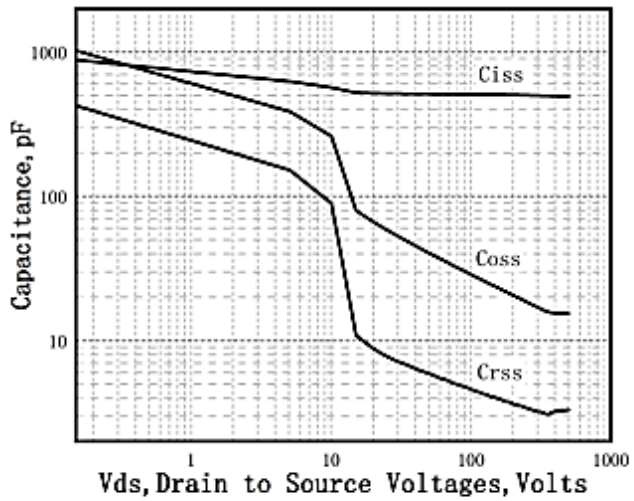


Figure 5 Capacitance Characteristics

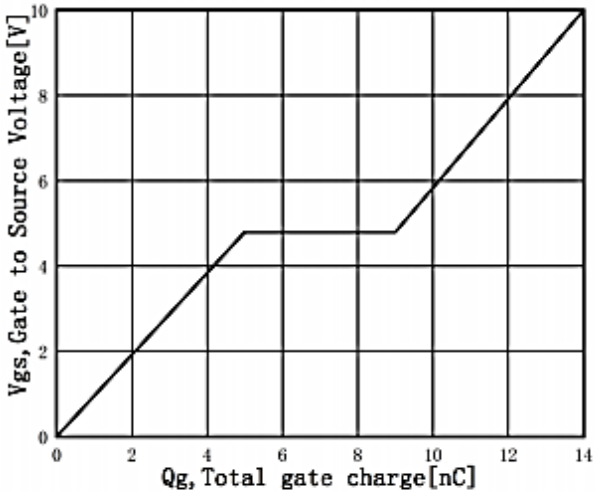


Figure 6. Gate Charge Characteristics

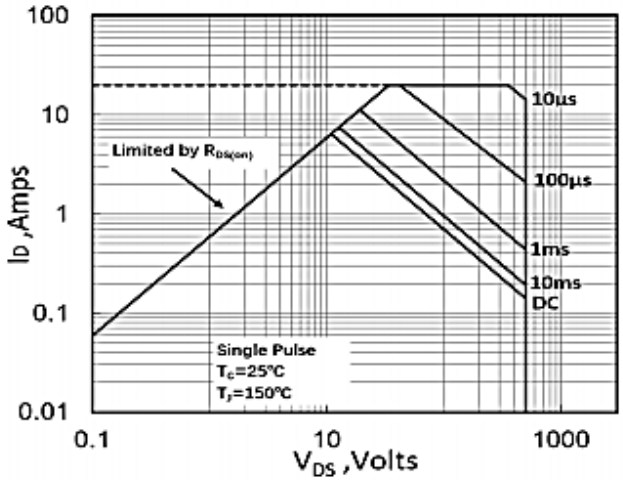


Figure 7. Maximum Safe Operating Area

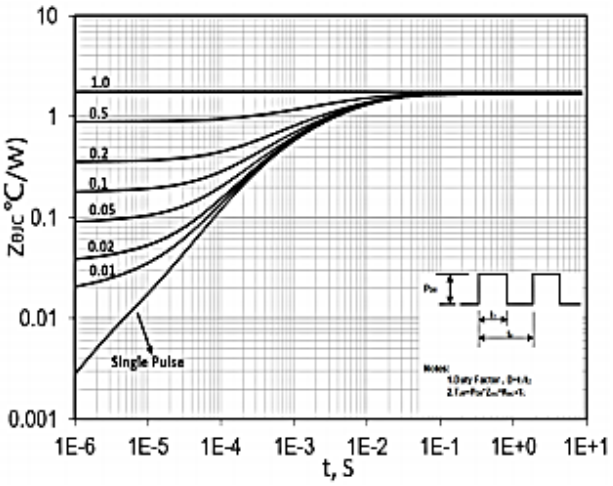
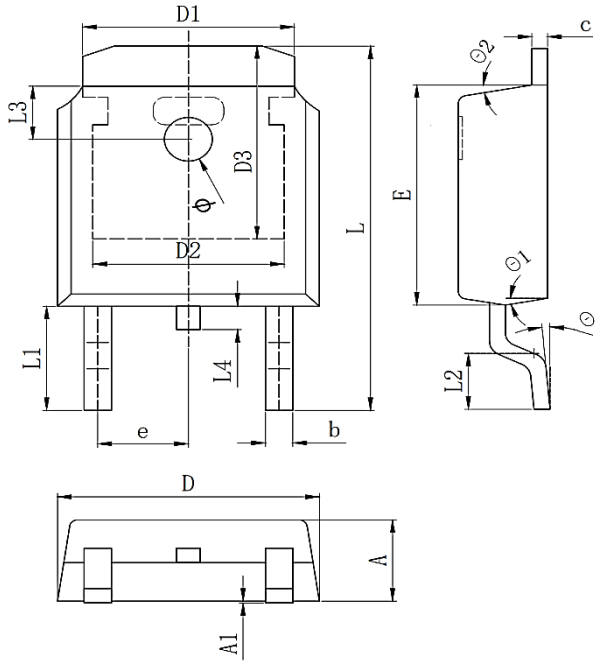


Figure 8. Transient Thermal Response Curve

Package Mechanical Data-TO-252-3L



Symbol	Dim in mm		
	Min	Typ	Max
A	2.1	2.3	2.5
A1	0	0.064	0.128
b	0.64	0.75	0.86
c	0.45	0.52	0.6
D	6.4	6.6	6.8
D1		5.33REF	
D2		4.83REF	
D3		5.25REF	
E	5.9	6.1	6.3
e		2.286TYP	
L	9.8	10.1	10.4
L1		2.888REF	
L2	1.4	1.5	1.7
L3		1.65REF	
L4	0.6	0.8	1
ϕ	1.1	1.2	1.3
θ	0°		10°
θ1	5°		10°
θ2	5°		10°

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500V N+FRD-Channel Enhancement Mode MOSFET

Edition	Date	Change
REV1.0	2021/1/31	Initial release

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