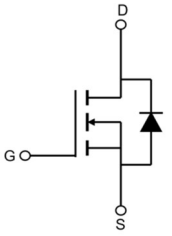
AP40N100K

N-Channel Enhancement Mosfet

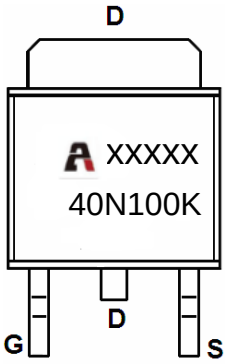
DATA SHEET

Feature

- 100V,40A
  $R_{DS(ON)}$ <23mΩ @V_{GS}=10V (TYP:18mΩ)
  $R_{DS(ON)}$ <33Ω @V_{GS}=4.5V (TYP:25 mΩ)
- Split Gate Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(ON)}$ and Low Gate Charge



Schematic Diagram



Marking and pin assignment

Application

- PWM applications
- Load Switch
- Power management

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
40N100K	AP40N100K	TO-252	13 Inch	-	2500

ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current (T_c =25℃)	I_D	40	A
Continuous Drain Current (T_c =100℃)	I_D	25	A
Pulsed Drain Current (1)	I_{DM}	120	A
Single Pulsed Avalanche Energy (2)	E_{AS}	64	mJ
Power Dissipation	P_D	50	W
Thermal Resistance from Junction to Case	$R_{\theta JC}$	2.65	℃/W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	62	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~ +150	℃

MOSFET ELECTRICAL CHARACTERISTICS(T_a=25℃ unless otherwise noted)

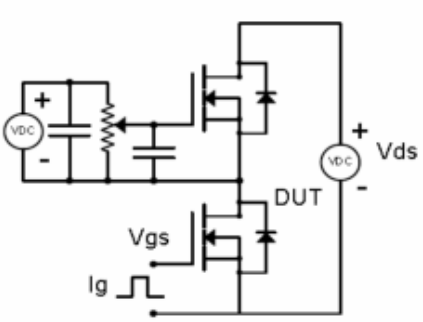
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	100	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS} =100V, V_{GS} = 0V	-	-	1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V, V_{DS} = 0V	-	-	±100	nA
Gate threshold voltage(3)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	1.2	1.8	2.8	V
Drain-source on-resistance(3)	$R_{DS(on)}$	V_{GS} =10V, I_D =15A	-	18	23	mΩ
		V_{GS} =4.5V, I_D =10A	-	25	33	mΩ
Forward Threshold Voltage	g_{fs}	V_{DS} =10V, I_D =20A	-	22	-	S
Gate Resistance	R_g	V_{DS} =V_{GS} =0V, f =1MHz	-	1.62	-	Ω
Dynamic characteristics						
Input Capacitance	C_{iss}	V_{DS} =50V, V_{GS} =0V, f =1MHz	-	822	-	pF
Output Capacitance	C_{oss}		-	310	-	
Reverse Transfer Capacitance	C_{rss}		-	23.5	-	
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	V_{DD}=50V, I_D=20A, V_{GS}=10V, R_G=3Ω	-	15	-	ns
Turn-on rise time	t_r		-	3.2	-	
Turn-off delay time	$t_{d(off)}$		-	30	-	
Turn-off fall time	t_f		-	7.6	-	
Total Gate Charge	Qg	VDS=50V, ID=20A, VGS=10V	-	22.7	-	nC
Gate-Source Charge	Qgs		-	6.2	-	
Gate-Drain Charge	Qgd		-	5.3	-	
Reverse Recovery Chrage	Qrr	I_F=20A,di/dt=100A/us		31		nC
Reverse Recovery Time	Trr	I_F=20A,di/dt=100A/us		34		ns
Source-Drain Diode characteristics						
Diode Forward voltage(3)	V_{DS}	V_{GS} =0V, I_S=10A	-	-	1.2	V
Diode Forward current(4)	I_S		-	-	40	A

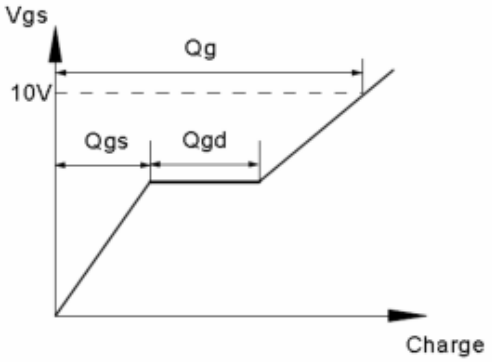
Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition:T_J=25℃,V_{DD}=50V,R_G=25Ω,L=0.5Mh
3. Pulse Test: pulse width≤300μs, duty cycle≤2%
4. Surface Mounted on FR4 Board,t≤10 sec

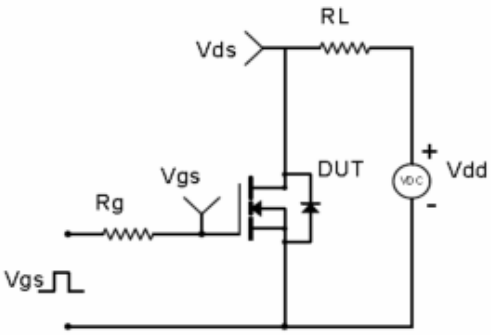
Test Circuit & Waveform

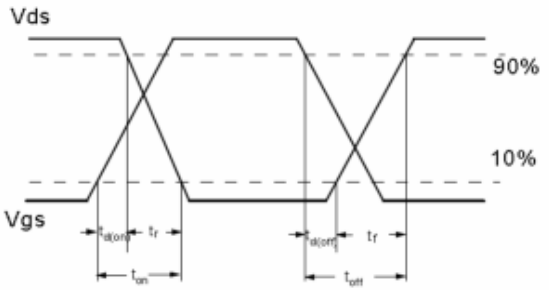
Gate Charge Test Circuit & Waveform



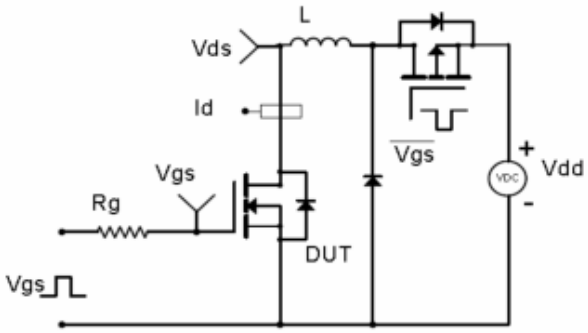


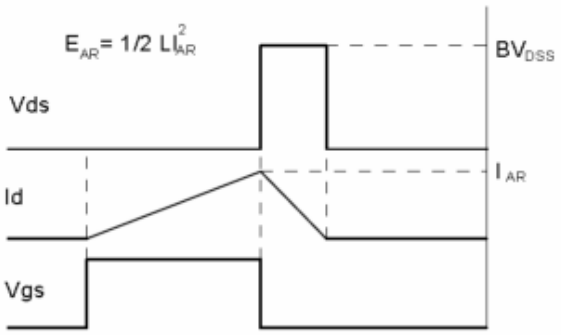
Resistive Switching Test Circuit & Waveforms



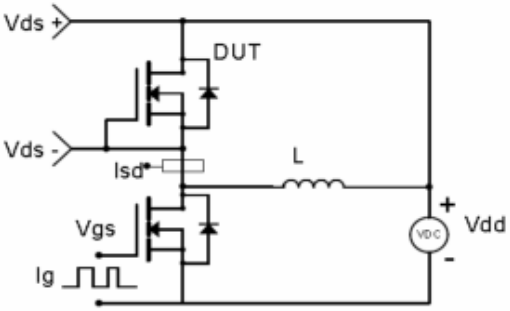


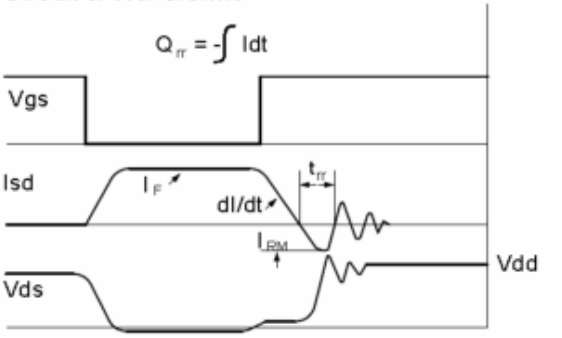
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms





Typical Performance Characteristics

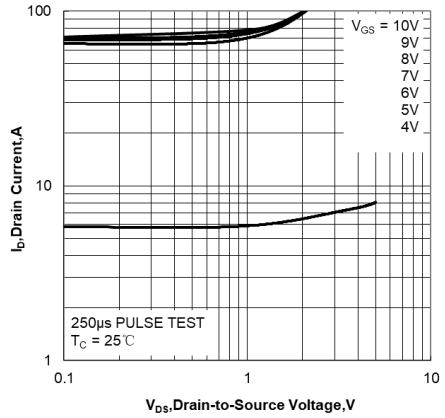


Figure 1. Output Characteristics

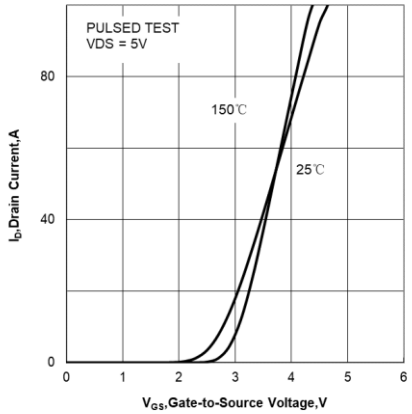


Figure 2. Transfer Characteristics

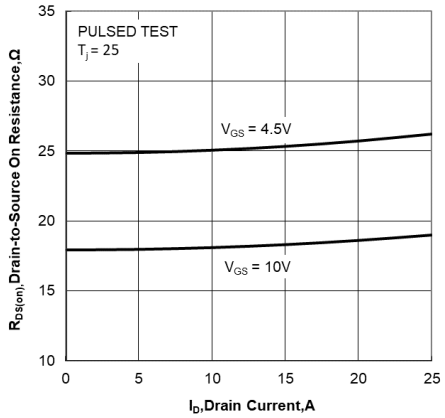


Figure 3. Drain-to-Source On Resistance vs Drain Current

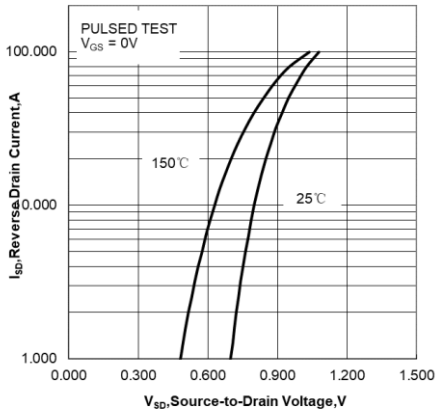


Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

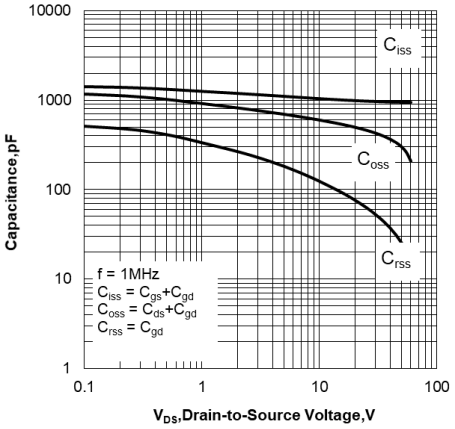


Figure 5. Capacitance Characteristics

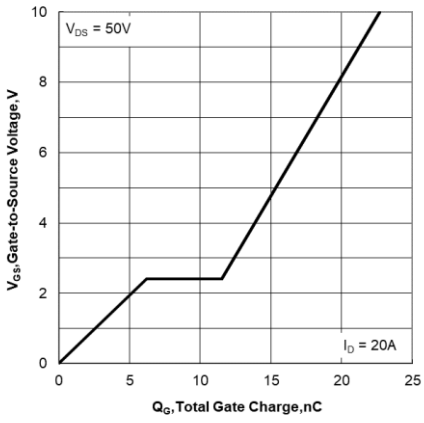


Figure 6. Gate Charge Characteristics

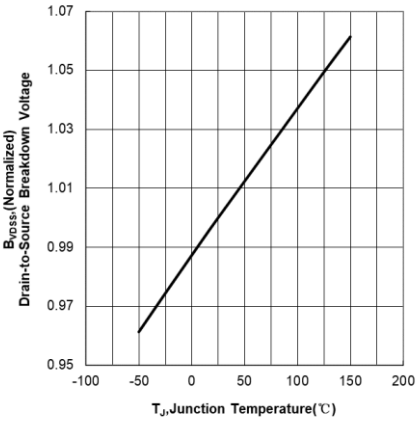


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

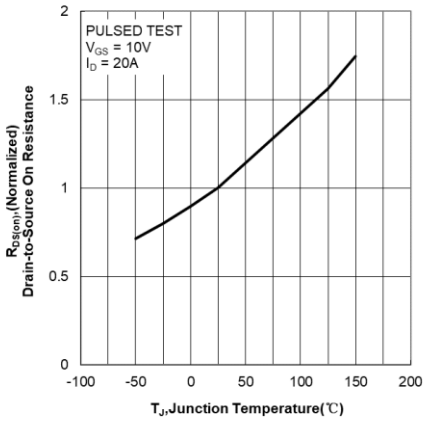


Figure 8. Normalized On Resistance vs Junction Temperature

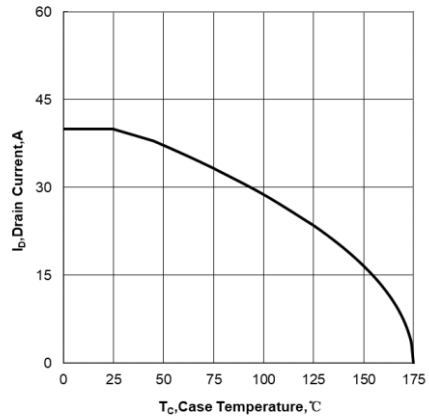


Figure 9. Maximum Continuous Drain Current vs Case Temperature

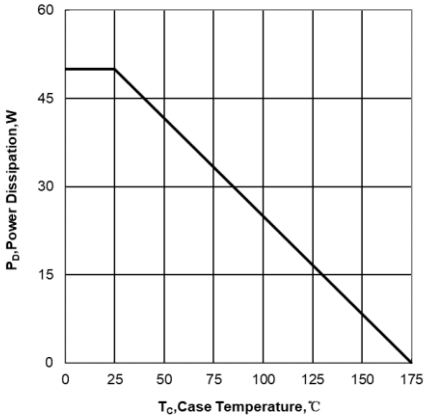


Figure 10. Maximum Power Dissipation vs Case Temperature

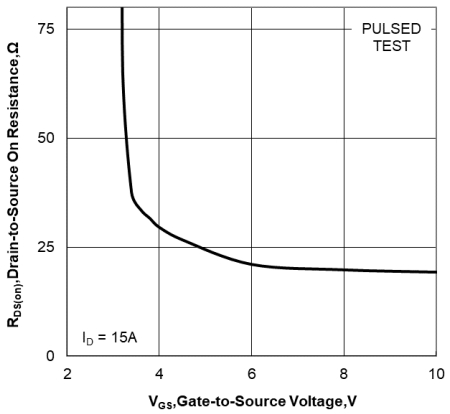


Figure11. Drain-to-Source On Resistance vs Gate Voltage and Drain Current

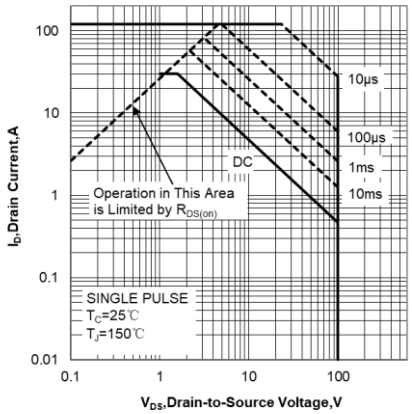


Figure 12. Maximum Safe Operating Area

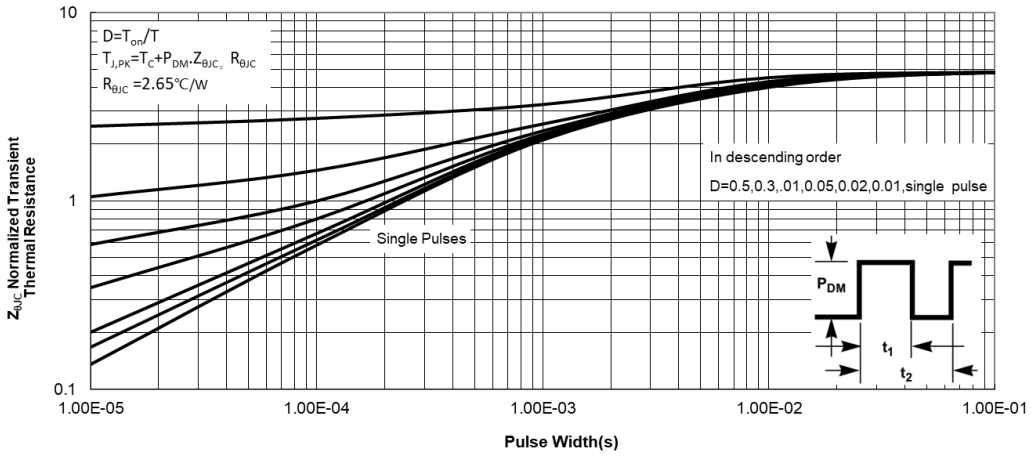
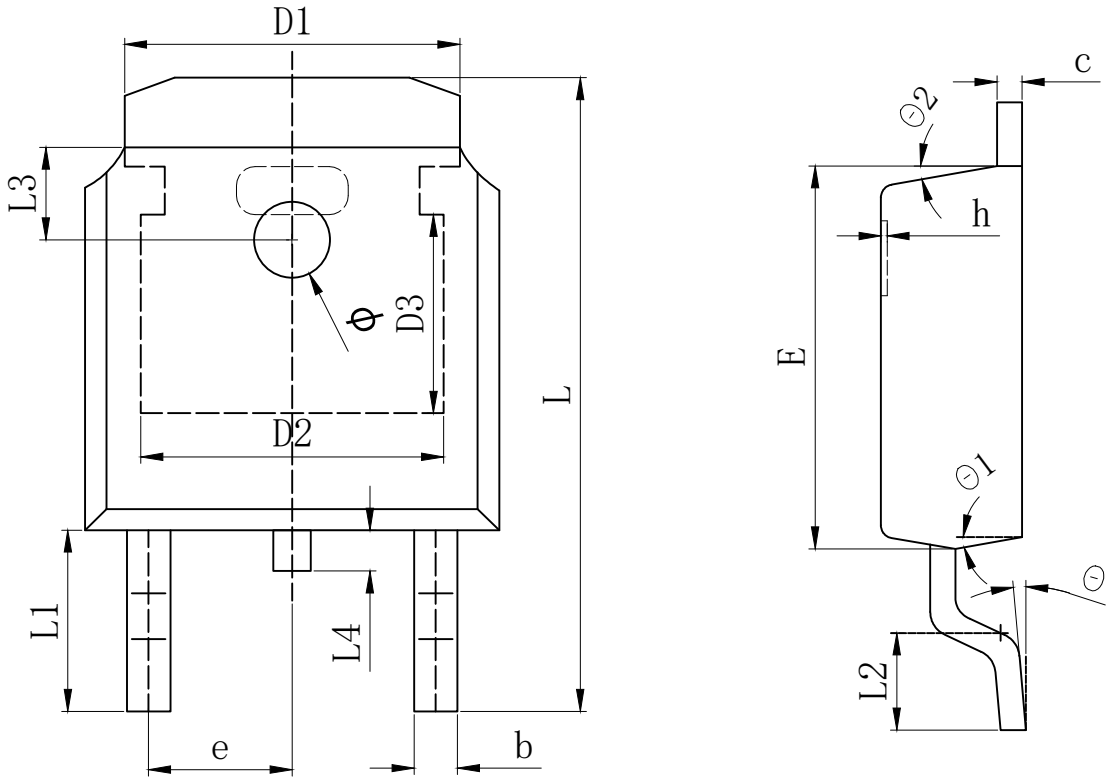
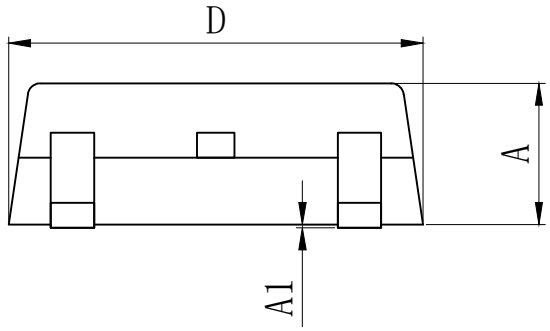


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

TO-252 Package Information





SYMBOL	MILLIMETER		
	MIN	Typ.	MAX
A	2.200	2.300	2.400
A1	0.000		0.127
b	0.640	0.690	0.740
c(电镀后)	0.460	0.520	0.580
D	6.500	6.600	6.700
D1	5.334 REF		
D2	4.826 REF		
D3	3.166 REF		
E	6.000	6.100	6.200
e	2.286 TYP		
h	0.000	0.100	0.200
L	9.900	10.100	10.300
L1	2.888 REF		
L2	1.400	1.550	1.700
L3	1.600 REF		
L4	0.600	0.800	1.000
Φ	1.100	1.200	1.300
θ	0°		8°
θ1	9° TYP		
θ2	9° TYP		

Revision History

Revision	Release	Remark
V1.1	2022/10/23	Initial Release

Disclaimer

The information given in this document describes the independent performance of the product,but similar performance is not guaranteed under other working conditions,and cannot be guaranteed when installed with other products or equipment.To achieve the required performance of the product in actual scenarios,the customer should conduct a complete application test to assess the functionality of the product.

Allpower assumes no responsibility for equipment failures result from using products at values that exceed the ratings,operating conditions,or other parameters listed in the product specifications.

The product described in this specification is not applicable for aerospace or other applications which requires high reliability.Customers using or selling these products for use in medical,life-saving,or life-sustaining applications do so at their own risk and agree to fully indemnify.

Due to product or technical improvements,the information described or contained herein may be changed without prior notice.