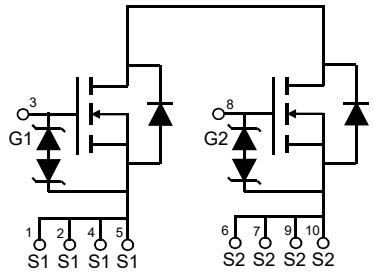
AP1213EED

Dual-N-Channel Enhancement Mosfet

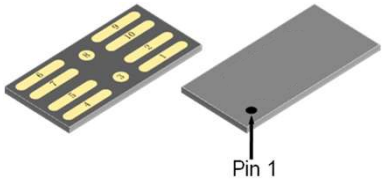
DATA SHEET

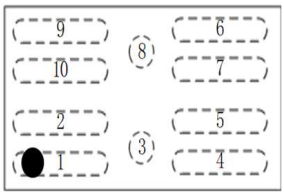
Feature

- $R_{SS(ON)}$ <2.4mΩ @V_{GS}=4.5V TYP=1.6 mΩ
  $R_{SS(ON)}$ <2.7mΩ @V_{GS}=3.8V TYP=1.8 mΩ
  $R_{SS(ON)}$ <3.5mΩ @V_{GS}=3.1V TYP=2.2 mΩ
  $R_{SS(ON)}$ <5.5mΩ @V_{GS}=2.5V TYP=3.5 mΩ
- Advanced Trench Technology
- Extremely Low RSS(ON)
- Common Drain Design
- Lead free product is acquired
- ESD ＞2KV



Equivalent Circuit





1,2,4,5. Source1 3. Gate1

6,7,9,10. Source2 8. Gate2

Application

- Battery Protection

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
1213EED	AP1213EED	WLCSP-10L	13 inch	-	5000

ABSOLUTE MAXIMUM RATINGS (T_j=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{SS}	12	V
Gate-Source Voltage	V_{GS}	±8	V
Continuous Drain Current (Tc =25℃) (1) (3)	I_{S1}	13	A
Continuous Drain Current (Tc =100℃) (1) (3)	I_{S1}	8.2	A
Continuous Drain Current (Tc =25℃) (1) (4)	I_{S2}	30	A
Continuous Drain Current (Tc =100℃) (1) (4)	I_{S2}	18.9	A
Pulsed Drain Current (1) (4)	I_{SM}	120	A
Power Dissipation (3)	P_{D1}	0.5	W
Power Dissipation (4)	P_{D2}	3.1	W
Thermal Resistance from Junction to Ambient (3)	$R_{\theta JA1}$	250	℃/W
Thermal Resistance from Junction to Ambient (4)	$R_{\theta JA2}$	40	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~ +150	℃

MOSFET ELECTRICAL CHARACTERISTICS(T_j=25℃ unless otherwise noted)

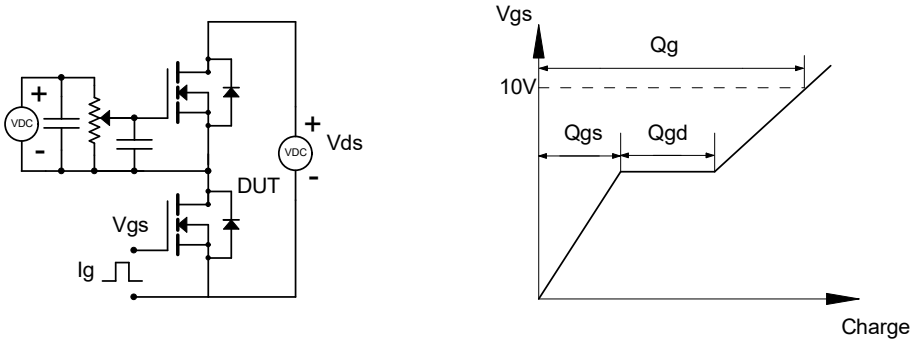
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)SSS}$	V_{GS} = 0V, I_D =250μA	12	-	-	V
Zero gate voltage drain current	I_{SSS}	V_{DS} =12V, V_{GS} = 0V	-	-	1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±8V,V_{DS} = 0V	-	-	±10	μA
Gate threshold voltage(2)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =1000μA	0.55	0.95	1.35	V
Drain-source on-resistance(2)	$R_{SS(on)}$	V_{GS} = 4.5 V, I_S = 4 A	-	1.6	2.4	mΩ
		V_{GS} = 3.8 V, I_S = 4 A	-	1.8	2.7	
		V_{GS} = 3.1 V, I_S = 4 A	-	2.2	3.5	
		V_{GS} = 2.5 V, I_S = 4 A	-	3.5	5.5	
Forward Source to Source Voltage	V_{FSS}	V_{GS} = 0 V, I_S = 4 A		0.6	1.2	V
Dynamic characteristics						
Input Capacitance	C_{iss}	V_{SS} =10V, V_{GS} =0V, f =1MHz	-	3500	-	pF
Output Capacitance	C_{oss}		-	450	-	
Reverse Transfer Capacitance	C_{rss}		-	400	-	
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	V_{SS}=6V, I_D=4A, V_{GS}=4.5V, R_G=3Ω	-	0.6	-	ns
Turn-on rise time	t_r		-	1.4	-	
Turn-off delay time	$t_{d(off)}$		-	6.6	-	
Turn-off fall time	t_f		-	4.0	-	
Total Gate Charge	Qg	V_{SS} =6V, ID=4A, V_{GS} =4.5V	-	23	-	nC
Gate-Source Charge	Qgs		-	11	-	
Gate-Drain Charge	Qgd		-	5	-	

Notes:

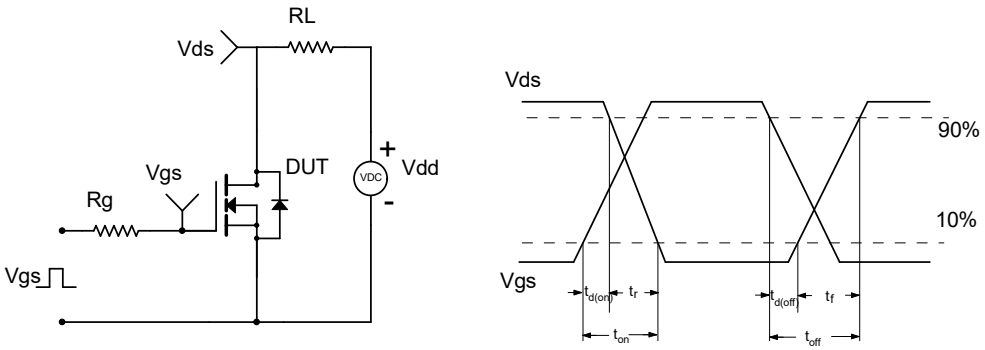
1. Repetitive Rating: pulse width limited by maximum junction temperature
2. Pulse Test: pulse width≤300μs, duty cycle≤2%
3. Mounted on FR4 Board（25.4mm*25.4mm*t1.0mm）using the minimum recommended pad size(36um Copper)
4. Mounted on Ceramic substrate(70mm*70mm*t1.0mm)

Test Circuit and Waveform

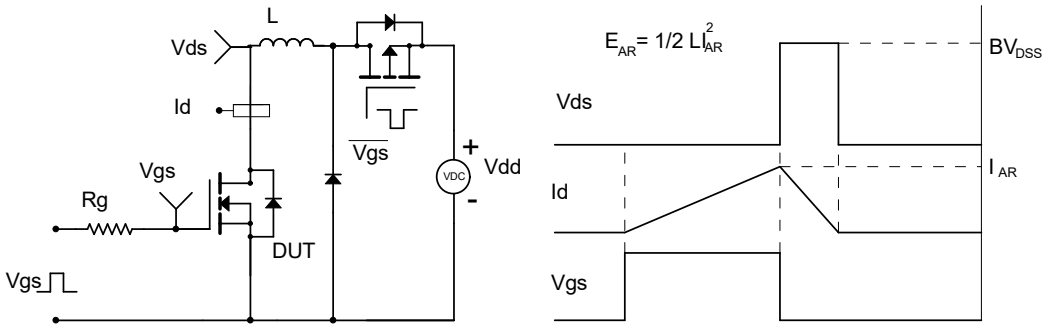
Gate Charge Test Circuit & Waveform



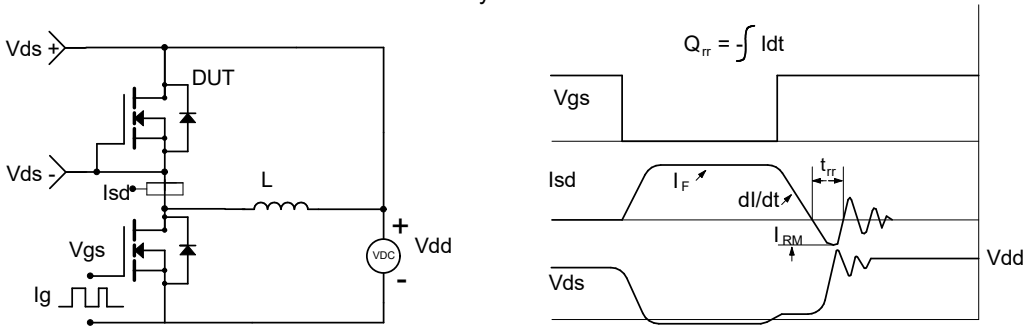
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Electrical Characteristics Diagrams

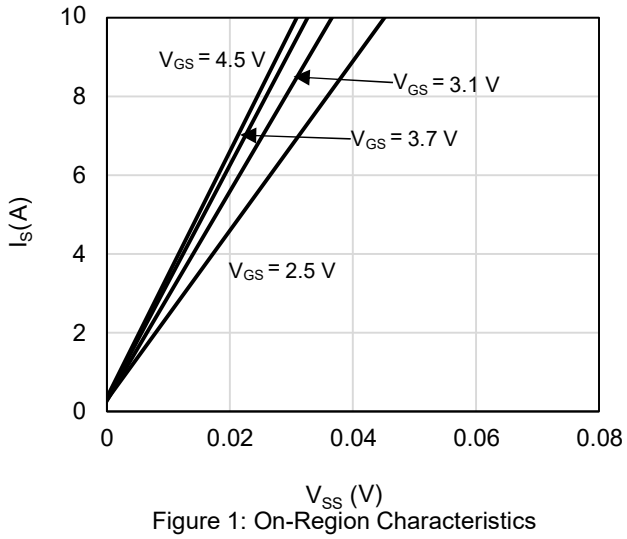


Figure 1: On-Region Characteristics

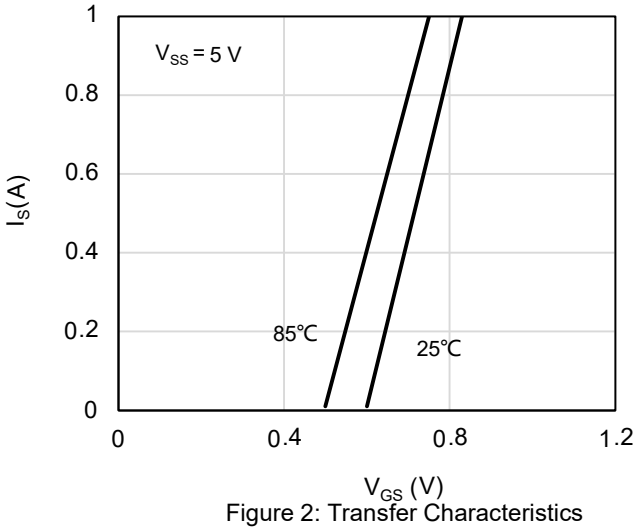


Figure 2: Transfer Characteristics

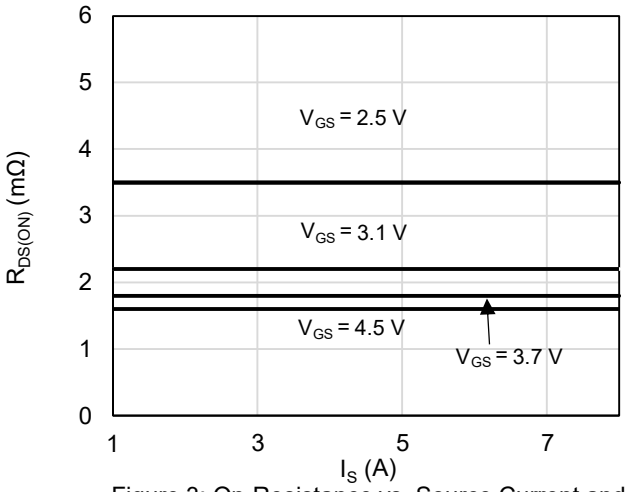


Figure 3: On-Resistance vs. Source Current and Gate Voltage

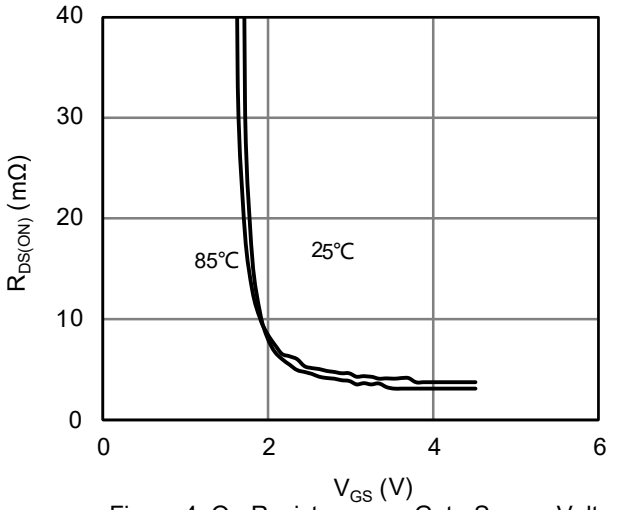


Figure 4: On-Resistance vs. Gate-Source Voltage

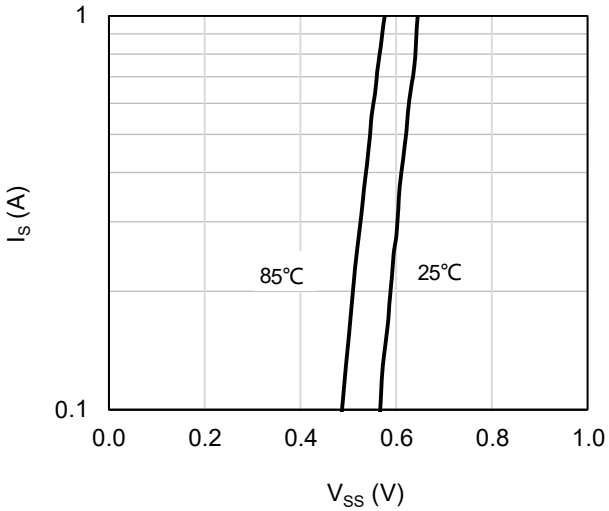


Figure 5: Body-Diode Characteristics

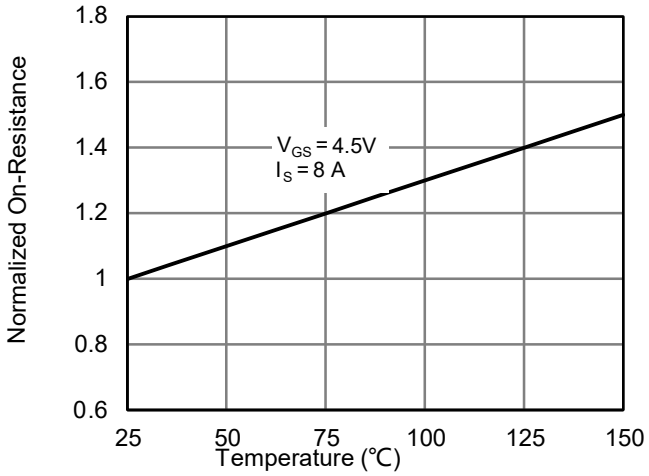


Figure 6: On-Resistance vs. Junction Temperature

Electrical Characteristics Diagrams

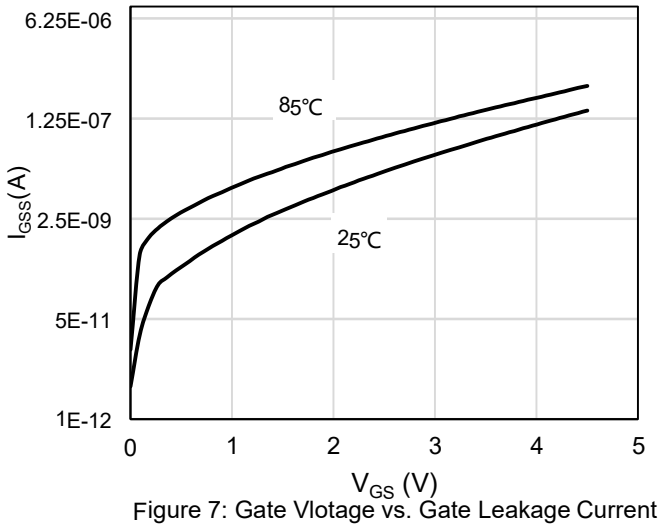


Figure 7: Gate Vlotage vs. Gate Leakage Current

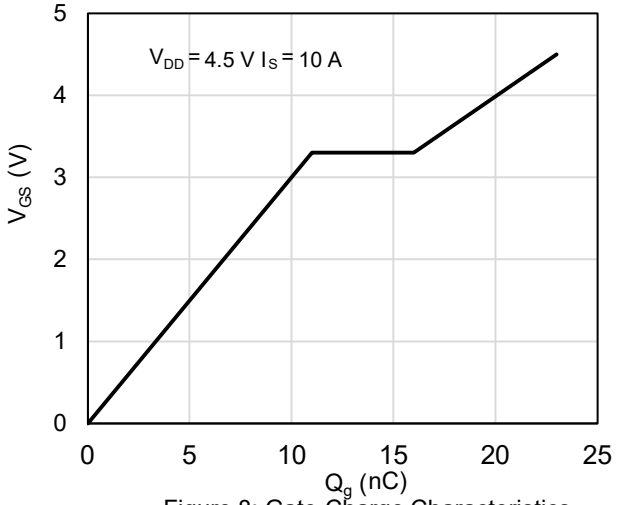


Figure 8: Gate-Charge Characteristics

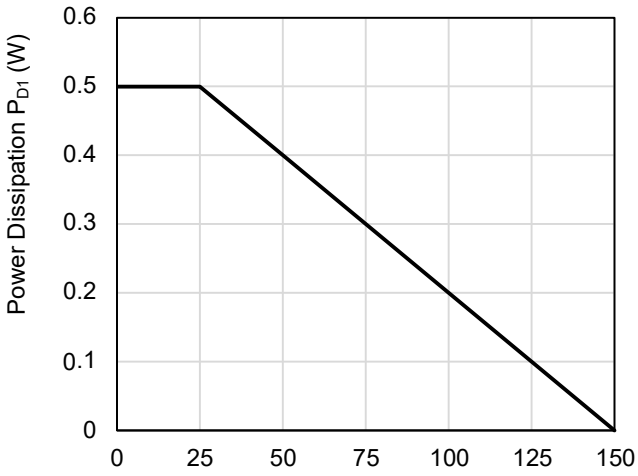


Figure 9: Power De-rating

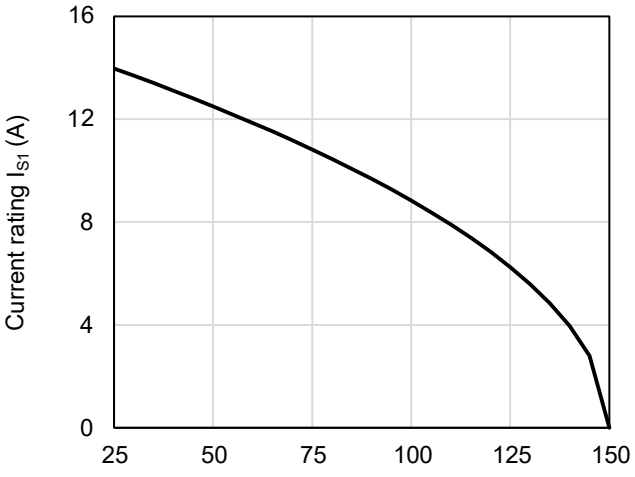


Figure 10: Current De-rating

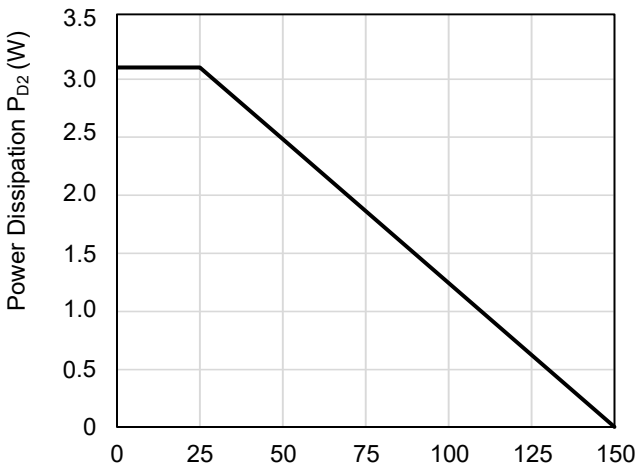


Figure 11: Power De-rating

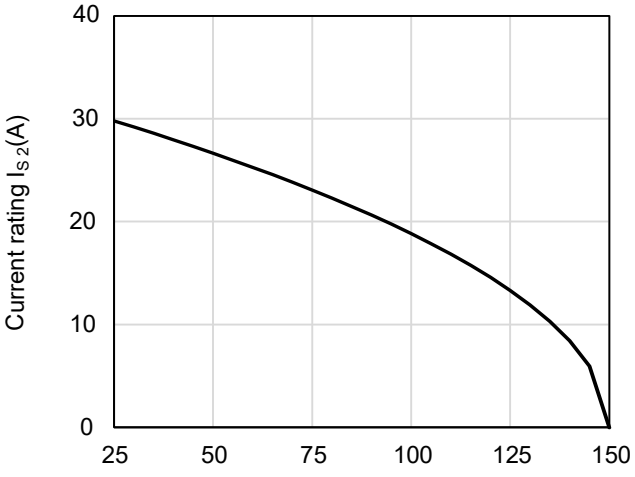


Figure 12: Current De-rating

Electrical Characteristics Diagrams

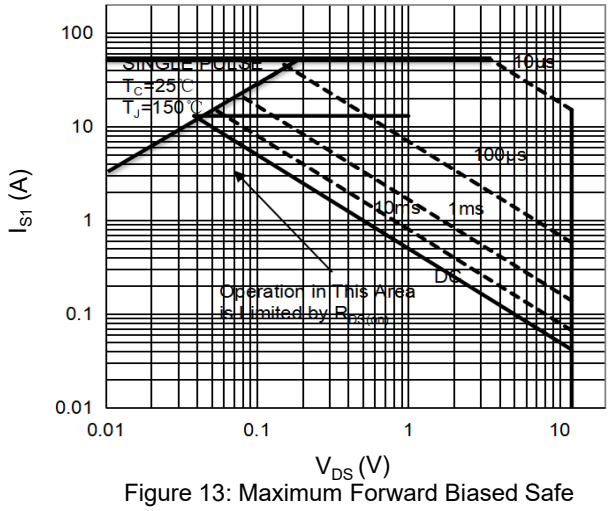


Figure 13: Maximum Forward Biased Safe Operating Area

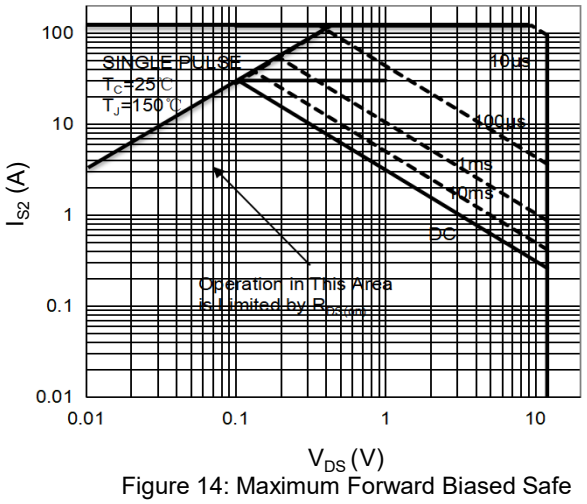


Figure 14: Maximum Forward Biased Safe Operating Area

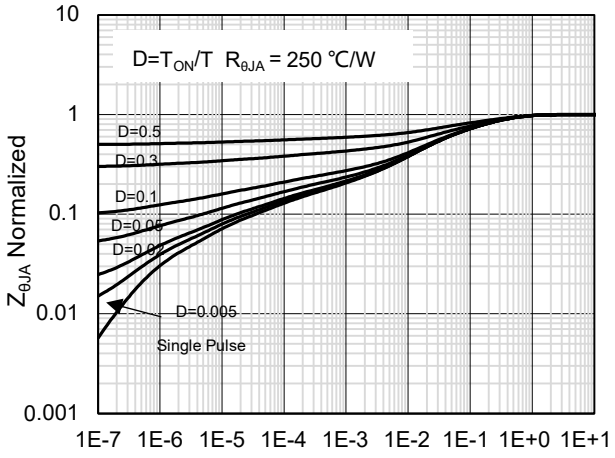
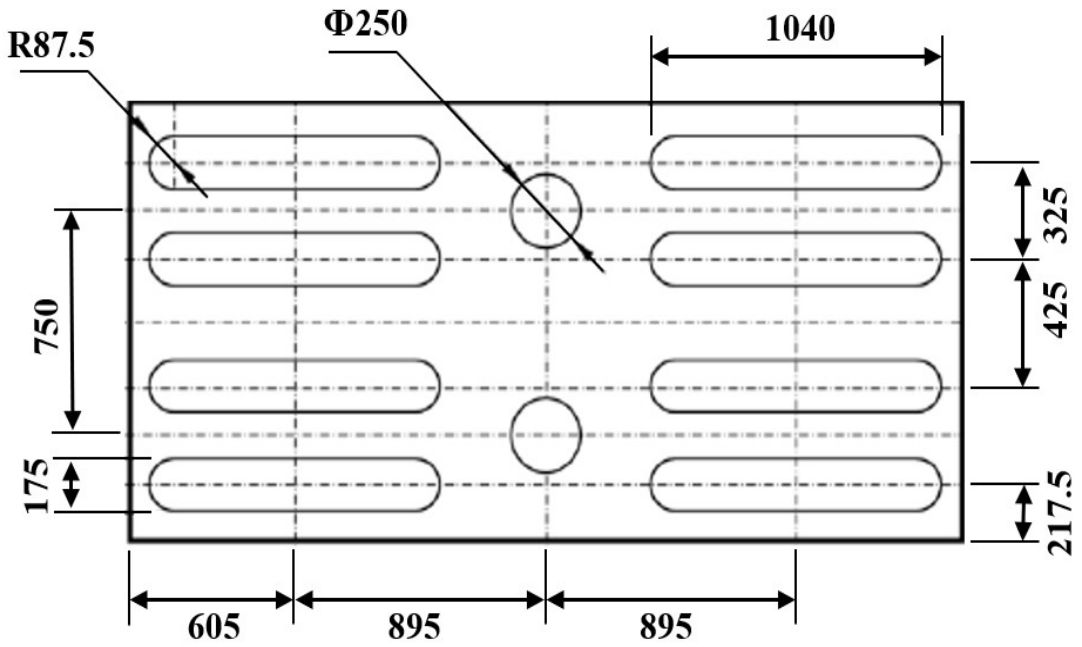


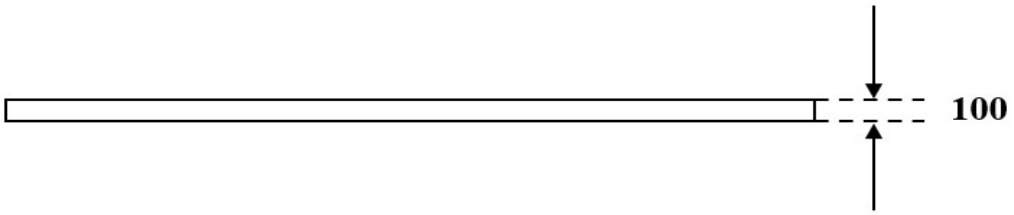
Figure 15: Normalized Maximum Transient Thermal Impedance

Package Outline

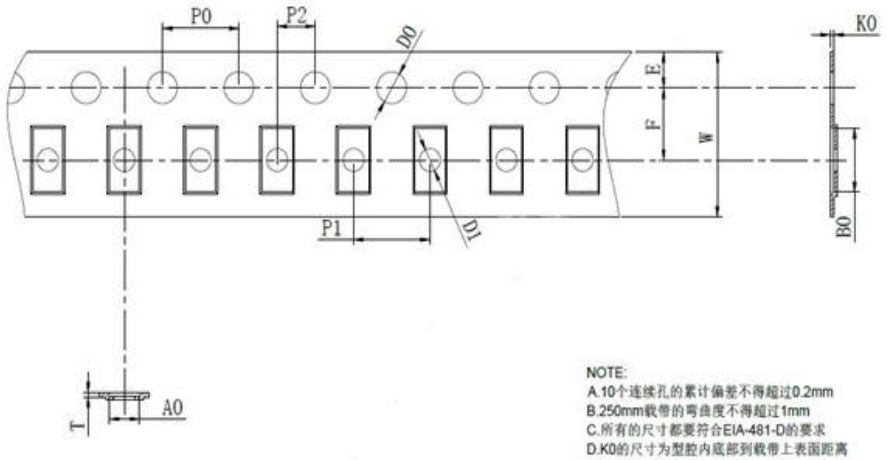
Bottom View unit : μm



Side View unit : μm



Reel and Tube Information



SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	1.60±0.05	3.10±0.05	0.18±0.05	4.00±0.10	4.00±0.10	2.00±0.05
SYMBOL	T	E	F	D0	D1	W
SPEC	0.20±0.05	1.75±0.10	3.50±0.05	1.50±0.05	1.10±0.10	$8.00^{+0.3}_{-0.1}$

NOTE:
A.10个连续孔的累计偏差不得超过0.2mm
B.250mm载带的弯曲度不得超过1mm
C.所有的尺寸都要符合EIA-481-D的要求
D.K0的尺寸为型腔内底部到载带上表面距离
E.材料:EC-AP2
F.A0&B0的测量位置在载带型腔最底部.
G.依据客户图纸绘制.
H. 供应商内部载带名称 "1429"

Revision History

Revision	Release	Remark
V1.0	2023/11/10	Initial Release
V1.1	2023/04/07	Add I_{S2},P_{D2},$R_{\theta JA2}$

Disclaimer

The information given in this document describes the independent performance of the product,but similar performance is not guaranteed under other working conditions,and cannot be guaranteed when installed with other products or equipment.To achieve the required performance of the product in actual scenarios,the customer should conduct a complete application test to assess the functionality of the product.

Allpower assumes no responsibility for equipment failures result from using products at values that exceed the ratings,operating conditions,or other parameters listed in the product specifications.

The product described in this specification is not applicable for aerospace or other applications which requires high reliability.Customers using or selling these products for use in medical,life-saving,or life-sustaining applications do so at their own risk and agree to fully indemnify.

Due to product or technical improvements,the information described or contained herein may be changed without prior notice.